INTEGRATED CIRCUITS

DATA HANDBOOK

Video and associated systems
Types FCB61C65 (L/LL) to TDA2655B

BOOK IC02a 1991

Philips Semiconductors

PHILIPS

Video and associated systems

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GENERAL

Product status definition for type numbers with prefixes NE, SA, SE and μA
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DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (–55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description

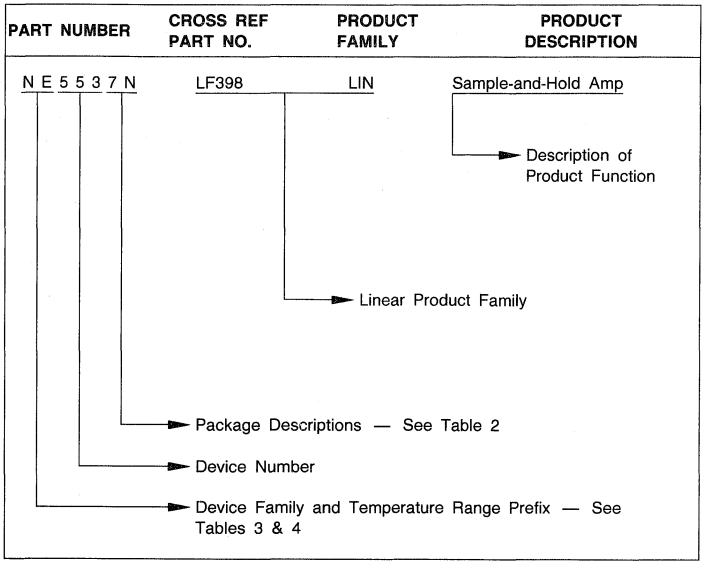


Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	–55°C to +125°C
SA	–40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard

Pro electron type designation code for integrated circuits

TYPE DESIGNATION

Basic type number

This type designation applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick- film and hybrid integrated circuits.

A basic type number consists of three letters followed by a serial number.

FIRST AND SECOND LETTER

Digital family circuits

The first two letters identify the family (see note 1).

Solitary circuits

The first letter divides the solitary circuits into:

S : solitary digital circuits
T : analog circuits
U : mixed analog/digital circuits

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 2).

Microprocessors

The first two letters identify microprocessors and correlated circuits as follows:

MA : microcomputer central processing unit
MB : slice processor (see note 3)
MD : correlated memories
ME : other correlated circuits (interface, clock, peripheral controller, etc.)

Charge-transfer devices and switched capacitors.

The first two letters identify the following:

NH : hybrid circuits
NL : logic circuits
NM : memories
NS : analog signal processing, using switched capacitors
NT : analog signal processing, using change-transfer device
NX : imaging devices
NY : other correlated circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range. The letters A to G give information about the temperature:

A : temperature range not specified below (see note 4)
B : 0 to + 70 °C
C : –55 to +125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example : the range 0 to +75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

Version letter(s)

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack (2 leads)
G : for flat pack (4 leads)
H : for quadrature flat pack (QFP)
L : for chip on tape (foil)
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Pro electron type designation code for integrated circuits

TYPE DESIGNATION

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : cylindrical
D : dual-in-line (DIL)
E : power DIL (with external heatsink)
F : flat (leads on 2 sides)
G : flat (leads on 4 sides)
H : quadrature flat pack (QFP)
K : diamond (TO-3 family)
M : multiple-in-line (except dual-, triple-, quadruple-in-line)
Q : quadruple-in-line (QIL)
R : power QIL (with external heatsink)
S : single-in-line
T : triple-in-line
W : lead chip-carrier (LCC)
X : leadless chip-carrier (LLCC)
Y : pin grid array (PGA)

SECOND LETTER: Material

C : metal-ceramic
G : glass-ceramic (cerdip)
M : metal
P : plastic

To avoid confusion when the serial number ends with a letter, a hyphen is used preceding the suffix.

Examples (see note 5)

PCF1105WP : Digital IC, PC family, operational temperature range –40 to +85 °C, serial number 1105, plastic leaded chip-carrier.

GMB74LS00A-DC: Digital IC, GM family, operational temperature range 0 to +70 °C, company number 74LSS00A, ceramic DIL package.

TDA1000P : Analog circuit, no standard temperature range, serial number 1000, plastic DIL package.

SAC2000 : Solitary digital circuit, operational temperature range –55 to +125 °C.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).

2. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

3. By 'slice processor' is meant: a functional slice of microprocessor.

4. In the case of two same types with two different temperature ranges not specified below, one type should use the letter 'A' as the third letter and the other, the letter 'X'.

5. Some companies have been using version letters and/or two letter-suffix, which differ from the Pro Electron definitions. In case of confusion Pro Electron may be contacted.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

Data sheet	
status	Product specification
date of issue	June 1990

FCB61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 55 ns and 70 ns
- Low current consumption:
  - active 70 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 100 µA max. (L-version)
  - standby (CMOS) 1 µA max. (LL-version)
- Suitable for battery back-up operation: (FCB61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 50 µA max. (L-version)
  - data retention current 1 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All inputs and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature 0 °C to +70 °C

GENERAL DESCRIPTION

The FCB61C65(L/LL) is a 65536-bit fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the low-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 55 ns and 70 ns.

The FCB61C65(L/LL) is ideally suited for memory applications where fast access time, low power and ease of use are required.

The FCB61C65(L/LL) is a CMOS device which uses a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCB61C65 (L/LL)-XXP	28	DIL (600 mil)	plastic	SOT117
FCB61C65 (L/LL)-XXT	28	SO28XL (330 mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

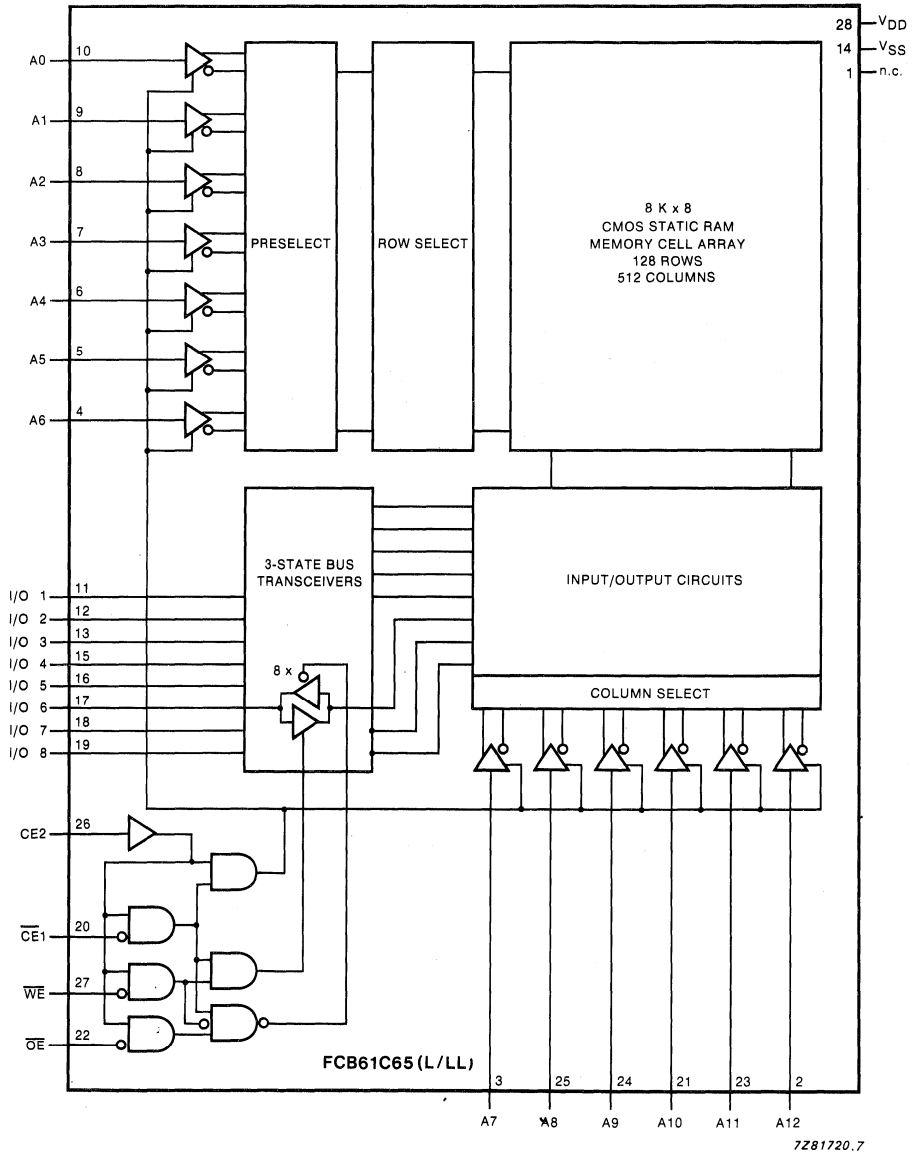


Fig.1 Block diagram.

Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

FCF61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 85 ns
- Low current consumption:
  - active 60 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 200 µA max. (L-version)
  - standby (CMOS) 4 µA max. (LL-version)
- Suitable for battery back-up operation: (FCF61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 100 µA max. (L-version)
  - data retention current 4 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All input and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature –40 °C to +85 °C

GENERAL DESCRIPTION

The FCF61C65(L/LL) is a 65536-bit, fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the lower-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 85 ns.

The FCF61C65(L/LL) is ideally suited for memory applications for the extended temperature range of –40 to +85°C where fast access time, low power and ease of use are required.

The FCF61C65(L/LL) is a full CMOS device using a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCF61C65 (L/LL)-85T	28	SO28XL(330mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM for extended temperature range

FCF61C65(L/LL)

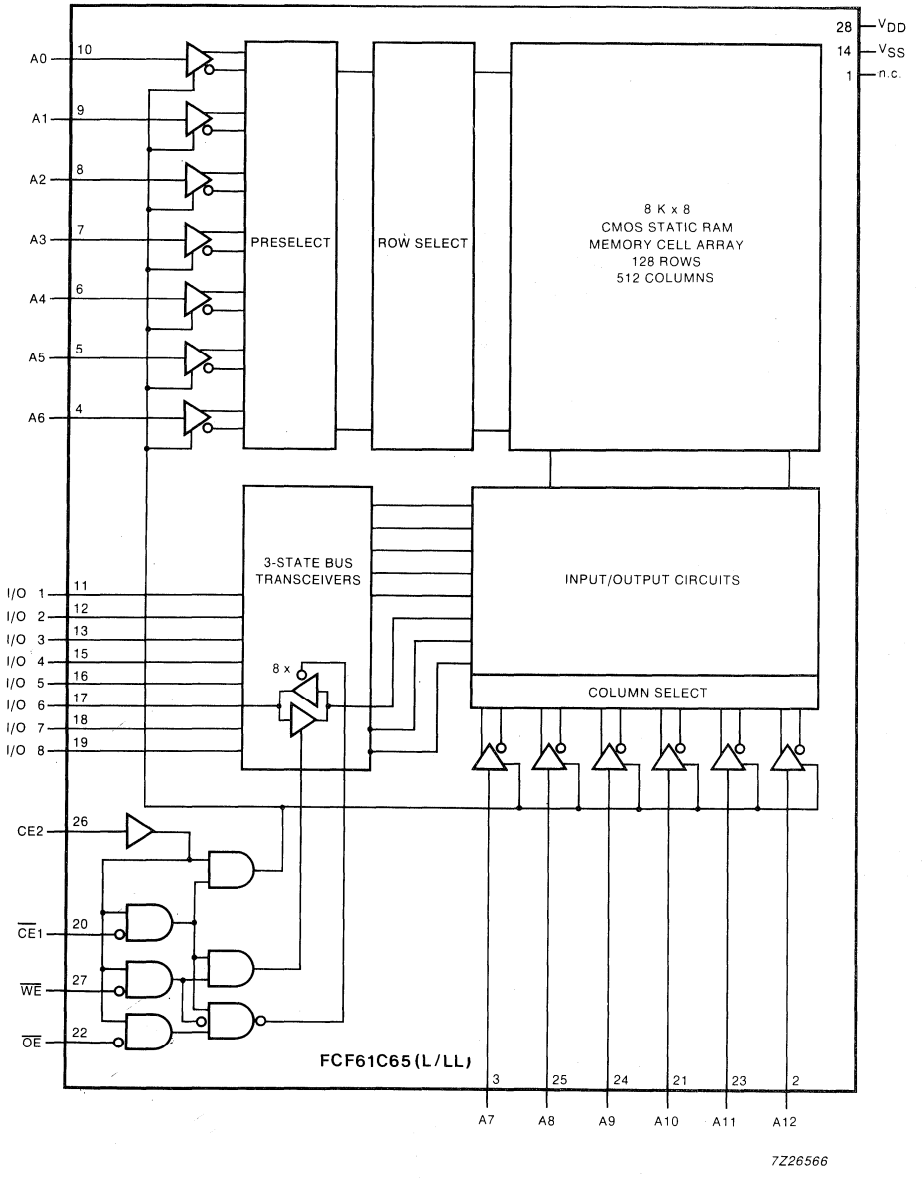


Fig.1 Block diagram.

NE5592
Video Amplifier

Product Specification

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

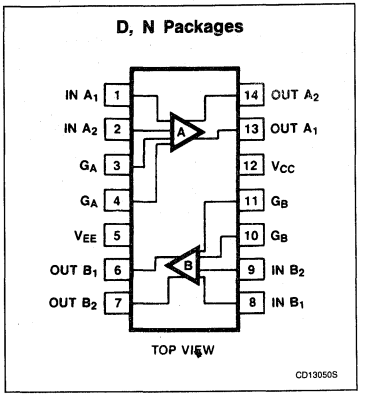
FEATURES

- **110MHz unity gain bandwidth**
- **Adjustable gain from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

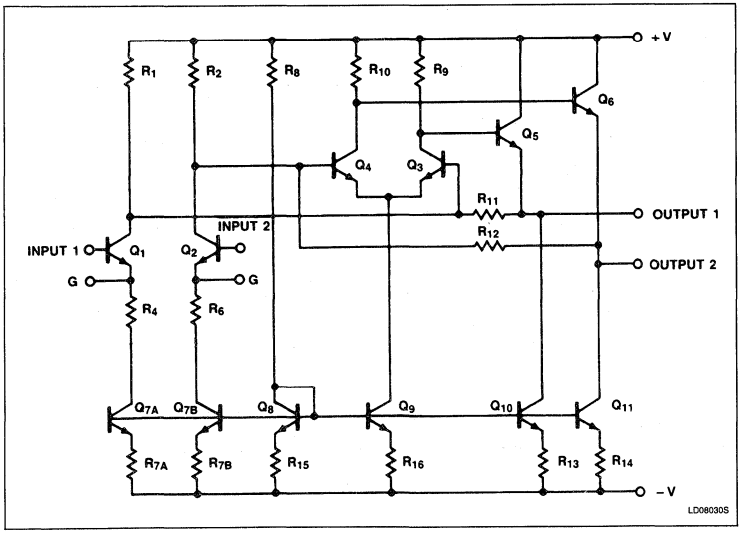
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1] D package N package	 1.03 1.48	 W W

NOTE:
1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	μA
I_{BIAS}	Input bias current			5	20	μA
	Input noise voltage	BW 1kHz to 10MHz		4		$nV/\sqrt{Hz}$
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $V_{CM} \pm 1V$, $f = 5MHz$	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50	85		dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$	65	70		dB
V_{OS}	Output offset voltage gain select pins open	$R_L = \infty$ $R_L = \infty$		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$		35	44	mA

DC ELECTRICAL CHARACTERISTICS $V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$, unless otherwise specified. Recommended operating supply voltage is $V_S = \pm 6.0V$, and gain select pins are connected together.

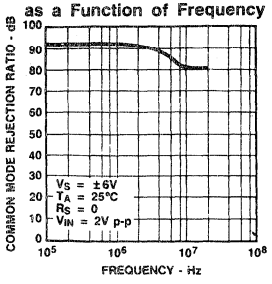
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$ $R_S = \phi$	55			dB
PSRR	Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
	Channel separation	$V_{OUT} = 1V_{P-P}$; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		70		dB
V_{OS}	Output offset voltage gain select pins connected together	$R_L = \infty$			1.5	V
	gain select pins open	$R_L = \infty$			1.0	V
V_{OUT}	Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
I_{CC}	Power supply current (total for both sides)	$R_L = \infty$			47	mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	$V_{OUT} = 1V_{P-P}$		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$		7.5	12	ns

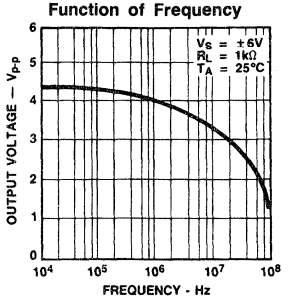
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



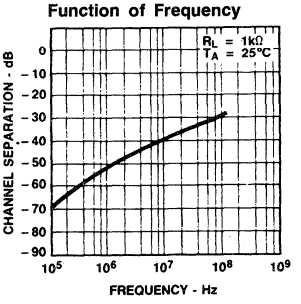
OP18580S

Output Voltage Swing as a Function of Frequency



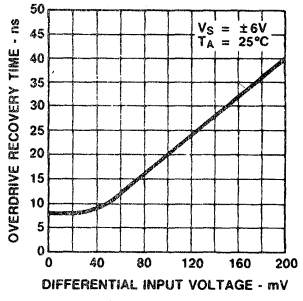
OP18590S

Channel Separation as a Function of Frequency



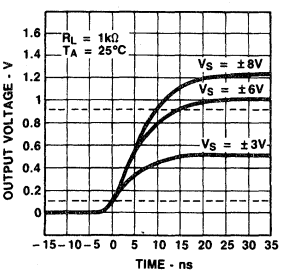
OP18600S

Differential Overdrive Recovery Time



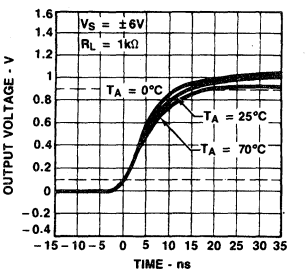
OP18610S

Pulse Response as a Function of Supply Voltage



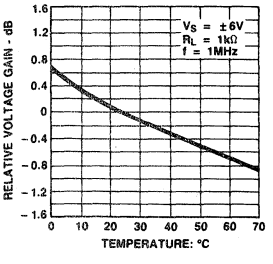
OP18620S

Pulse Response as a Function of Temperature



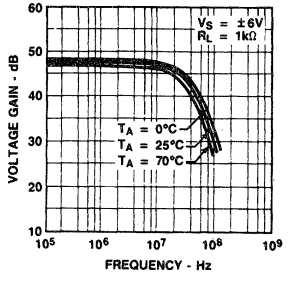
OP18630S

Voltage Gain as a Function of Temperature



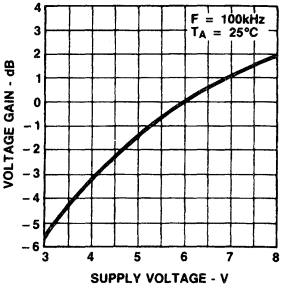
OP18640S

Gain vs Frequency as a Function of Temperature



OP18650S

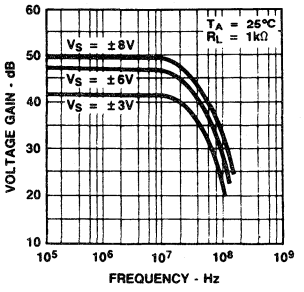
Voltage Gain as a Function of Supply Voltage



OP18660S

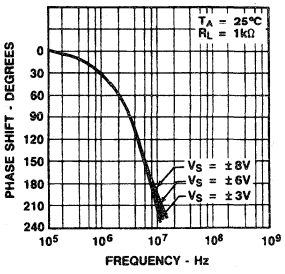
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



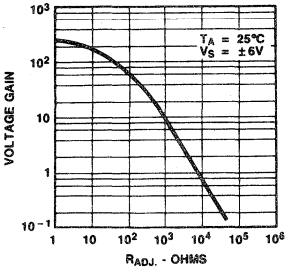
OP18670S

Phase vs Frequency as a Function of Supply Voltage



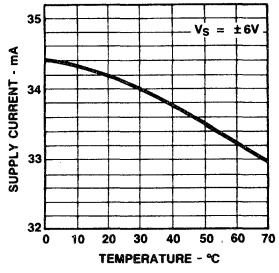
OP18660S

Voltage Gain as a Function of R_{ADJ}



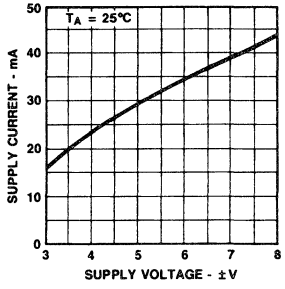
OP18690S

Supply Current as a Function of Temperature



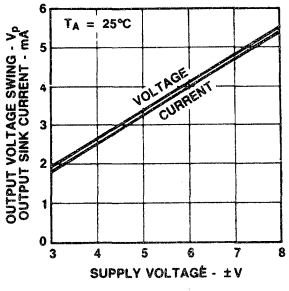
OP18700S

Supply Current as a Function of Supply Voltage



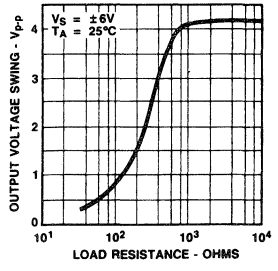
OP18710S

Output Voltage Swing and Sink Current as a Function of Supply Voltage



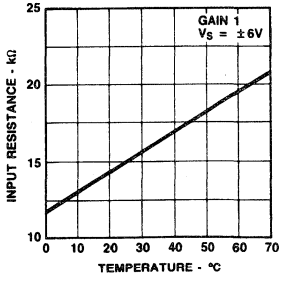
OP18720S

Output Voltage Swing as a Function of Load Resistance



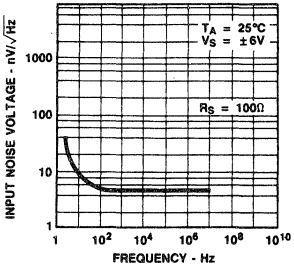
OP18730S

Input Resistance as a Function of Temperature



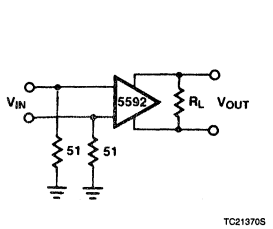
OP18740S

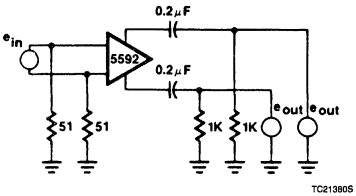
Input Noise Voltage as a Function of Frequency

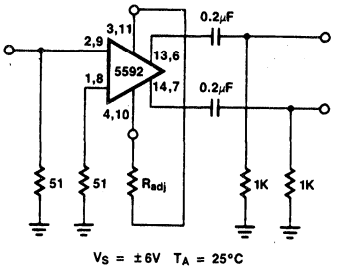


OP18750S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.







NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

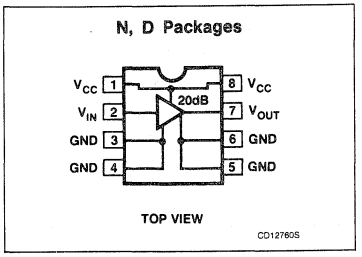
No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **Bandwidth (min.)**
  200 MHz, ± 0.5dB
  350 MHz, − 3dB
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  Z_O = 75Ω (Z_O = 50Ω)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION



APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

ORDERING INFORMATION

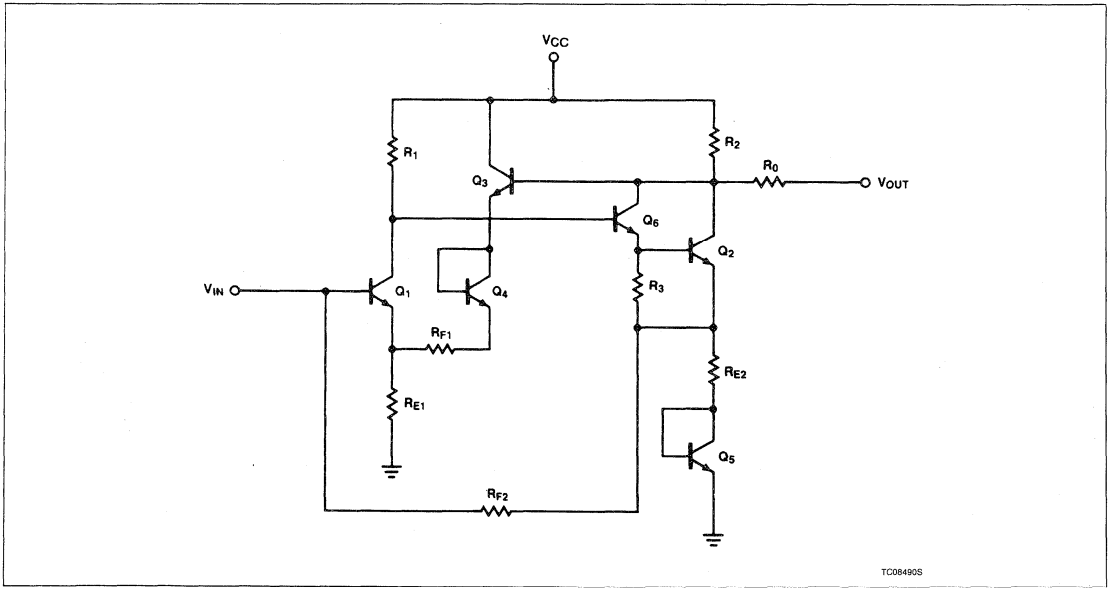
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 −40 to +85	 °C °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f = 100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

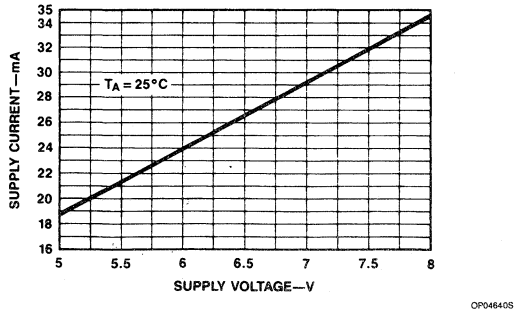


Figure 1. Supply Current vs Supply Voltage

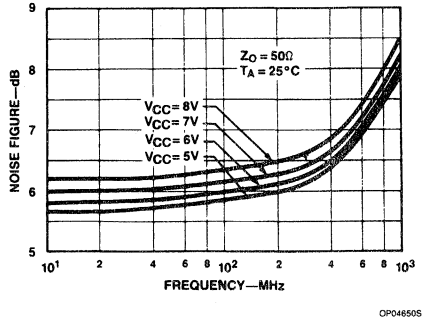


Figure 2. Noise Figure vs Frequency

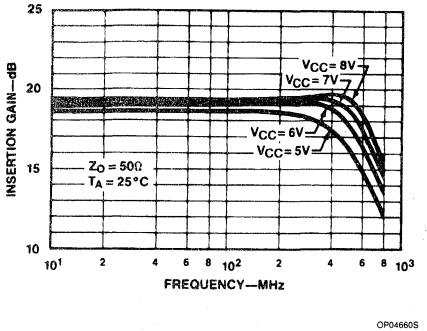


Figure 3. Insertion Gain vs Frequency (S_{21})

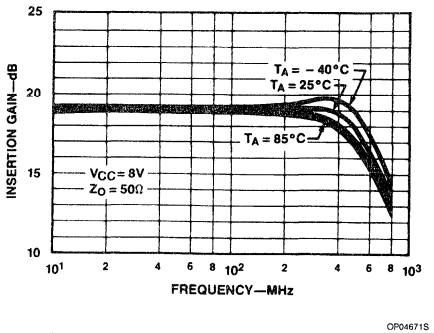


Figure 4. Insertion Gain vs Frequency (S_{21})

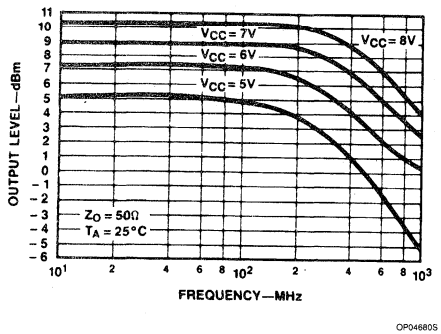


Figure 5. Saturated Output Power vs Frequency

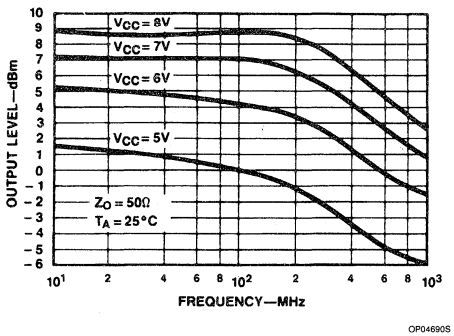


Figure 6. 1dB Gain Compression vs Frequency

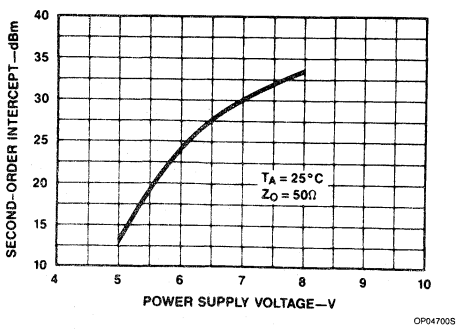


Figure 7. Second-Order Output Intercept vs Supply Voltage

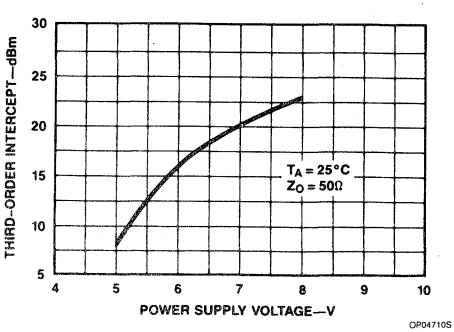


Figure 8. Third-Order Intercept vs Supply Voltage

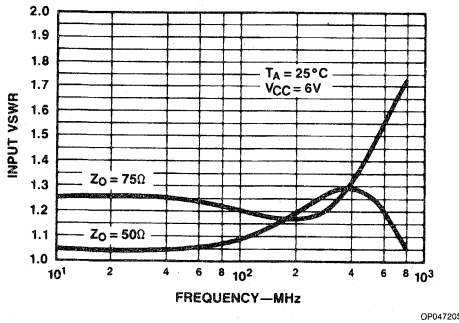


Figure 9. Input VSWR vs Frequency

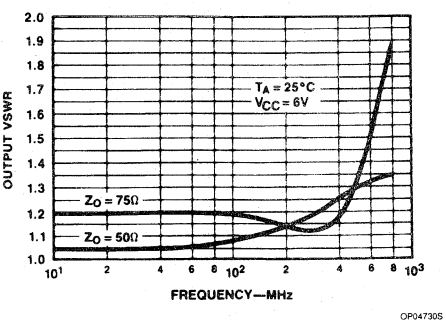


Figure 10. Output VSWR vs Frequency

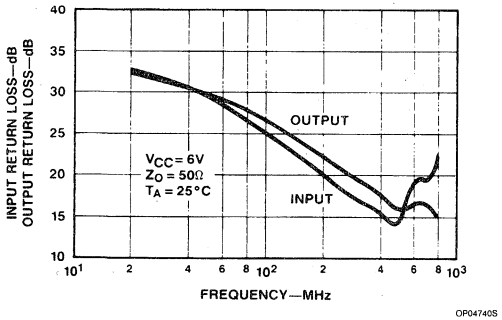


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

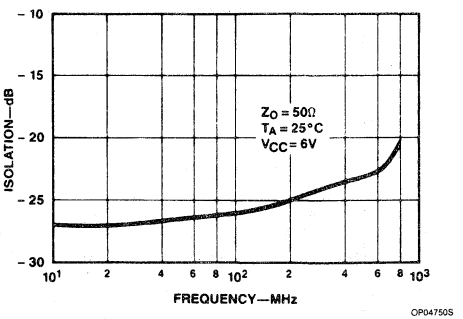


Figure 12. Isolation vs Frequency (S_{12})

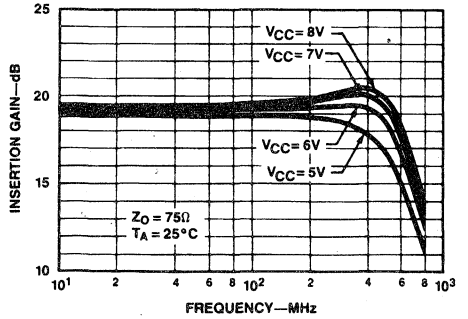


Figure 13. Insertion Gain vs Frequency (S_{21})

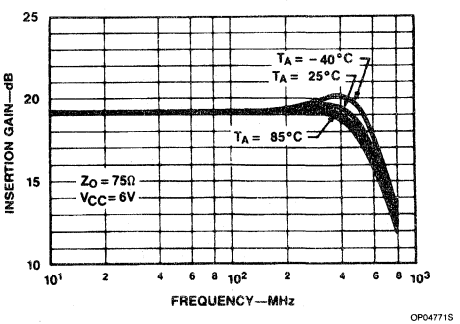


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left\{1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} \text{dB} \quad (2)$$

where $I_{C1} = 5.5\text{mA}$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26\text{mV}$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\,R_{E1} \quad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8\text{V}$, $I_{C1} = 5\text{mA}$ and $I_{C3} = 7\text{mA}$ (currents rated at $V_{CC} = 6\text{V}$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6\text{V}$, $R_2 = 225\Omega$, $I_{C2} = 7\text{mA}$ and $I_{C6} = 5\text{mA}$.

From here, it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

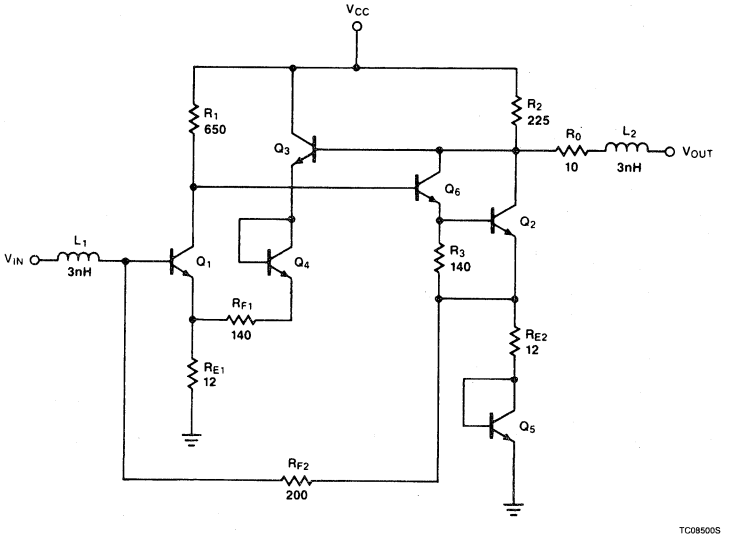


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

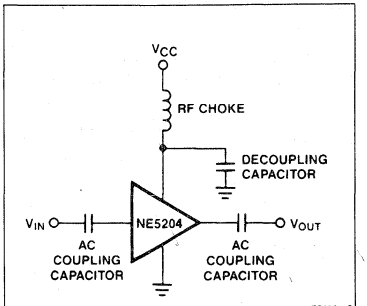
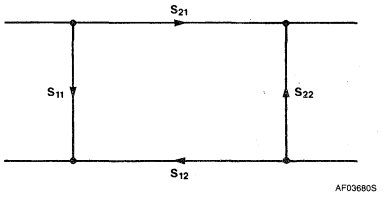


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE5204 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

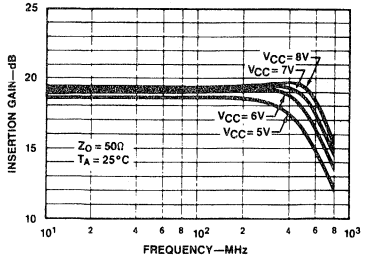
$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

AF03690S

b.

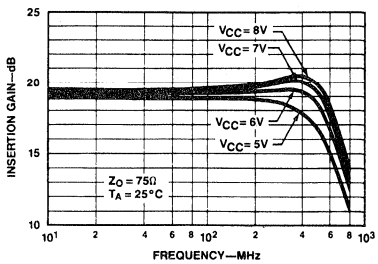
Figure 17

50Ω System

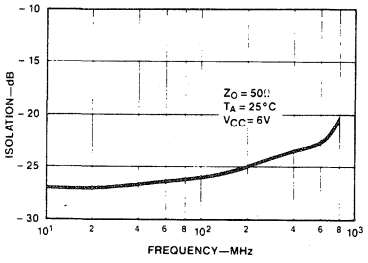


a. Insertion Gain vs Frequency (S_{21})

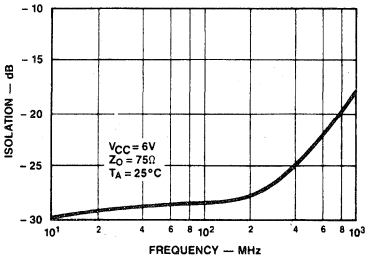
75Ω System



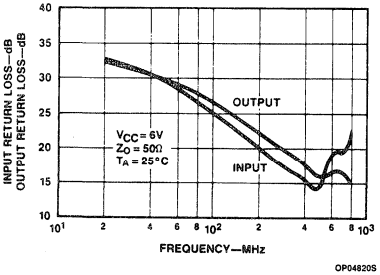
b. Insertion Gain vs Frequency (S_{21})



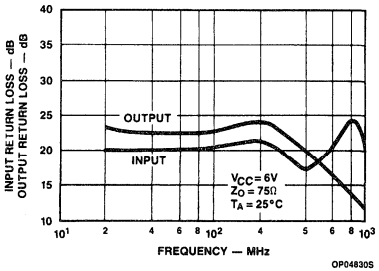
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency



f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

Actual S-parameter measurements, using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B), are shown in Figure 18.

Values for Figure 20 are measured and specified in the data sheet to ease adaptation and comparison of the NE5204 to other high-frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5204

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE5204}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain
V_I = Insertion Voltage Gain

Measured value for the NE5204 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10\text{Log}\ |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20\text{Log}\ S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing-wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = S_{11}dB
$S_{11}\text{dB} = 20\text{Log}\ |S_{11}|$

OUTPUT RETURN LOSS = S_{22}dB
$S_{22}\text{dB} = 20\text{Log}\ |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to non-linearities in the amplifier, an indication of the point of transition between small-signal operation and the large-signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

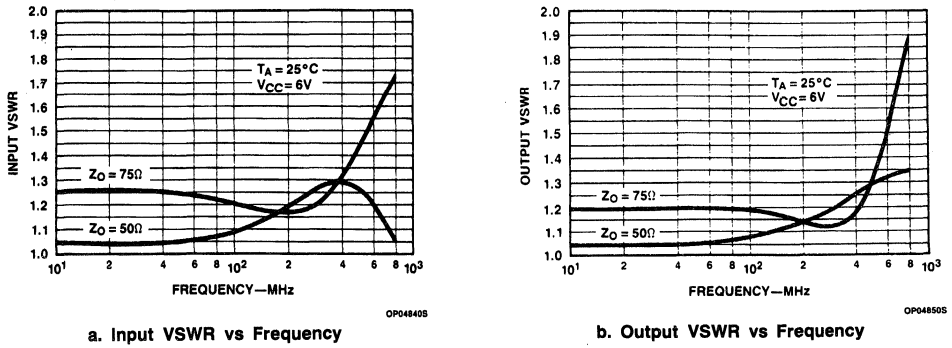
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second-order IMR is equal to the difference between the second-order intercept and the fundamental output level. The third-order IMR is equal to twice the difference between the third-order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second- and third-order output intercepts in dBm, and IMR_2 and IMR_3 are the second- and third- order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small-signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point, the intermodulation products no longer follow the straight-line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be care-



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ful, however, not to select levels which are too low, because the test equipment may not be able to recover the signal from the noise. For the NE5204, an output level of –10.5dBm was chosen with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers*; by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985, published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, HP App Note 154, 1972.

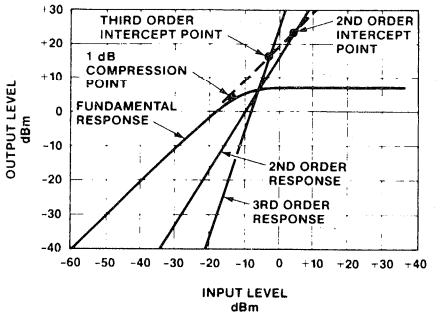


Figure 20

Document	853-1453
ECN No.	00223
Date of Issue	August 20, 1990
Status	Product Specification
RF Communications	

NE/SA5209

Wideband variable gain amplifier

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

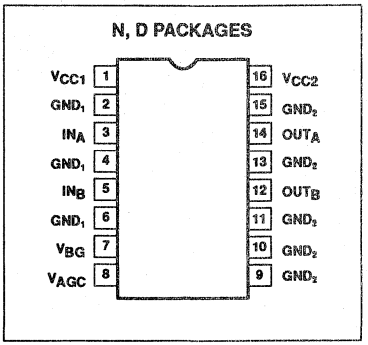
FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi–purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	–40 to +85°C	SA5209D
16-Pin Plastic DIP	–40 to +85°C	SA5209N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	–0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTES:
3.Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
16-Pin DIP: θ_{JA} = 85°C/W
16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 –40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 –40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50µA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	Ω
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	V
PSRR	Output offset supply rejection ratio		20	45		dB
	(output referred)	Over temperature[1]	15			dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	V

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0V<V_{AGC}<1.3V$		–0.7	–6	µA
		Over temperature[1]			–10	µA

NOTES:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	–3dB bandwidth		600	850		MHz
		Over temperature[1]	500			MHz
GF	Gain flatness	DC – 500MHz		±0.4		dB
		Over temperature[1]		±0.6		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended)	$R_L = 50Ω$		400		mV_{P-P}
	for linear operation[2]	$R_L = 1kΩ$		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	$R_S = 50Ω$, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		–60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50Ω$		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	–3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		–3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		–10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:
1."Over Temperature Range" testing is as follows:
NE is 0 to +70°C
SA is –40 to +85°C
At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2.With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With $R_L = 50Ω$, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 – 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

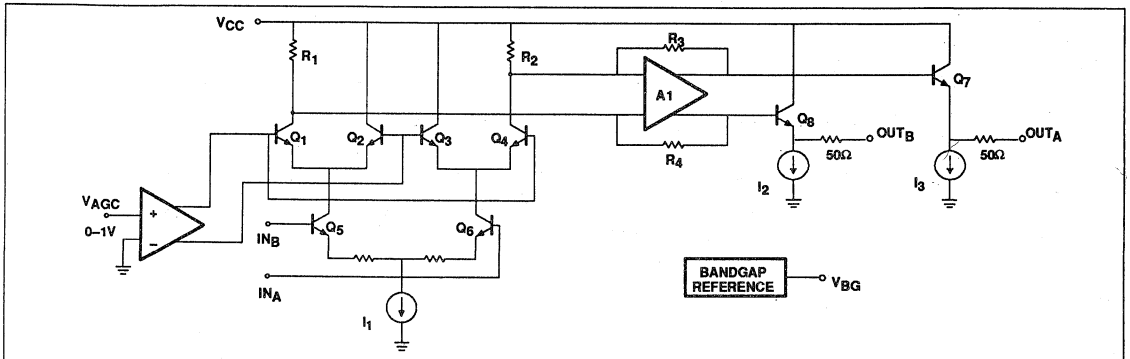


Figure 1. Equivalent Schematic of the VGA

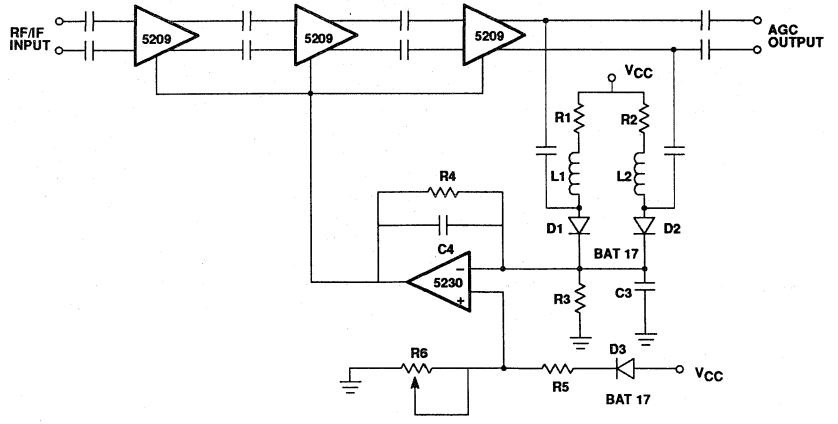


Figure 2. AGC Configuration Using Cascaded NE5209s

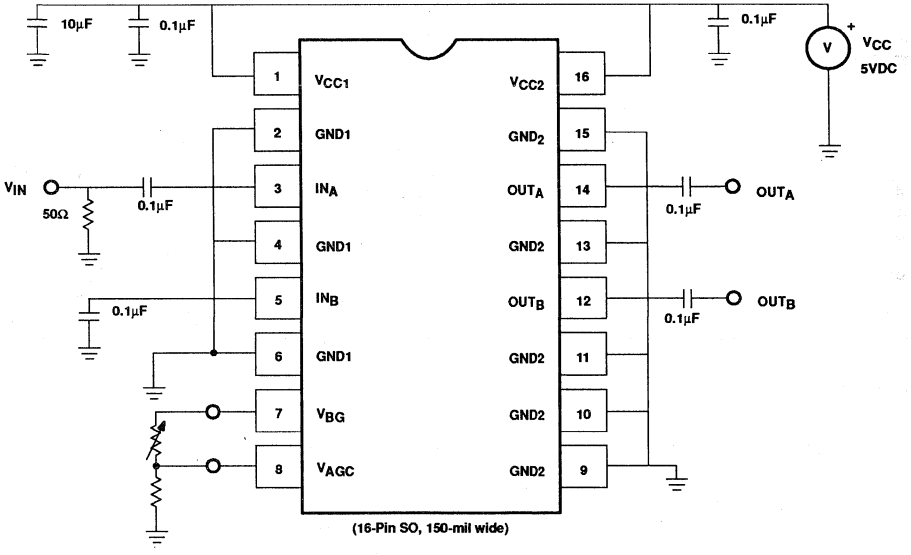
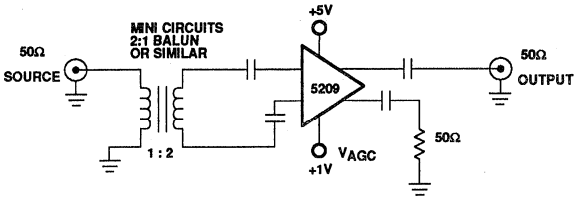
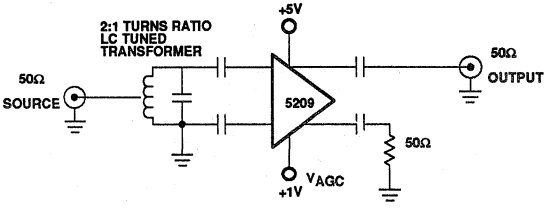


Figure 3. VGA AC Evaluation Board



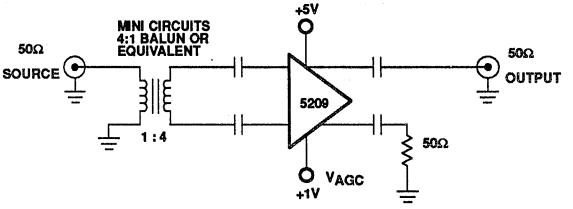
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



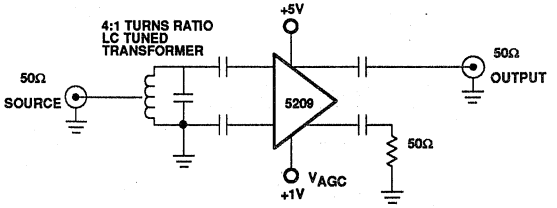
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



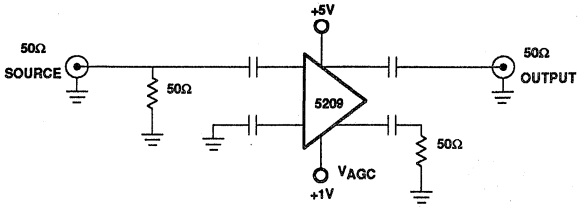
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration

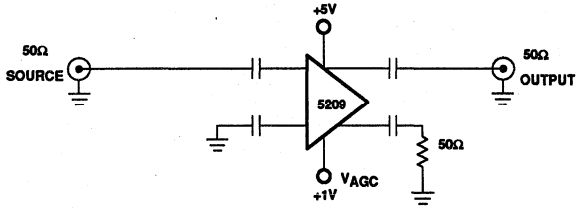


Figure 9 Unterminated Configuration

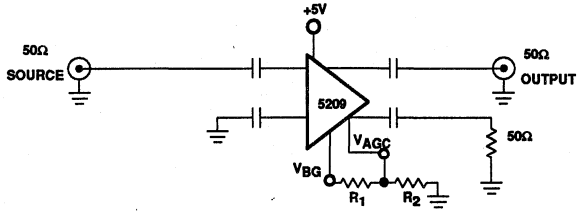


Figure 10. User-Programmable Fixed Gain Block

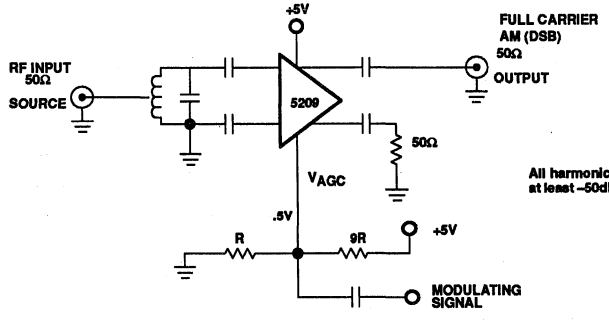


Figure 11. AM Modulator

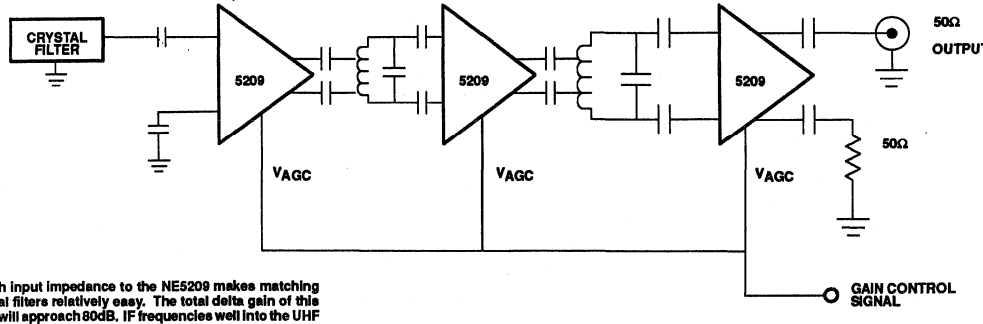


Figure 12. Receiver AGC IF Chain

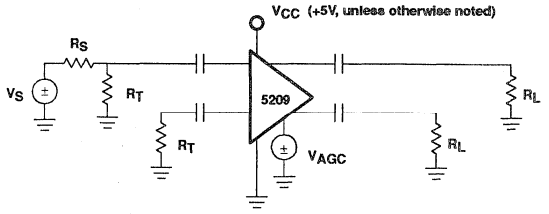


Figure 13. Test Set-up 1 (Used for all Graphs)

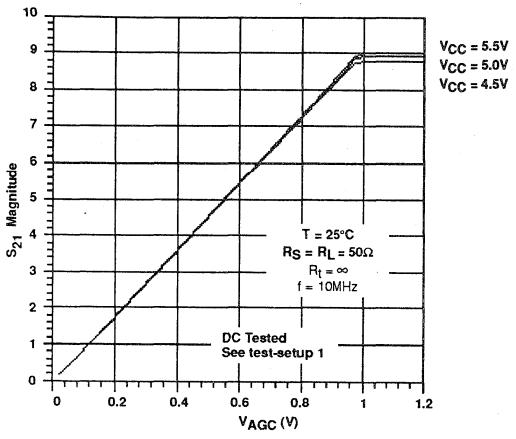


Figure 14. Gain vs V_{AGC} and V_{CC}

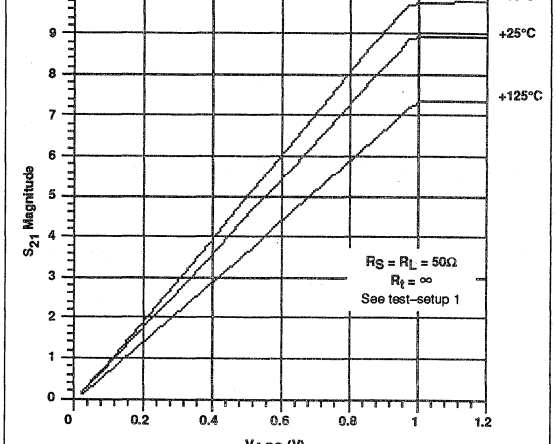


Figure 15. Insertion Gain vs V_{AGC} and Temperature

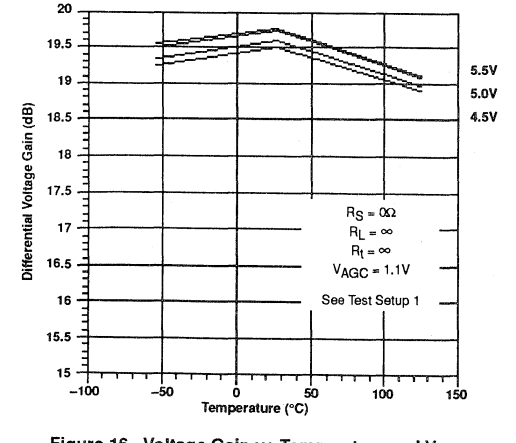


Figure 16. Voltage Gain vs Temperature and V_{CC}

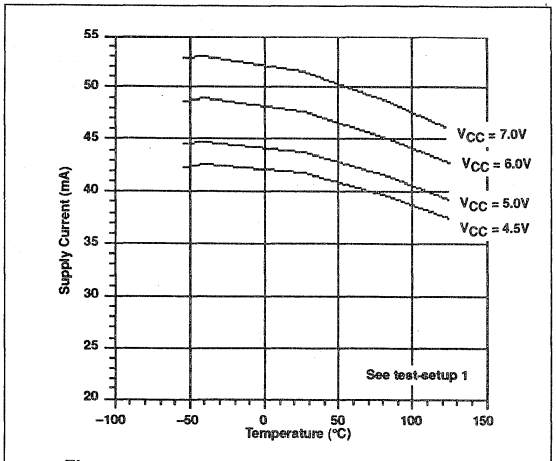


Figure 17. Supply Current vs Temperature and V_{CC}

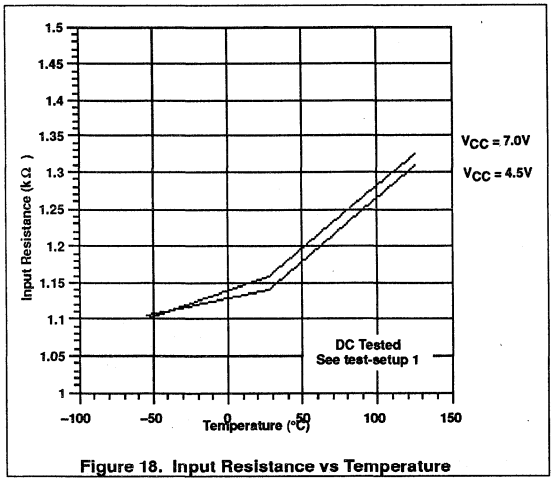


Figure 18. Input Resistance vs Temperature

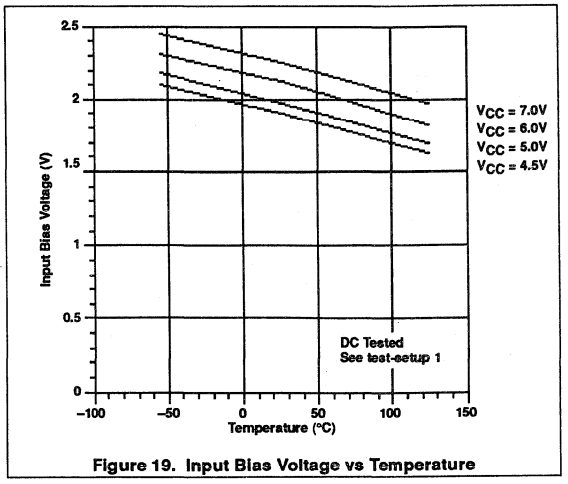


Figure 19. Input Bias Voltage vs Temperature

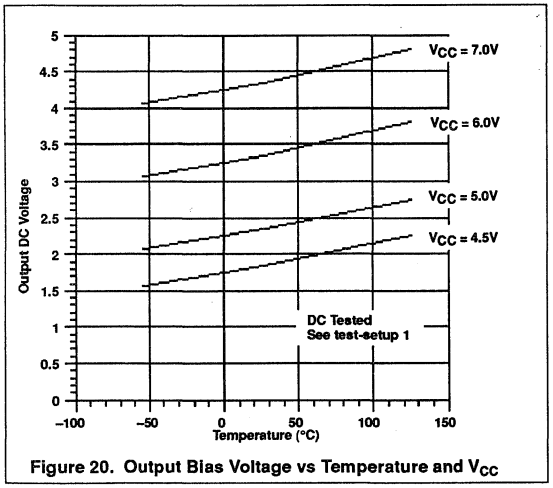


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

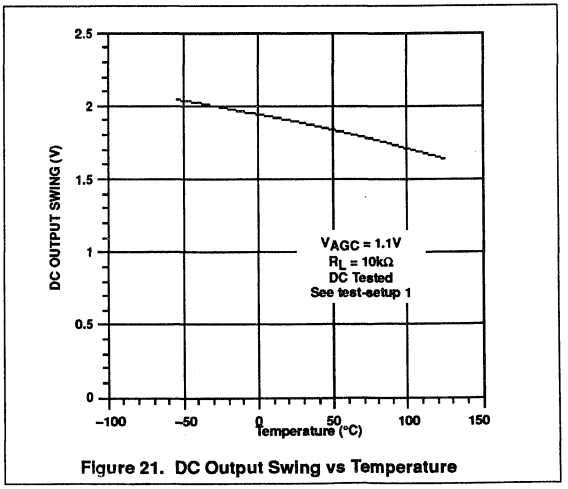


Figure 21. DC Output Swing vs Temperature

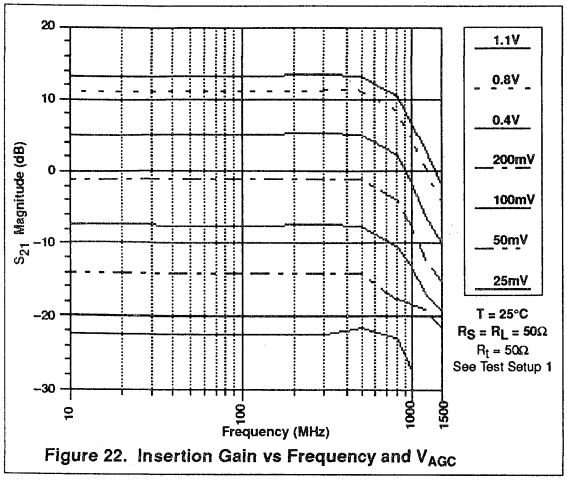


Figure 22. Insertion Gain vs Frequency and V_{AGC}

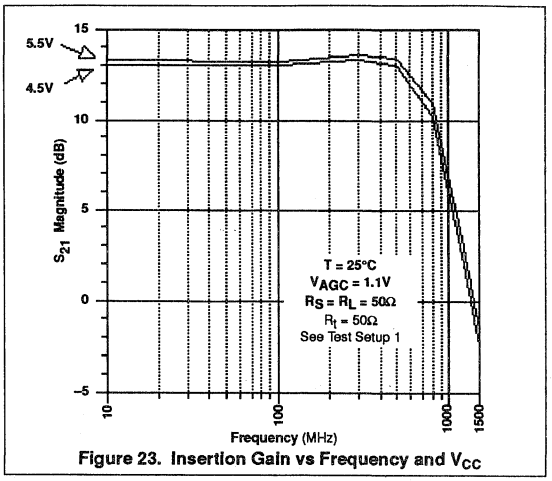


Figure 23. Insertion Gain vs Frequency and V_{CC}

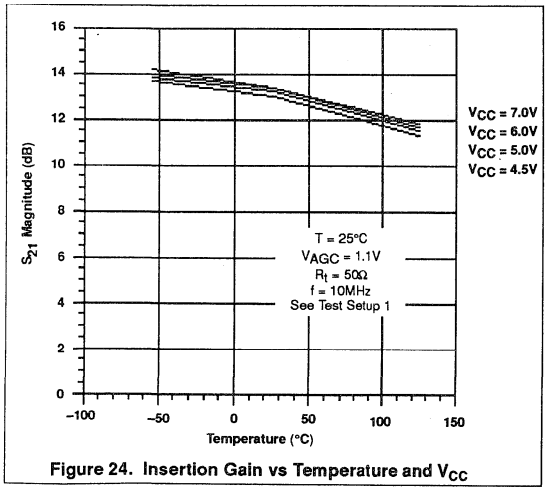


Figure 24. Insertion Gain vs Temperature and V_{CC}

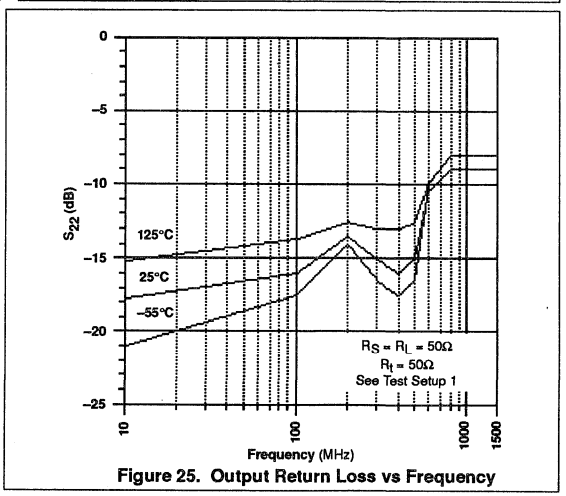


Figure 25. Output Return Loss vs Frequency

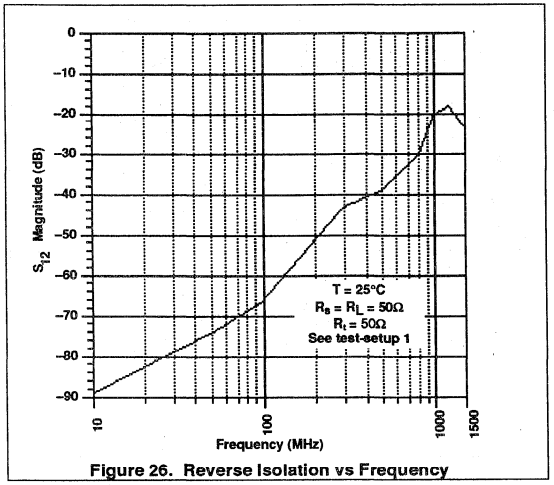


Figure 26. Reverse Isolation vs Frequency

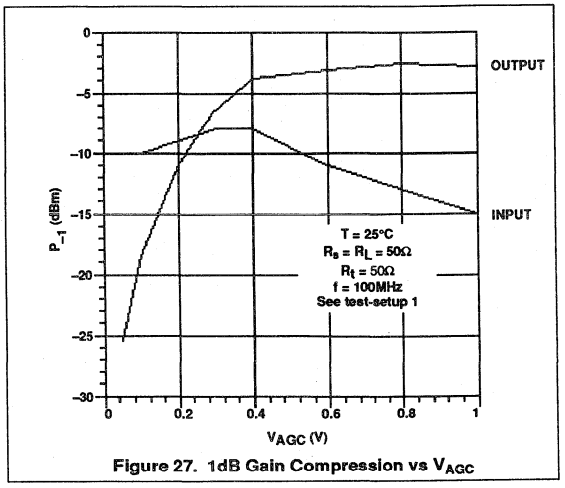


Figure 27. 1dB Gain Compression vs V_{AGC}

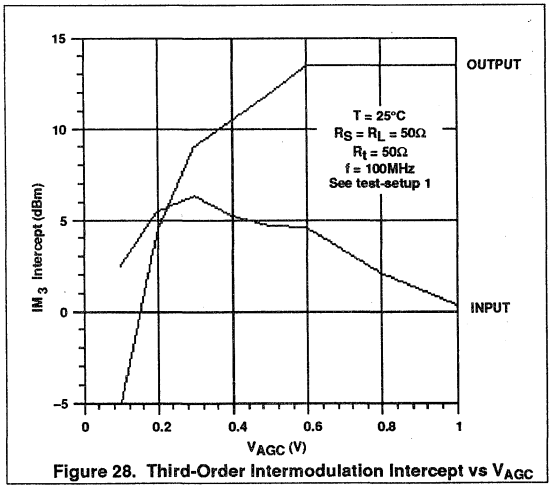


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

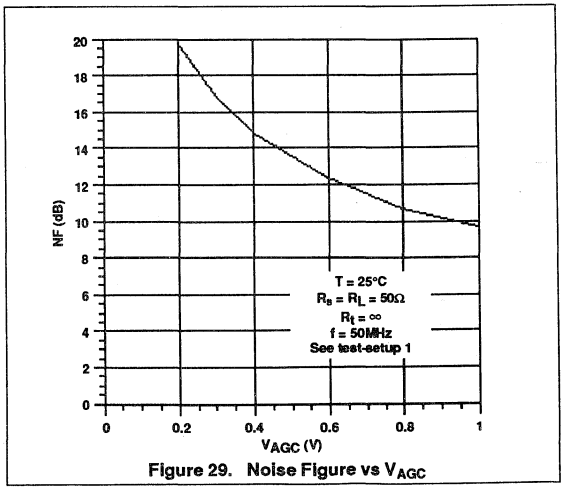


Figure 29. Noise Figure vs V_{AGC}

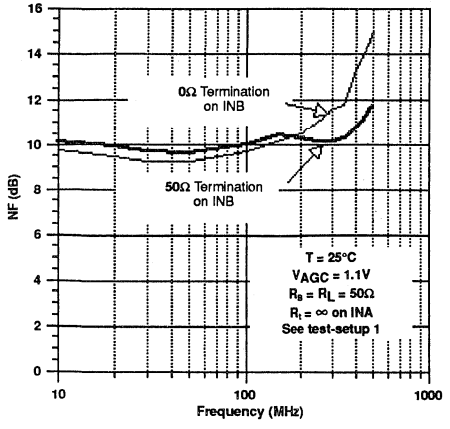


Figure 30. Noise Figure vs Frequency

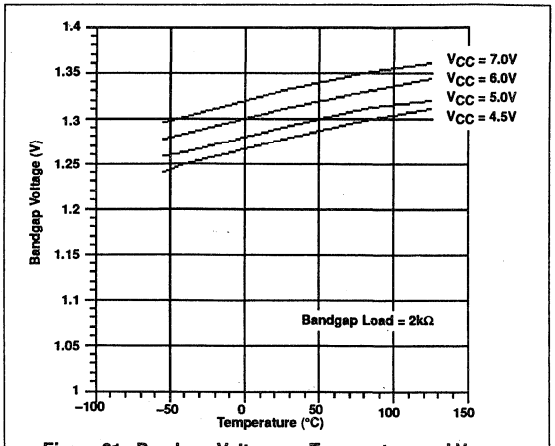


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

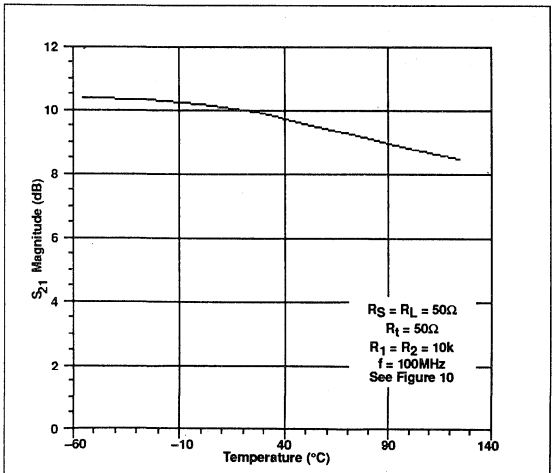
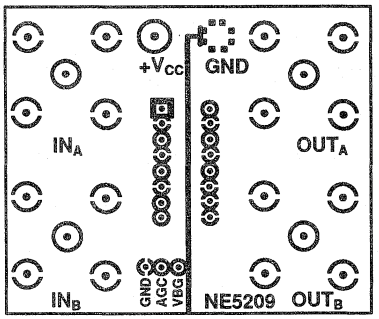
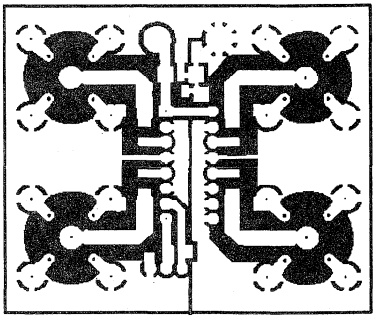


Figure 32. Fixed Gain vs Temperature

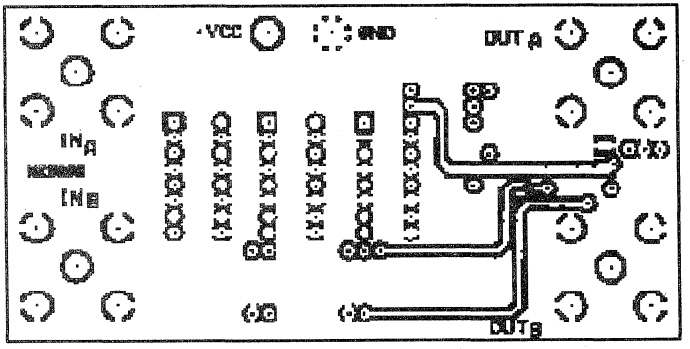


TOP VIEW - COMPONENT SIDE

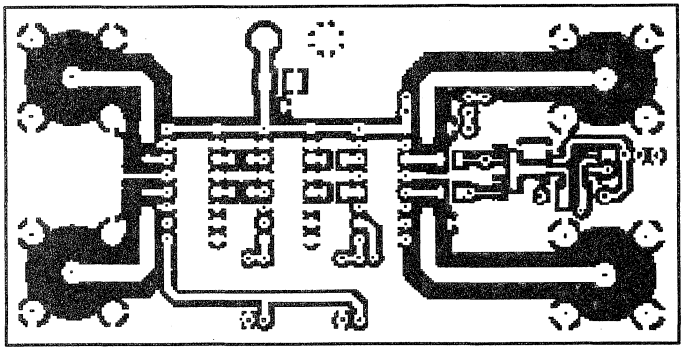


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout

NE/SA/SE592
Video Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

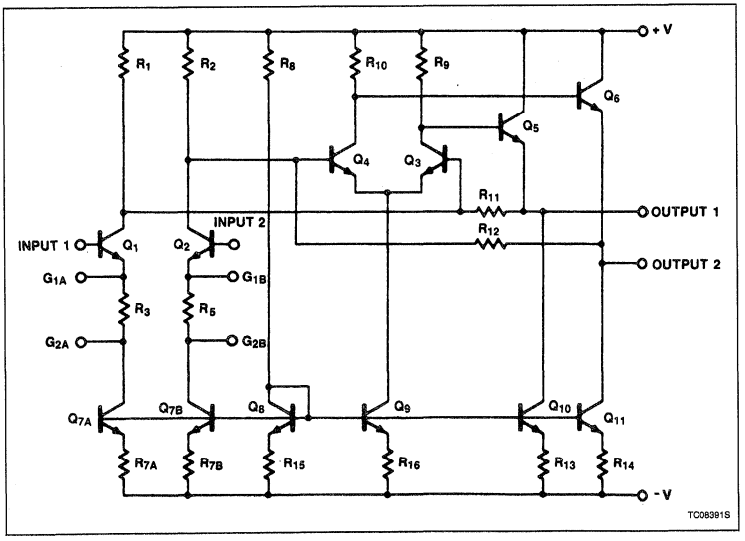
FEATURES

- **120MHz unity gain bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**
- **MIL-STD processing available**

APPLICATIONS

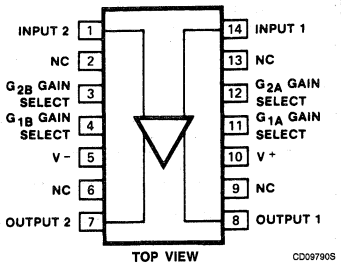
- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

EQUIVALENT CIRCUIT

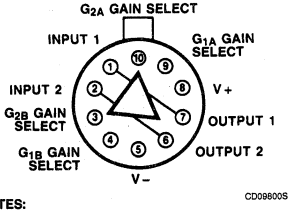


PIN CONFIGURATIONS

D, F, N Packages

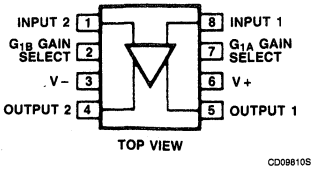


H Package*



NOTES:
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

D, F, N, Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin Plastic DIP	−40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	−40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	−55°C to +125°C	SE592H

NOTE:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range		
	SE592	−40 to +85	°C
	NE592	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1]		
	F-14 package	1.17	W
	F-8 package	0.79	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	H package	0.83	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTE:
1. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		kΩ
	Gain 2[2, 4]		10	30		20	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	60	86		60	86		dB
	Gain 2[4]	$V_{CM} \pm 1V$, $f = 5MHz$		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leq T_A \leq 70°C$ for NE592; $-40°C \leq T_A \leq 85°C$ for SA592, $-55°C \leq T_A \leq 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part								
	Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$	250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 2[2, 4]		8.0			8.0			kΩ
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

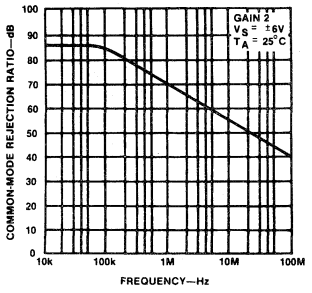
$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay								
	Gain 1[1]	$V_{OUT} = 1V_{P-P}$		7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

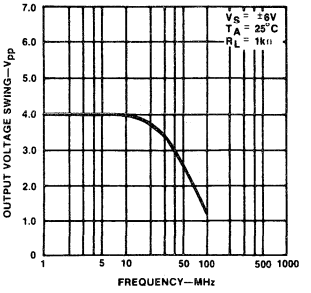
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency



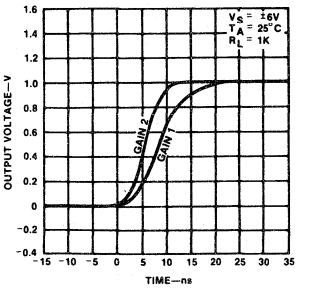
OP04421S

Output Voltage Swing as a Function of Frequency



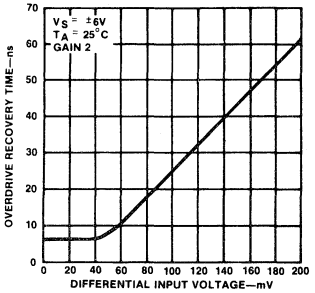
OP04430S

Pulse Response



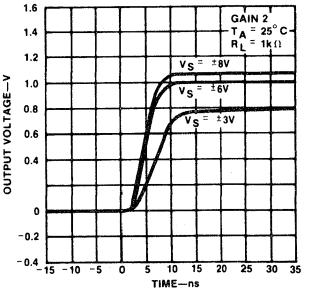
OP04440S

Differential Overdrive Recovery Time



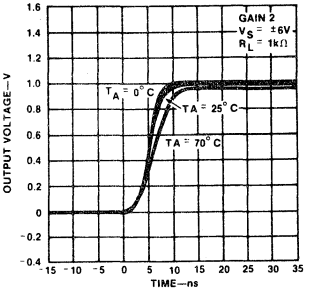
OP04450S

Pulse Response as a Function of Supply Voltage



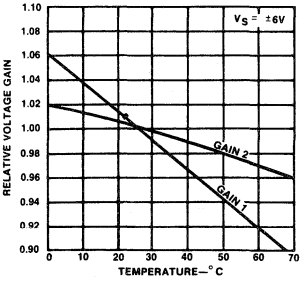
OP04460S

Pulse Response as a Function of Temperature



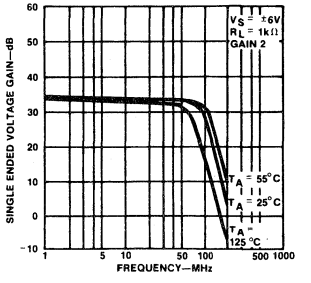
OP04470S

Voltage Gain as a Function of Temperature



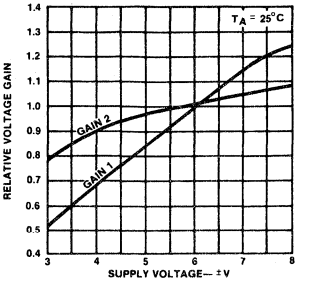
OP04480S

Gain vs Frequency as a Function of Temperature



OP04490S

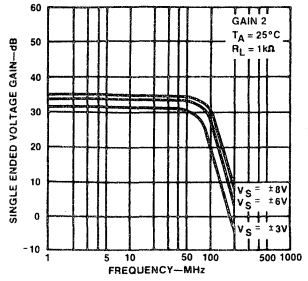
Voltage Gain as a Function of Supply Voltage



OP04500S

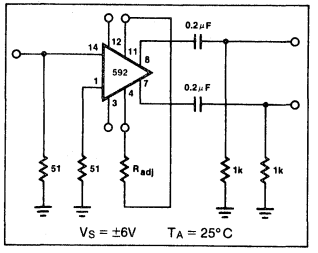
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage



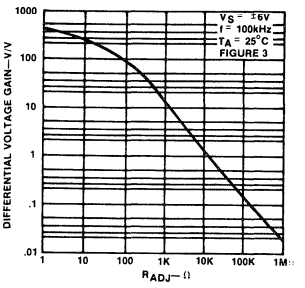
OP04510S

Voltage Gain Adjust Circuit



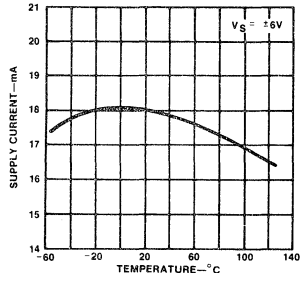
OP04521S

Voltage Gain as a Function of RADJ (Figure 3)



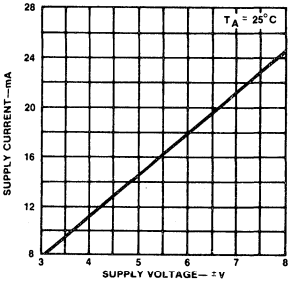
OP04530S

Supply Current as a Function of Temperature



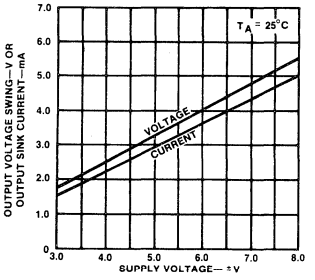
OP04540S

Supply Current as a Function of Supply Voltage



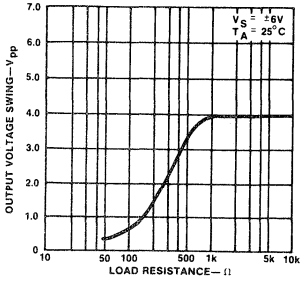
OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage



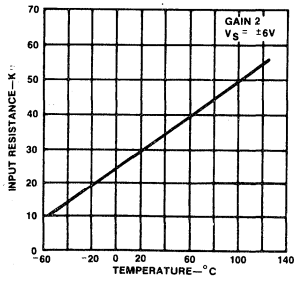
OP04560S

Output Voltage Swing as a Function of Load Resistance



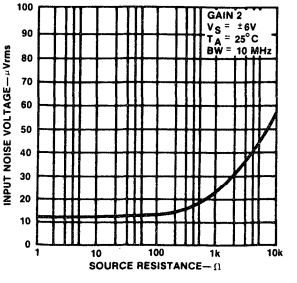
OP04570S

Input Resistance as a Function of Temperature



OP04580S

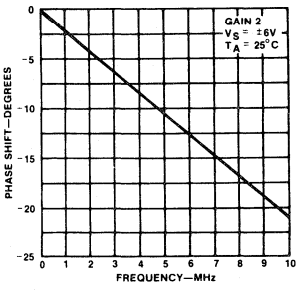
Input Noise Voltage as a Function of Source Resistance



OP04590S

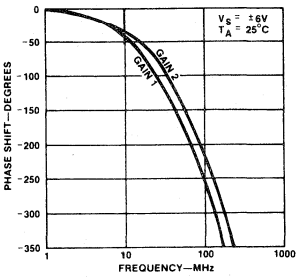
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



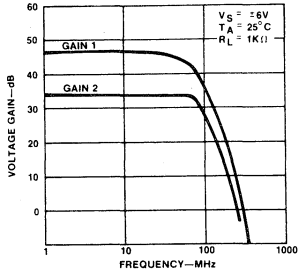
OP04600S

Phase Shift as a Function of Frequency



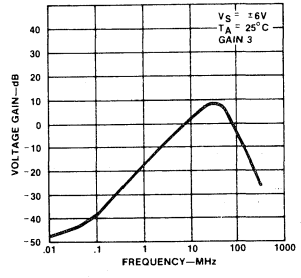
OP04610S

Voltage Gain as a Function of Frequency



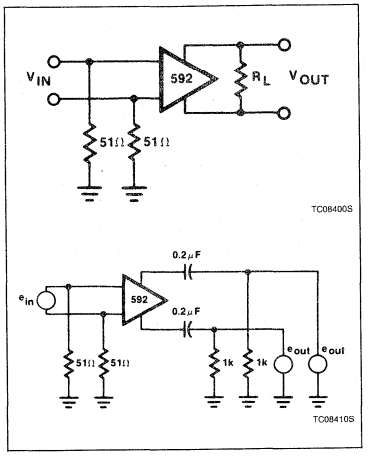
OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

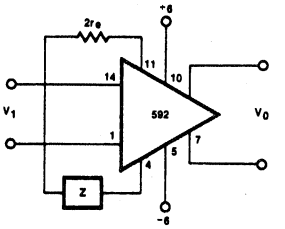


OP04630S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



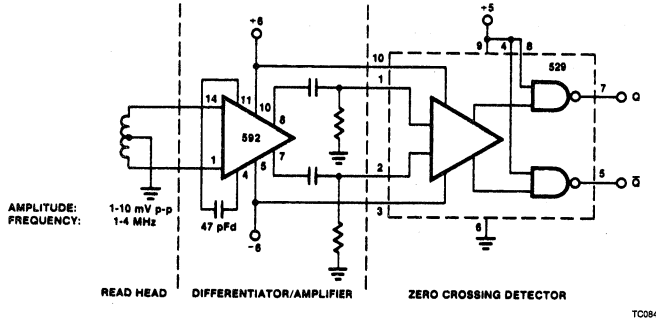
TYPICAL APPLICATIONS



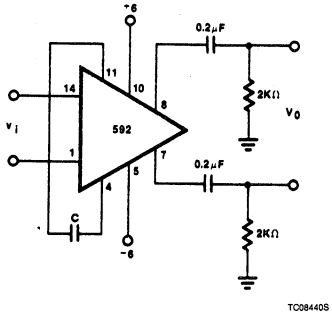
NOTE:

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e} \cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration



Disc/Tape Phase-Modulated Readback Systems

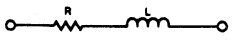
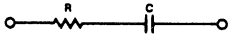
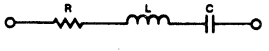
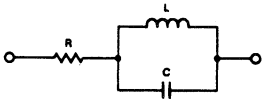


NOTE:
For frequency $F_1 << \frac{1}{2}\pi(32)C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

TC08422S

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES

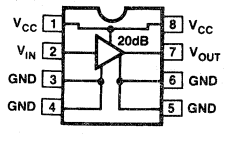
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

PIN CONFIGURATIONS

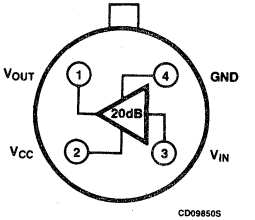
N, FE, D Packages



TOP VIEW

CD12760S

EC Package



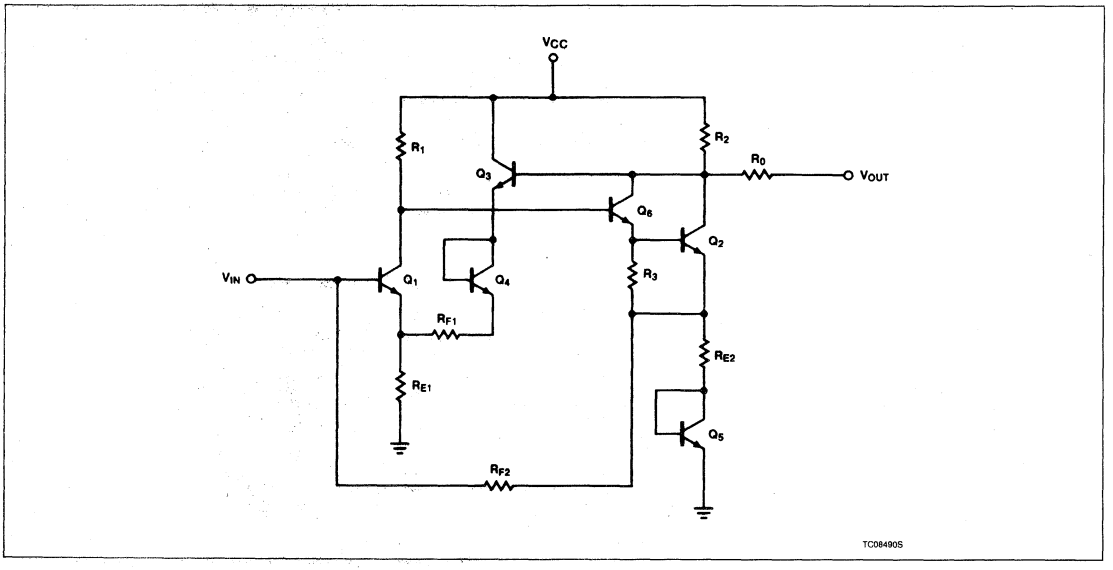
CD09850S

NOTE:
Tab denotes Pin 1.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
4-Pin Metal can	0 to +70°C	NE5205EC
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	-40°C to +85°C	SA5205D
8-Pin Plastic DIP	-40°C to +85°C	SA5205N
8-Pin Cerdip	-40°C to +85°C	SA5205FE
8-Pin Cerdip	-55°C to +125°C	SE5205FE
8-Pin Plastic DIP	-55°C to +125°C	SE5205N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	−40 to +85	°C
	SE grade	−55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[1, 2]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	EC package	1250	mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, $Z_S = Z_L = Z_O = 50\Omega$ and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	±0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	±0.5dB EC					500		MHz
f_{MAX}	Bandwidth	±0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
f_{MAX}	Bandwidth	-3dB EC				600			MHz
f_{MAX}	Bandwidth	-3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+7.0			+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24			+24		dBm

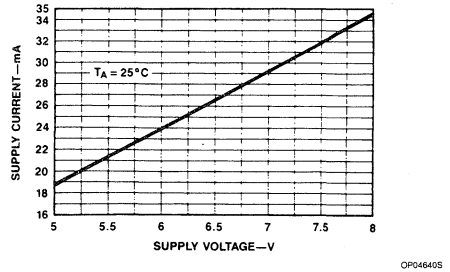


Figure 1. Supply Current vs Supply Voltage

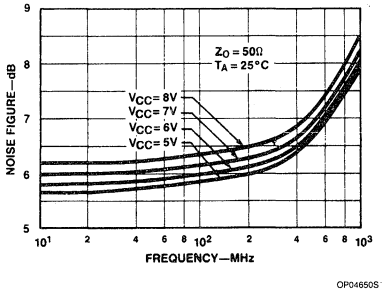


Figure 2. Noise Figure vs Frequency

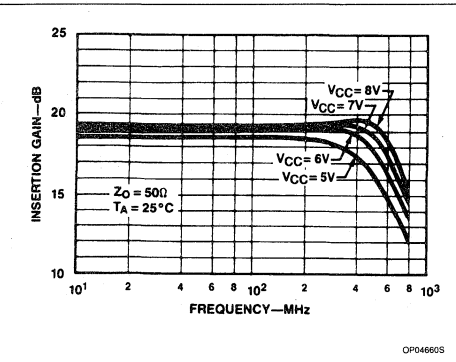


Figure 3. Insertion Gain vs Frequency (S_{21})

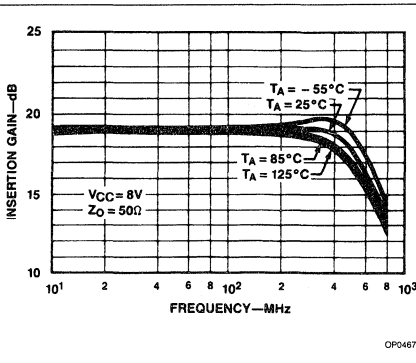


Figure 4. Insertion Gain vs Frequency (S_{21})

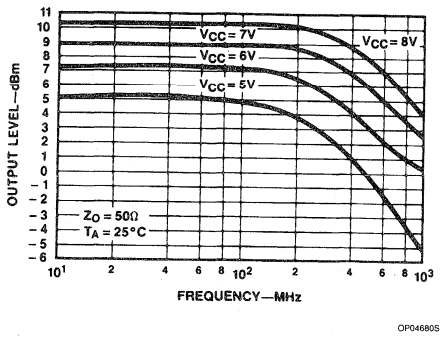


Figure 5. Saturated Output Power vs Frequency

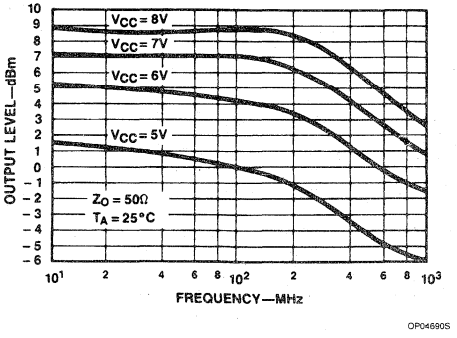


Figure 6. 1dB Gain Compression vs Frequency

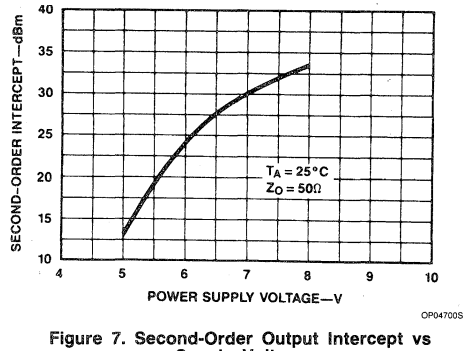


Figure 7. Second-Order Output Intercept vs Supply Voltage

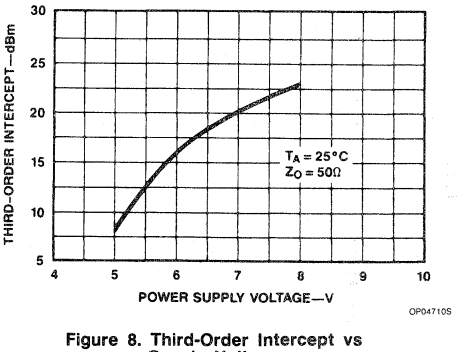


Figure 8. Third-Order Intercept vs Supply Voltage

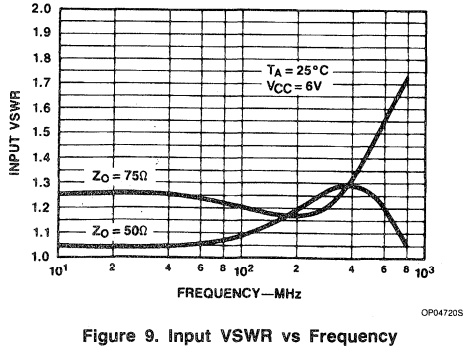


Figure 9. Input VSWR vs Frequency

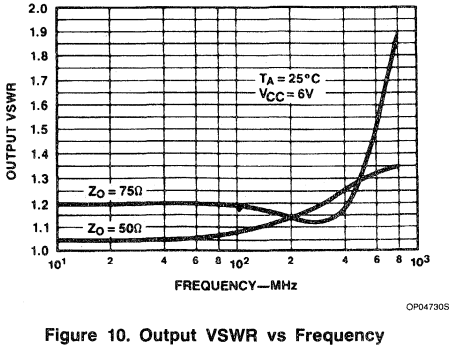


Figure 10. Output VSWR vs Frequency

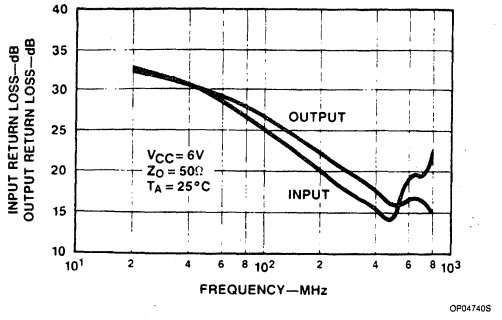


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

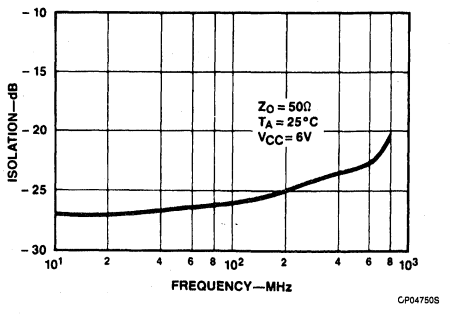


Figure 12. Isolation vs Frequency (S_{12})

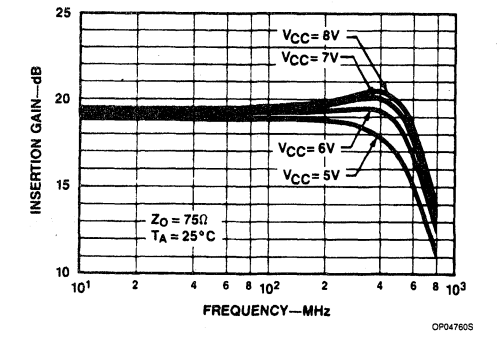


Figure 13. Insertion Gain vs Frequency (S_{21})

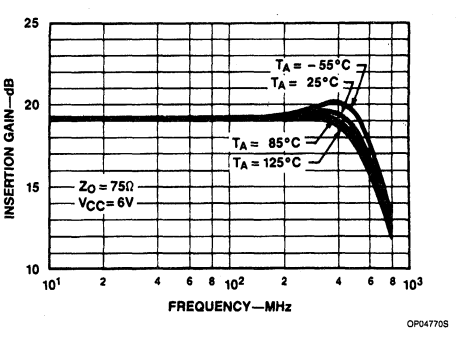


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0} \right\} \text{ dB} \quad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})\ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \quad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.

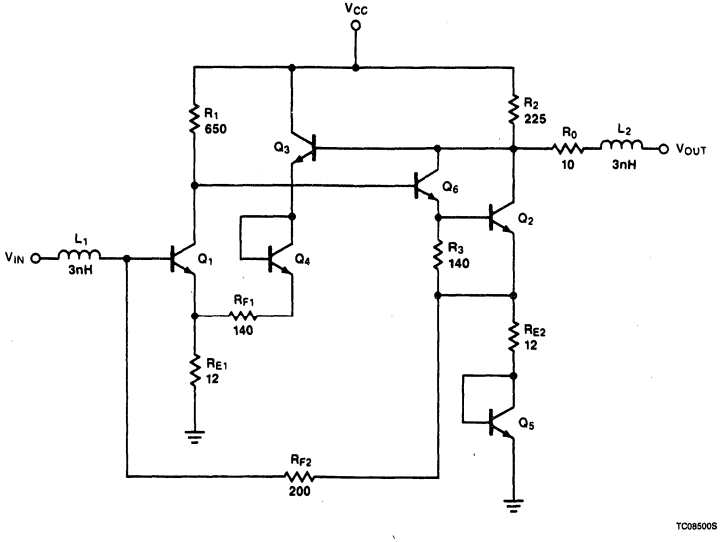


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

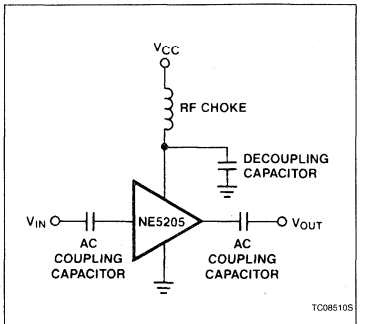


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

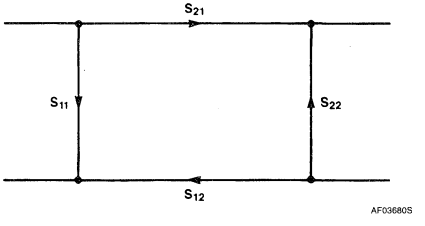


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

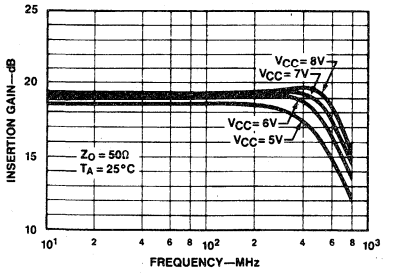
AF03690S

Figure 17b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

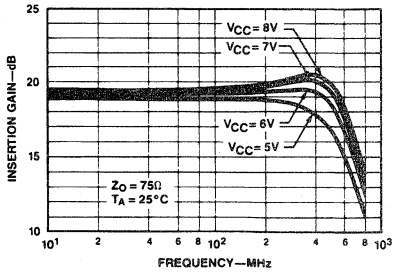
Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

50Ω System

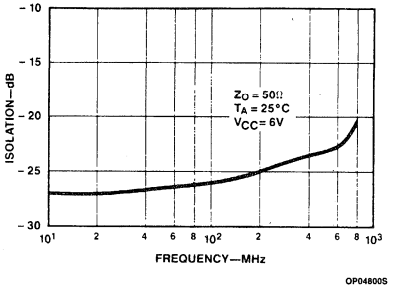


a. Insertion Gain vs Frequency (S_{21})

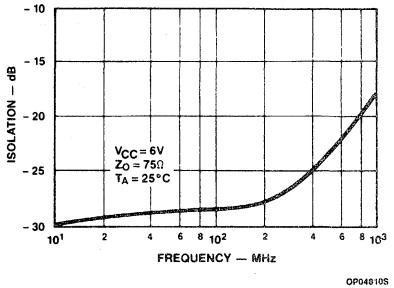
75Ω System



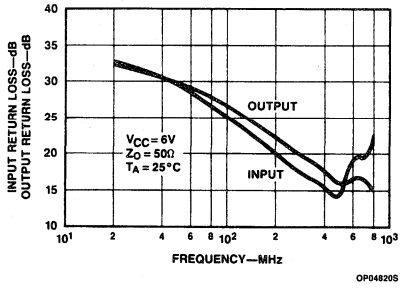
b. Insertion Gain vs Frequency (S_{21})



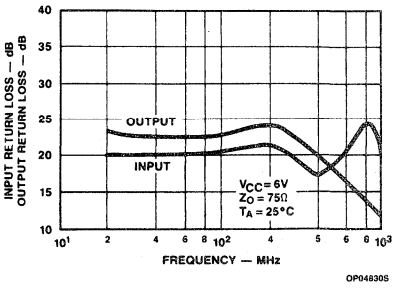
c. Isolation vs Frequency (S_{12})



d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

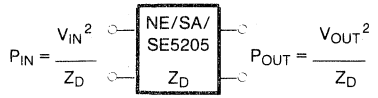


f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

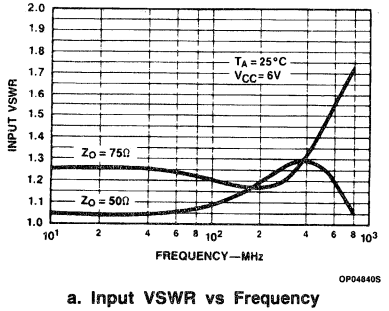
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

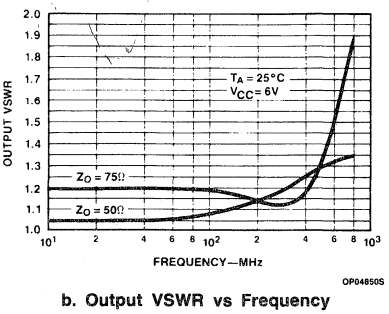
$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

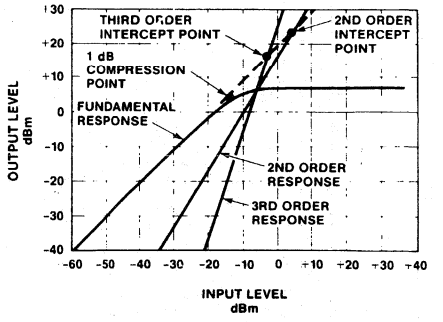


Figure 20

NE/SE5539
High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

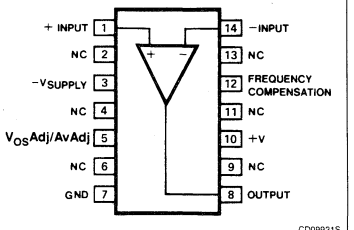
- **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
- **Slew rate: 600/Vμs**
- **A_{VOL}: 52dB typical**
- **Low noise – 4nV/$\sqrt{Hz}$ typical**
- **MIL-STD processing available**

APPLICATIONS

- **High speed datacomm**
- **Video monitors & TV**
- **Satellite communications**
- **Image processing**
- **RF instrumentation & oscillators**
- **Magnetic storage**
- **Military communications**

PIN CONFIGURATION

D, F, N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	−55°C to +125°C	SE5539N
14-Pin Cerdip	−55°C to +125°C	SE5539F

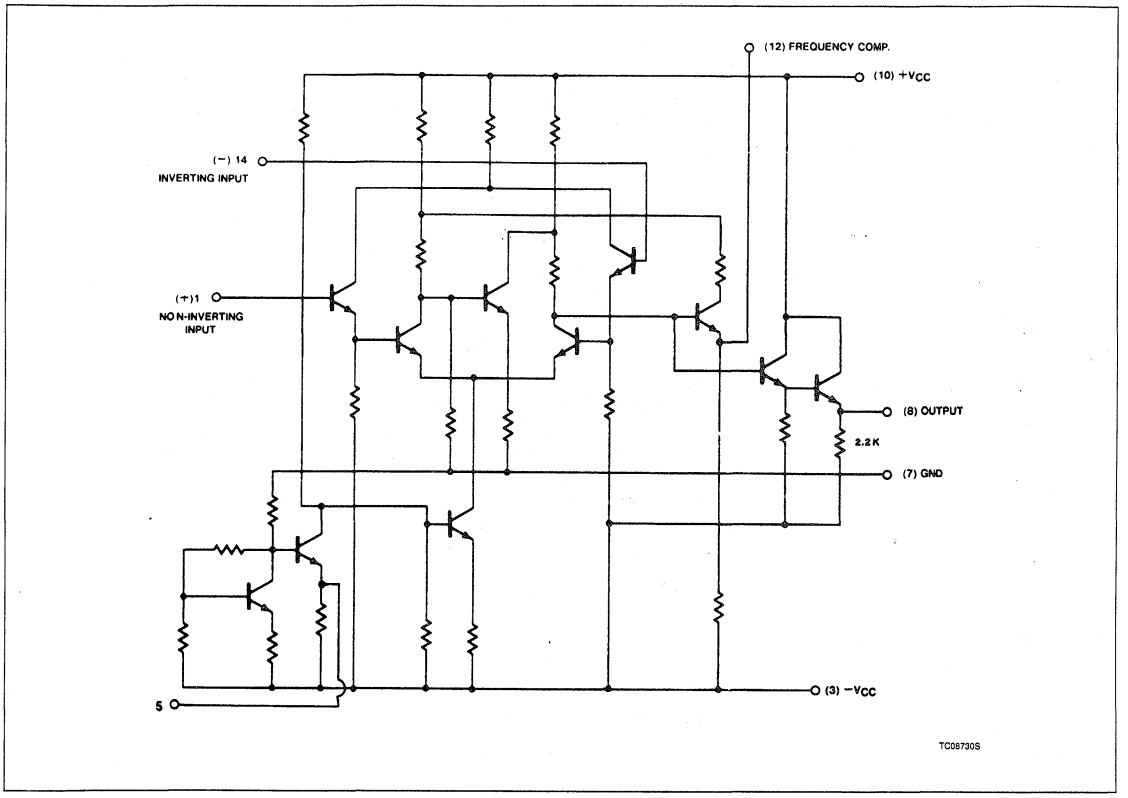
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			NE5539			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$		+Swing				+2.3	+2.7		V
				-Swing				-1.7	-2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0					V
				-Swing	-1.5	-2.1					
			$T_A = 25°C$	+Swing	+2.5	+3.1					V
				-Swing	-2.0	-2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$		Over temp		14	18				mA
				$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$		Over temp		11	15				mA
				$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000				μV/V
				$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$						47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2\Omega$ to GND									dB
				$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND		Over temp	46		60				dB
				$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	μA
				$T_A = 25°C$		0.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				-Swing	-1.1	-1.7		
			$T_A = 25°C$	+Swing	+1.5	+2.0		
				-Swing	-1.4	-1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_O = 0.1\ V_{P-P}$		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega$[1]		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega$[1]		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega$[1]		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega$[1]		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega$[1]		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega$[1]		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		$nV/\sqrt{Hz}$
	Input noise current	1MHz		6			6		$pA/\sqrt{Hz}$

NOTE:
1. External compensation.

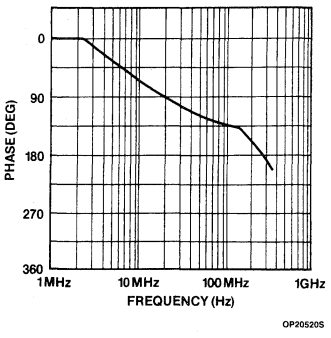
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2$[1]		120		MHz
t_S	Settling time	$A_{CL} = 2$[1]		23		ns
SR	Slew rate	$A_{CL} = 2$[1]		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$[1]		4.5		ns
	Full power response	$A_{CL} = 2$[1]		20		MHz

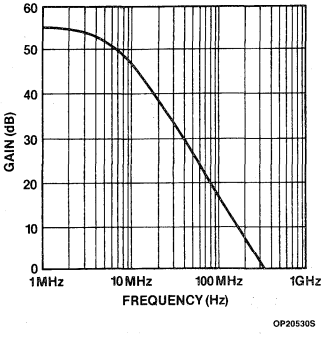
NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

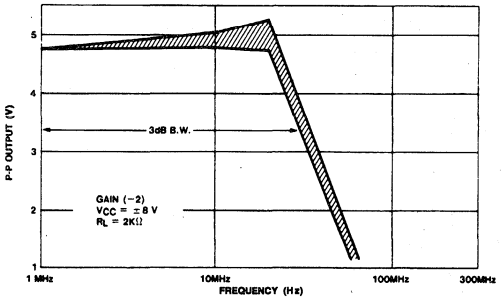


NE5539 Open-Loop Gain



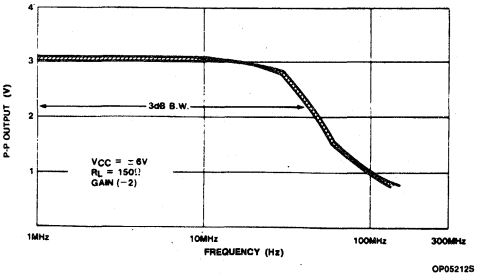
TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)



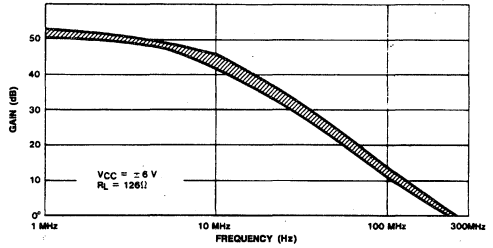
OP05202S

Power Bandwidth (NE)



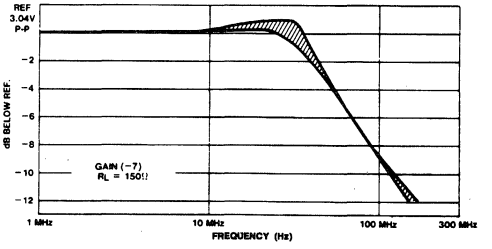
OP05212S

SE5539 Open-Loop Gain vs Frequency



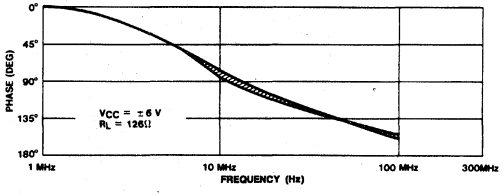
OP05222S

Power Bandwidth

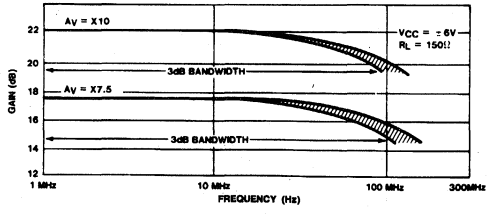


OP05231S

SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency



OP05251S

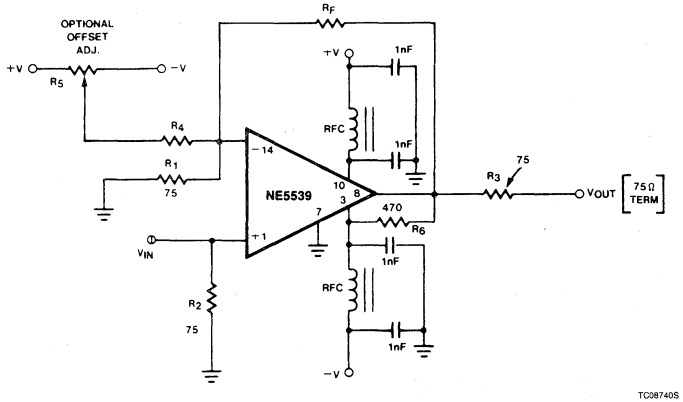
NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

OP05241S

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.

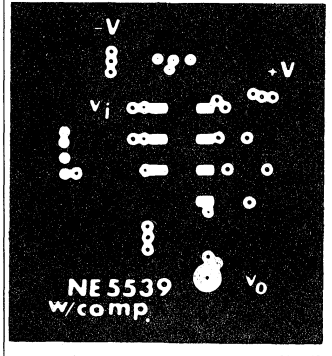


NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

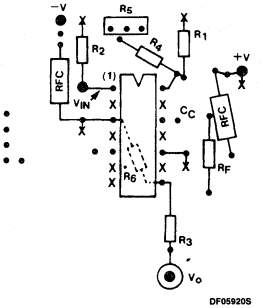
RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



DF05910S

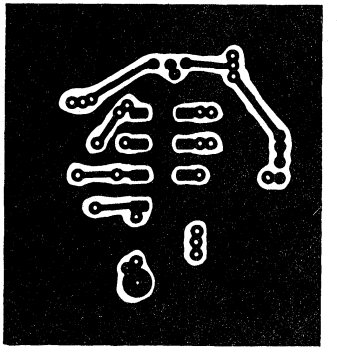
Component Side (Component Layout)



DF05920S

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

Bottom Plane Copper[1]



DF05930S

NOTE:
1. Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

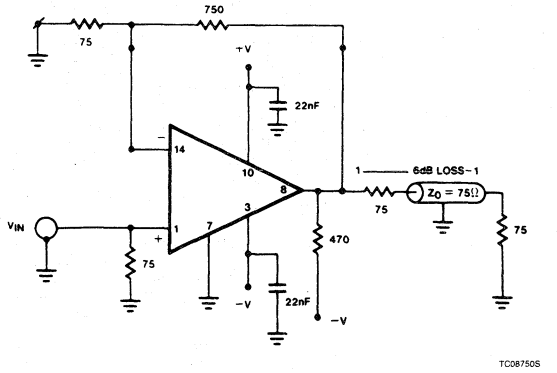


Figure 2. NE5539 Video Amplifier

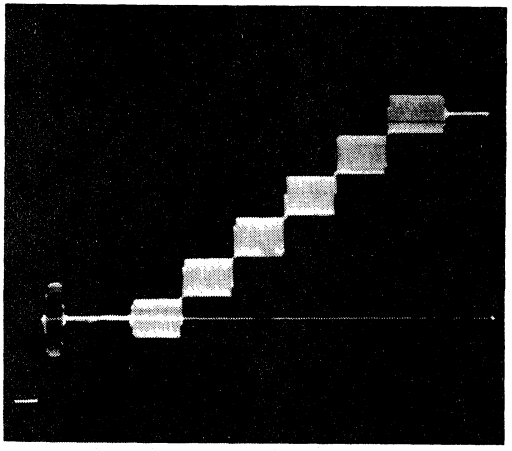


Figure 3. Input Signal

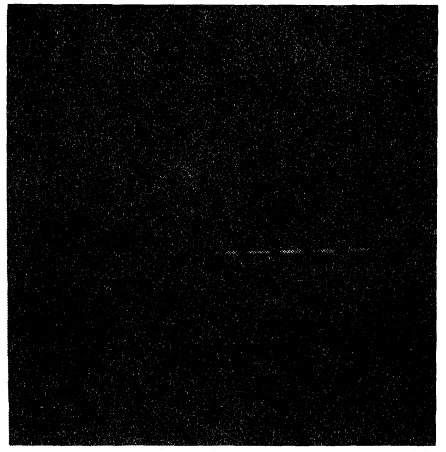


Figure 4. Differential Gain < 0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

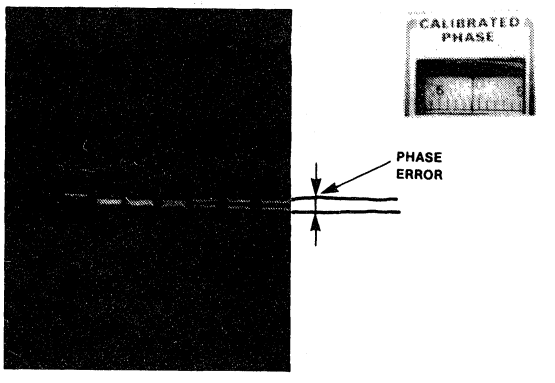


Figure 5. Differential Phase +0.1°

APPLICATIONS

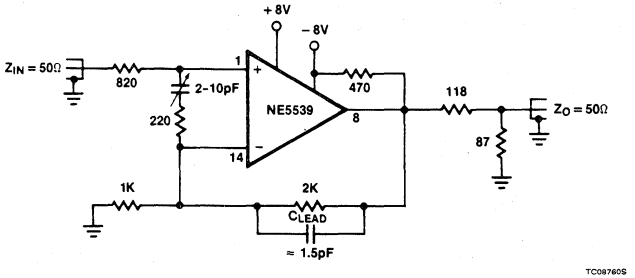


Figure 6. Non-Inverting Follower

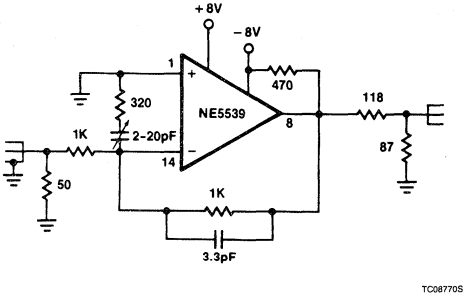


Figure 7. Inverting Follower

Document No.	
ECN No.	
Date of Issue	October 1990
Status	Preliminary Specification
Microcontroller Product	

83C053/87C054

Microcontroller for Television and Video (MTV)

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

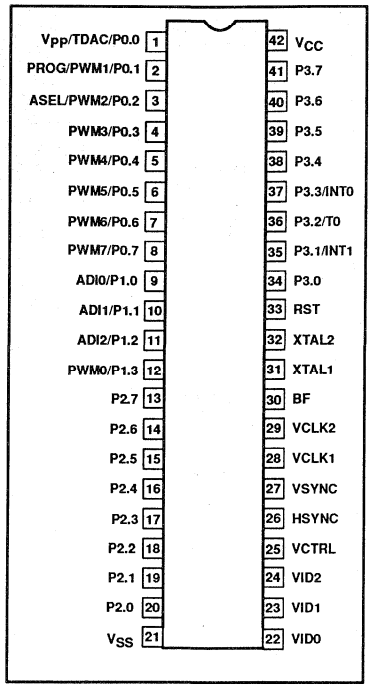
DESCRIPTION

The Microcontroller for Television and Video (MTV) applications is a derivative of Philips' industry-standard 80C51 microcontroller that is intended for use as the central control mechanism in a television receiver or tuner. Providing tuner functions and an On Screen Display facility, it represents a next-generation replacement for the currently available parts.

FEATURES

- 8192 x 8 masked ROM (83C) or 16384 x 8 OTPROM (87C)
- 192 x 8 RAM
- On Screen Display (OSD) Controller
- Three digital video outputs
- Multiplexer/mixer and background intensity controls
- Flexible formatting with OSD New Line Option
- 128 x 10 display RAM
- 60 x 18 x 14 character generator ROM
- Eight text-shadowing modes
- Text color selectable per character
- Background color selectable per word
- Background color vs. video selectable per character
- Eight 6-bit pulse width modulators for analog voltage integration
- One 14-bit PWM for high-precision voltage integration
- D/A converter and comparator with three-input multiplexer
- Nine dedicated I/Os plus 28 port bits
- 15 port bits have alternate uses
- Four high-current open-drain port outputs
- 12 high-voltage (+12V) open drain outputs
- Programmable video input and output polarities
- 80C51 instruction set
- No external memory capability
- 42-pin shrunk DIP (0.07-inch center pins)
- High-speed CMOS technology
- 5V ± 10% operation

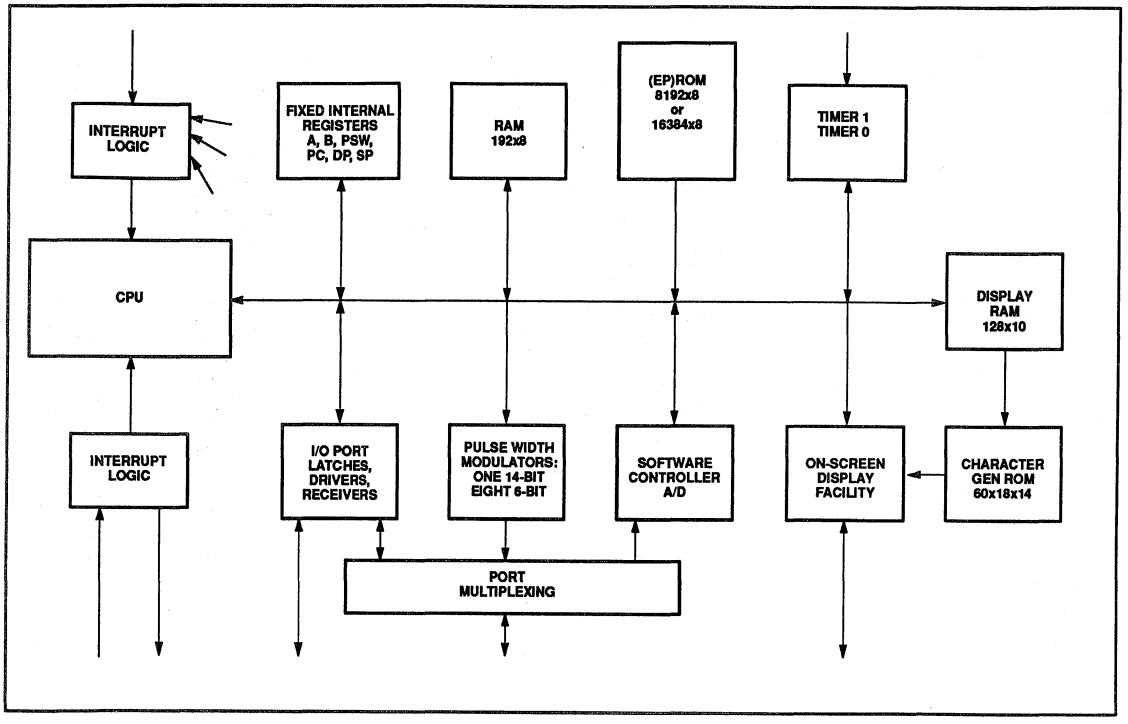
PIN CONFIGURATION



PART NUMBER SELECTION

ROM	EPROM	TEMPERATURE AND PACKAGE	FREQUENCY
P83C053BBP N	P87C054BBP N	0 to +70°C, plastic DIP	3.5 to 12MHz

BLOCK DIAGRAM



Philips Components

Data sheet	
status	Preliminary specification
date of issue	December 1990

PC.8582 Family

256 x 8-BIT CMOS EEPROMS with I²C-BUS interface

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories.

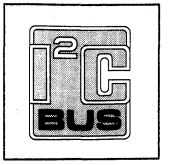
Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient.

Chip select is accomplished by the three address inputs, which also allows up to eight devices to be connected to the I²C-bus.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, and PCF8581
- Mini-pack package for SMD technology.



QUICK SELECTION GUIDE

TYPE	PCF8582A	PCA8582B	PCF8582C	PCD8582D	PCF8582E
extended temperature range	•	•	•	–	•
extended voltage supply range	–	–	•	•	–
no external RC required	–	–	•	•	•
single bit error correction for extended number of erase/write cycles	–	•	•	•	•

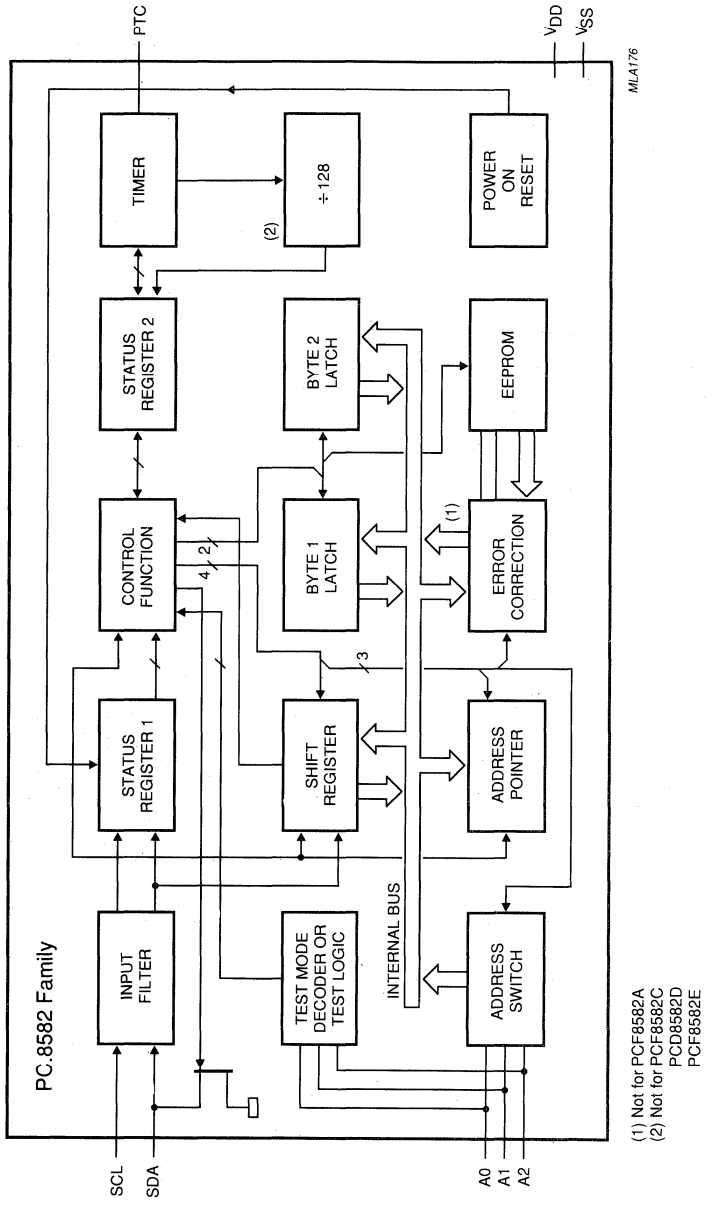


Fig.1 Block diagram.

(1) Not for PCF8582A.

(2) Not for PCF8582C, PCD8582D or PCF8582E.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

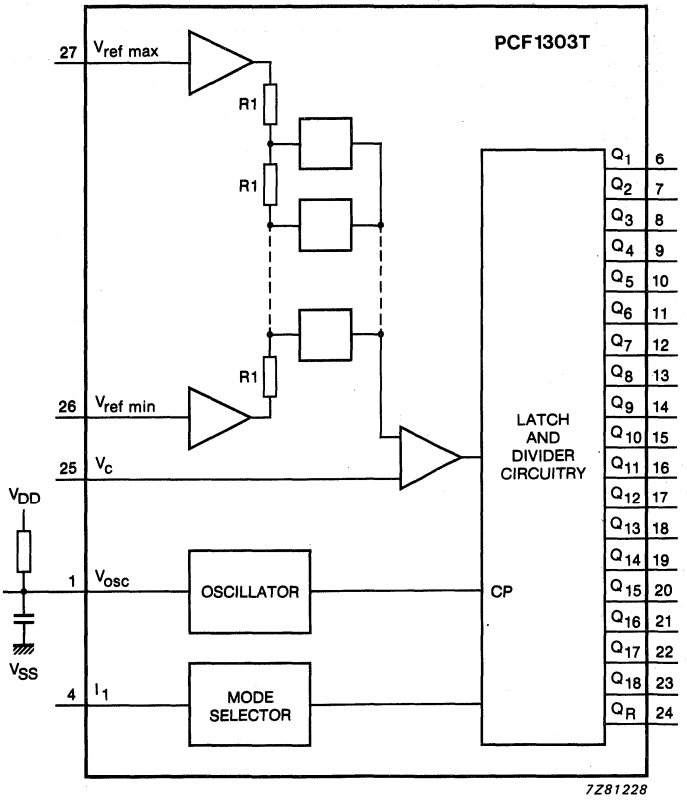
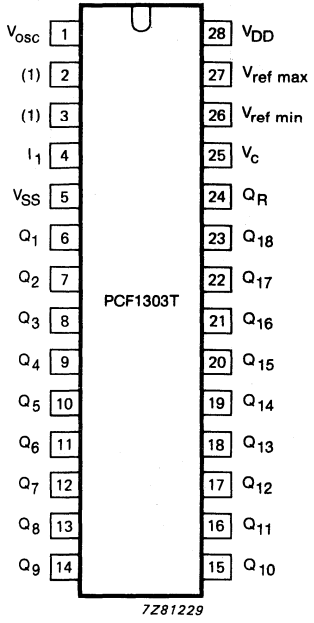


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

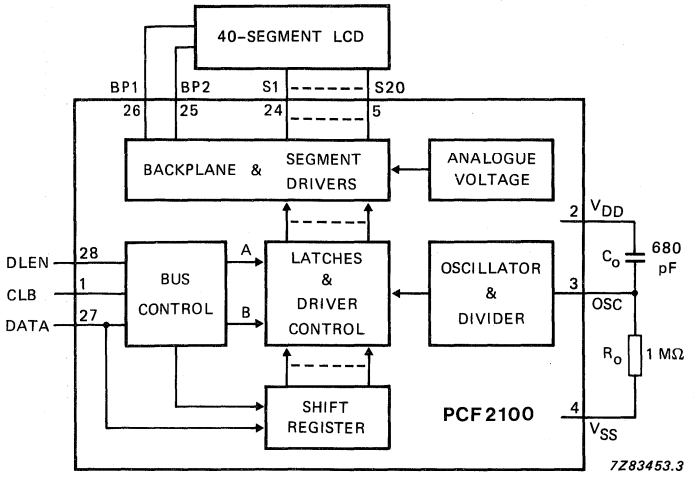


Fig. 1 Block diagram; PCF2100

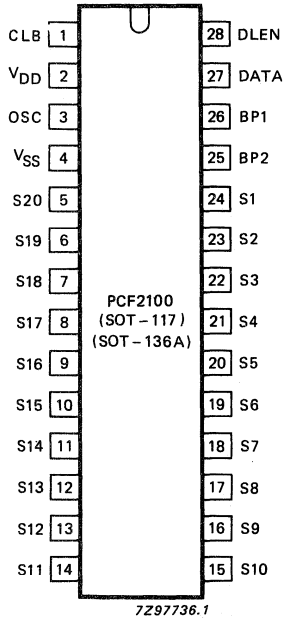


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

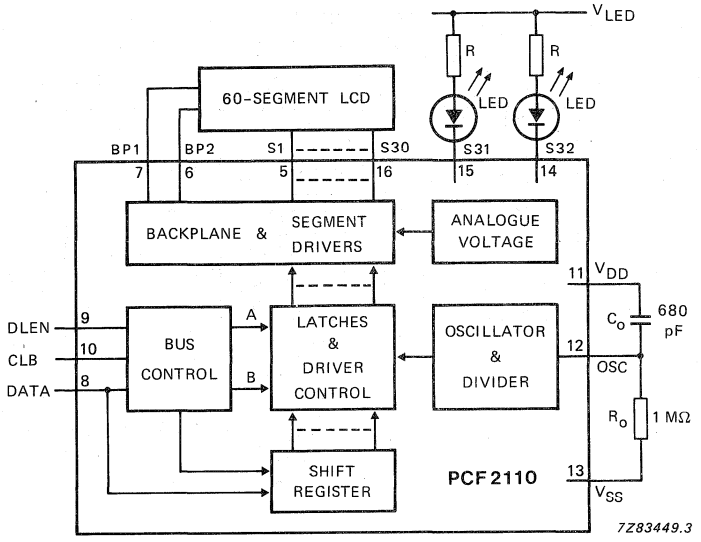


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

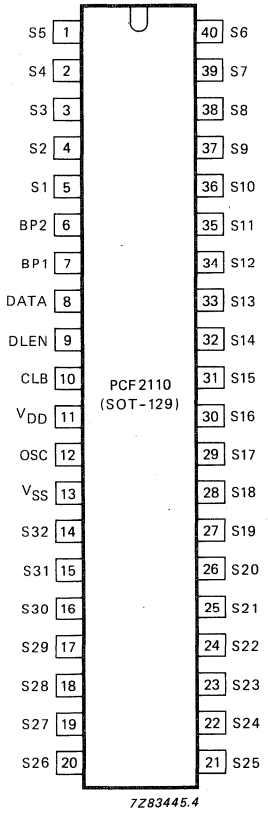


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

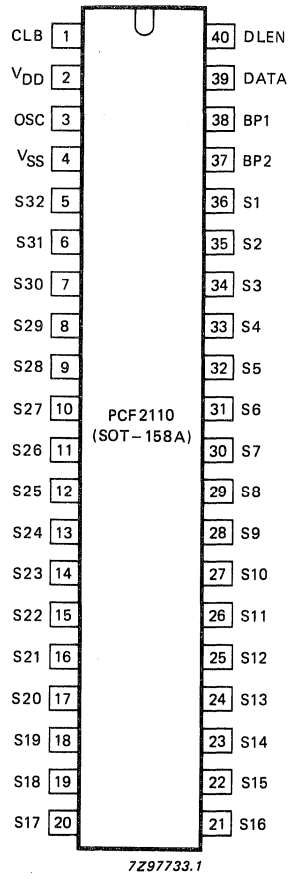


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

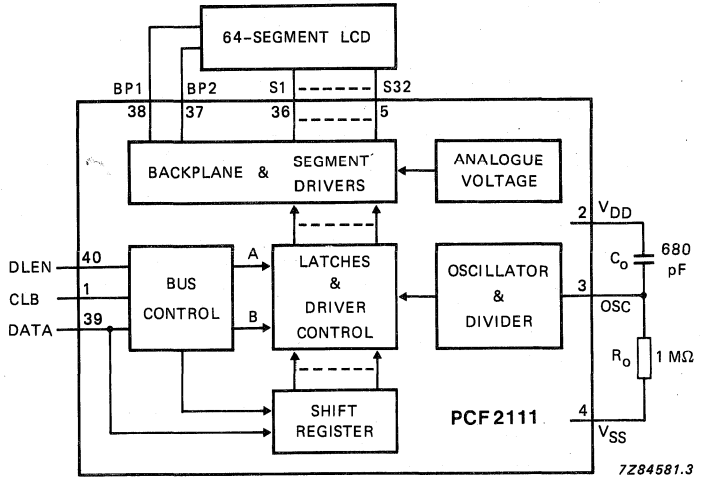


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

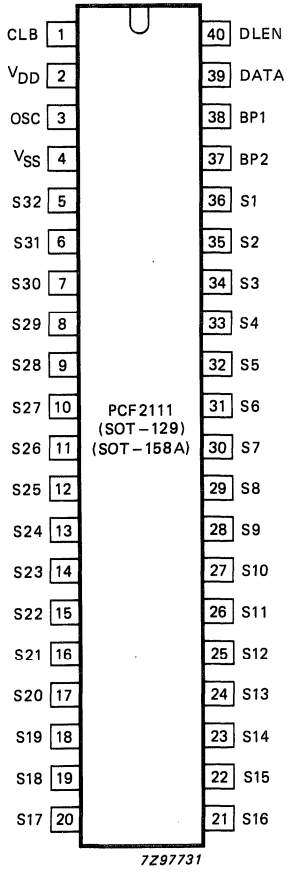


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line } CBUS
40	DLEN	data line enable } CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

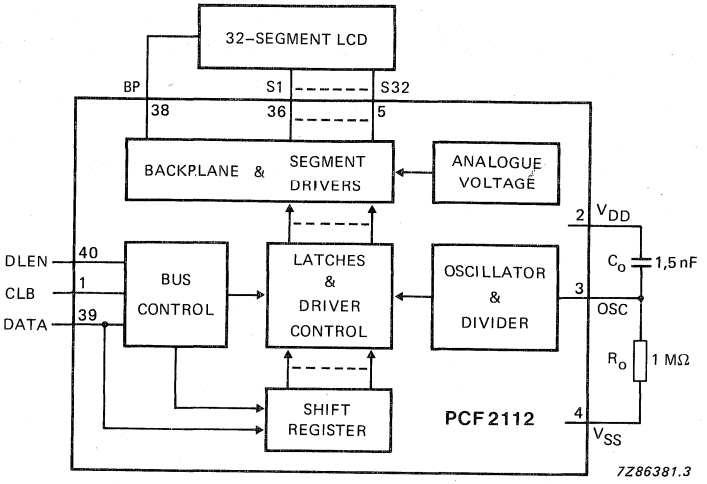


Fig. 8 Block diagram; PCF2112

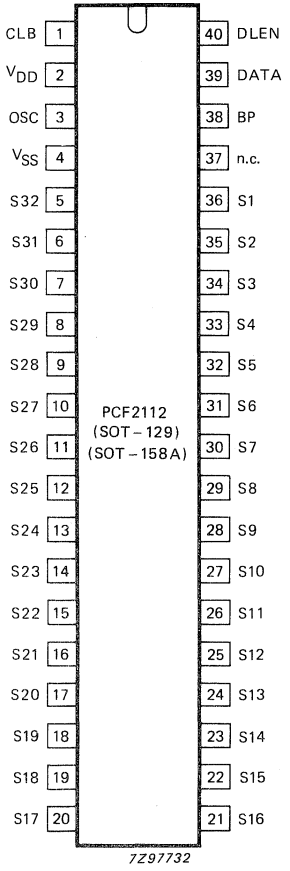


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

Single-chip 8-bit microcontroller family specification

PCF84CXXX

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

1 INTRODUCTION

This family data sheet describes the microcontroller core which is common for all members of the PCF84CXXX family. For complete information of a particular microcontroller, consult both the specific microcontroller data sheet and this family data sheet.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single package
- Up to 8 K bytes ROM
- Up to 256 bytes RAM
- Over 80 instructions, all instructions 1 or 2 cycles
- 8 or more quasi bi-directional I/O port lines
- 8-bit programmable timer/event counter
- 3 single-level vectored interrupts (external, 8-bit programmable timer/counter, SIO/derivative)
- 2 Test inputs: T0 (may also be used as an interrupt) and T1 (may also be used as an input to an 8-bit counter)
- Serial I/O interface (not all devices)
- Power-on-reset
- 2 power reduction modes: Idle and Stop
- V_{DD} supply range: 2.5 V to 5.5 V
- Clock frequency range: 450 kHz to 10 MHz
- Operating temperature range: −40 °C to 85 °C
- Silicon gate CMOS fabrication process

3 GENERAL DESCRIPTION

The PCF84CXXX single-chip 8-bit microcontroller family consists of a wide range of derivatives containing up to 8 K bytes of on-chip mask programmable program ROM and up to 256 bytes RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the MAB8048.
A number of PCF84CXXX family members may be used as CMOS replacements for their NMOS counterparts, where lower power consumption and higher speed are required.

The family is well supported with:

- Cross assemblers
- In-circuit emulation tools
- Window debugger
- Piggy-back versions for prototyping.

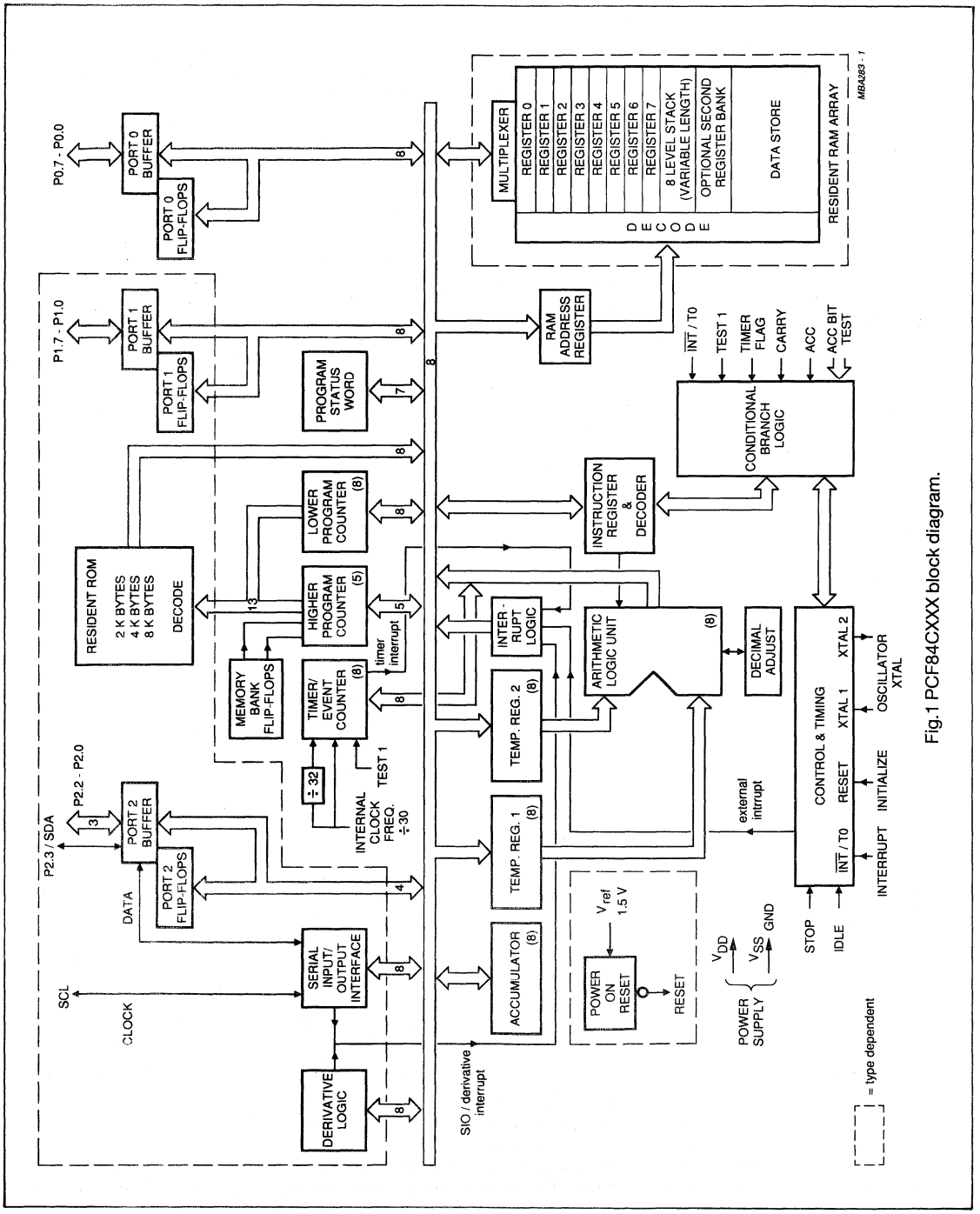


Fig.1 PCF84CXXX block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: –40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see 84CXXX family specification

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

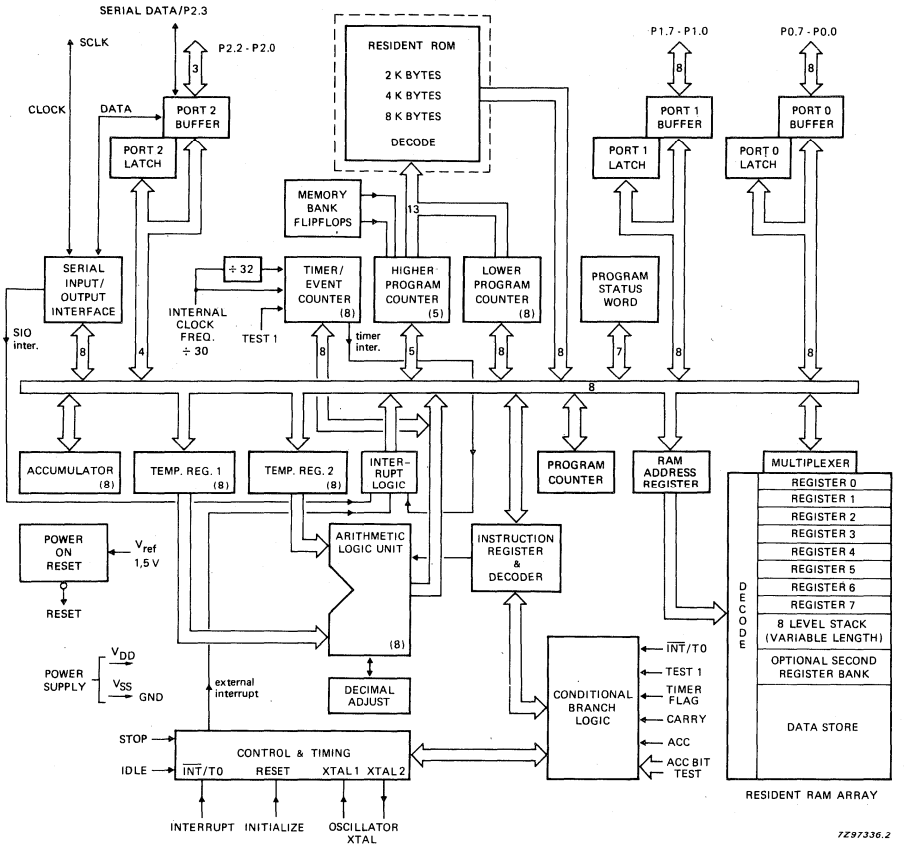


Fig. 1 Block diagram.

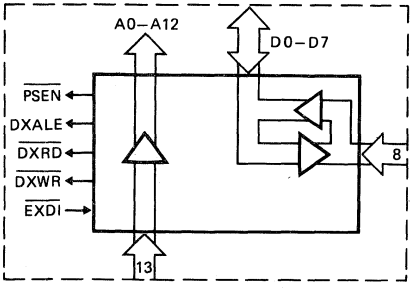


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

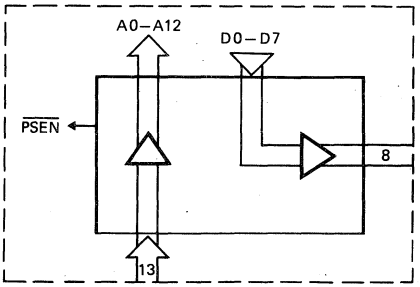


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Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C12, PCF84C22 and PCF84C42 microcontrollers. Each device has 13 quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C12 – 64 x 8 RAM, 1 K x 8 ROM
- PCF84C22 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C42 – 64 x 8 RAM, 4 K x 8 ROM

These efficient microcontrollers also perform well as arithmetic processors. The instruction set is similar to that of the MAB8048. They have bit handling abilities and facilities for both binary and BCD arithmetic.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K, 2 K or 4 K x 8 ROM
- 64 x 8 RAM
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level, vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 V to 5.5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: –40 to + 85 °C

PACKAGE OUTLINES

PCF84C12/22/42P: 20-lead DIL; plastic (SOT146).
PCF84C12/22/42T: 20-lead mini-pack; plastic (SO20, SOT163A).

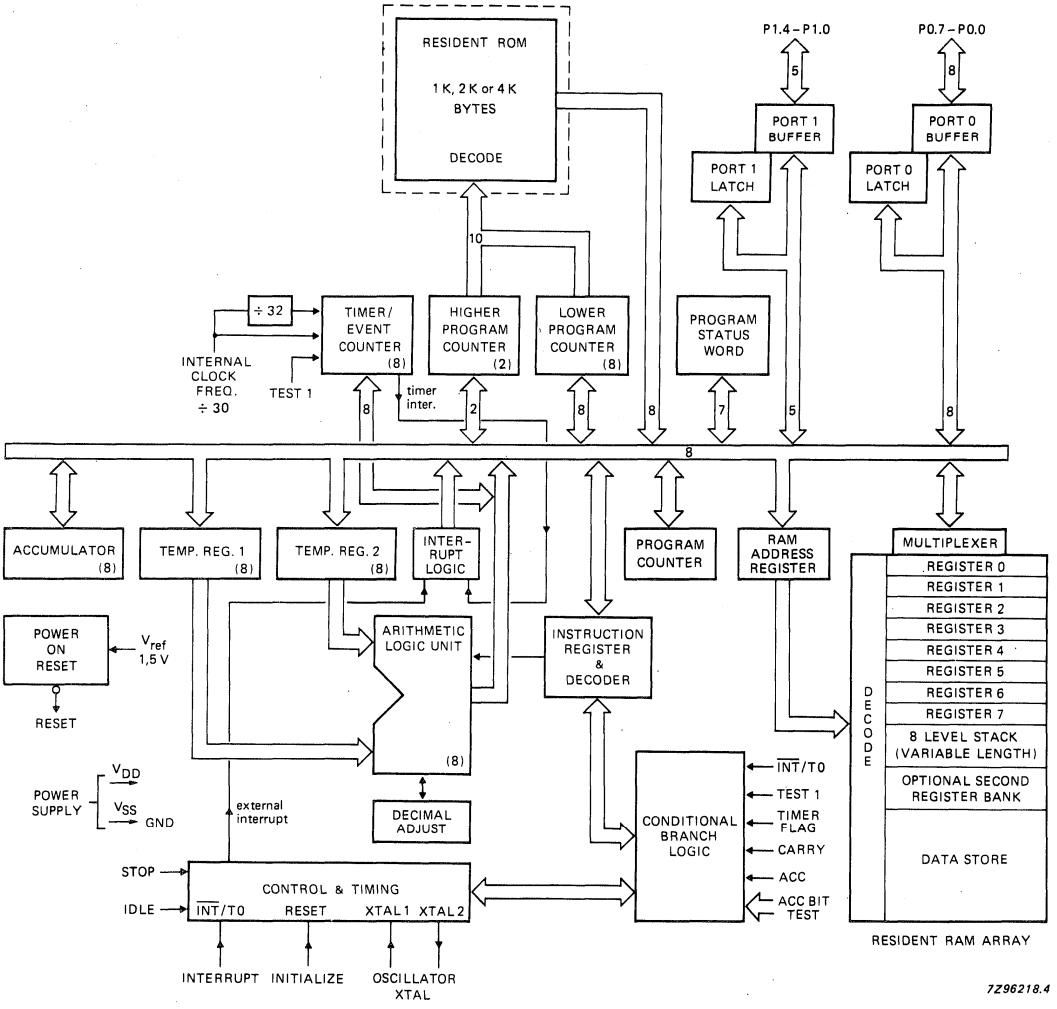


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the 84CXXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer
  (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158A).

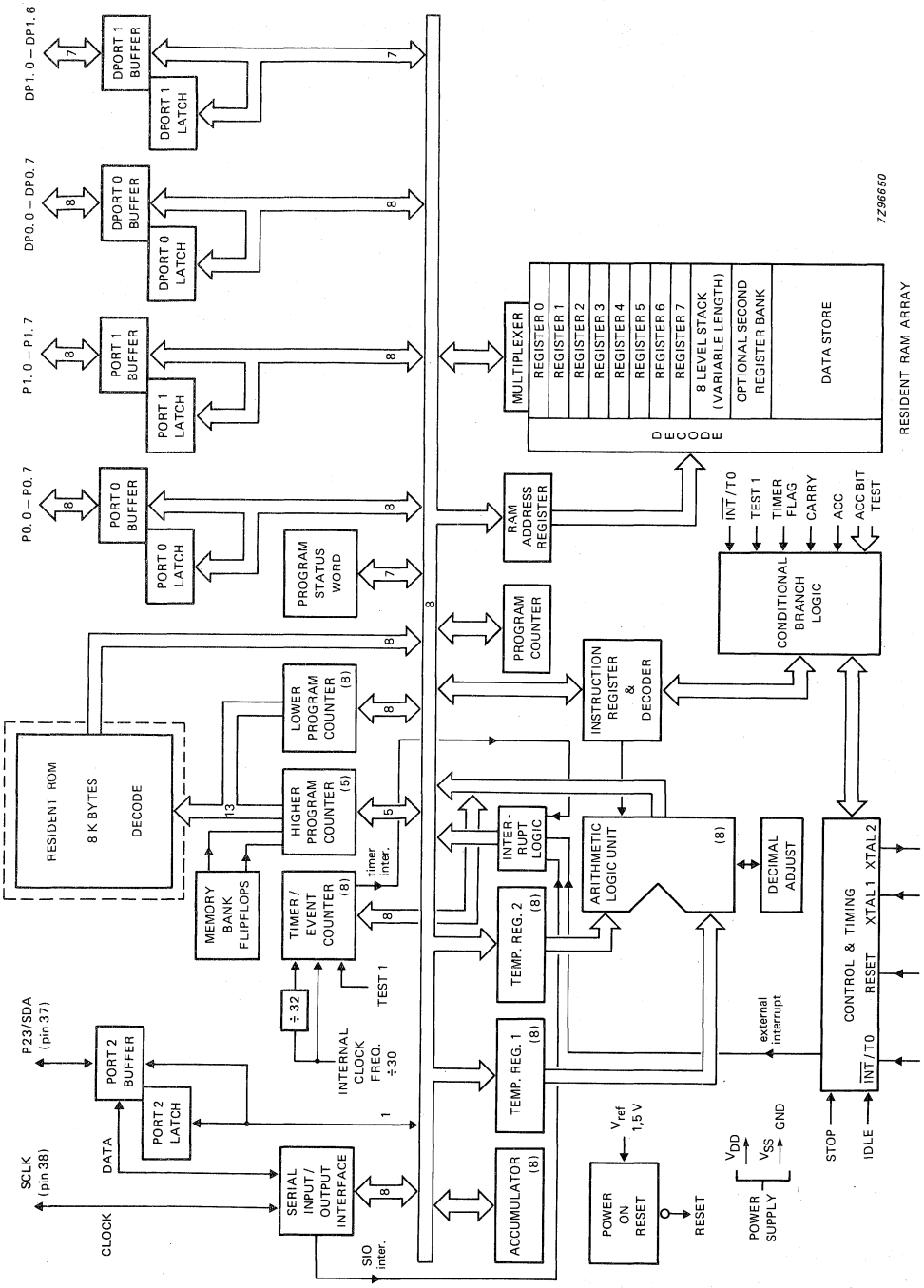


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 BYTES EEPROM

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C121. The PCF84C121 has 13 quasi-bidirectional I/O port lines, three single-level vectored interrupts (one external and two timer), 8 bytes of EEPROM, two 8-bit timer counters and on-chip clock oscillator and clock circuits.

This efficient microcontroller also performs well as an arithmetic processor. The PCF84C121 is pin- and instruction set compatible with the PCF84C12. The PCF84C121 has bit handling abilities and facilities for both binary and BCD arithmetic.

This microcontroller is a member of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a single 20-lead DIL or SO package
- 1 K x 8 ROM
- 64 x 8 RAM
- 8 x 8 EEPROM, designed for 10000 erase/write cycles per byte minimum
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- 3 single-level, vectored interrupts: external, Timer 1 and Timer 2
- Two test inputs: one of which is also the external interrupt input
- 8-bit programmable timer/event counter
- Clock frequency range: 450 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C; 0 to +55 °C for programming

PACKAGE OUTLINES

PCF84C121P: 20-lead DIL; plastic (SOT146).
PCF84C121T: 20-lead mini-pack; plastic (SO20; SOT163A).

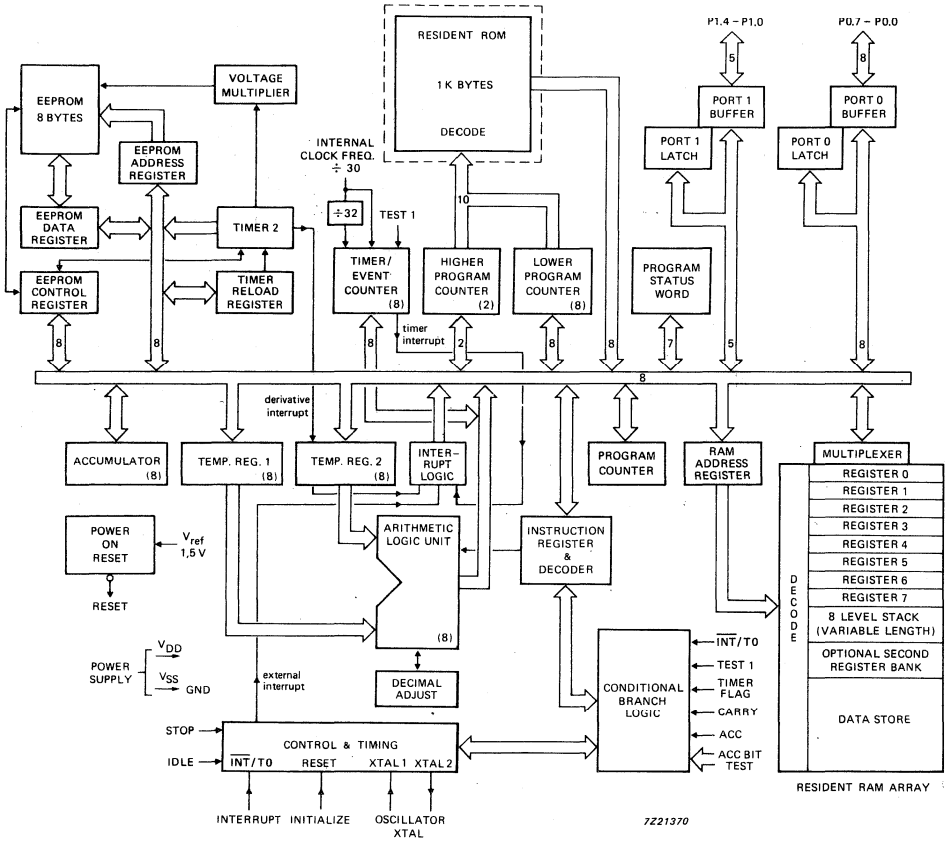


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The PCF84C230 is a single-chip 8-bit microcontroller manufactured in CMOS technology, and is a member of the 84CXXX family. For detailed information see the 84CXXX family specification.

The PCF84C230 provides 12 general purpose quasi-bidirectional I/O port lines, a line that is directly testable (T1), one external interrupt line, and an LCD driver for up to 64 graphic elements. The IC is mask-programmable and is designed for control in small systems with LCD displays.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL package
- 2 K ROM bytes
- 64 RAM bytes
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 12 quasi-bidirectional I/O port lines
- Configuration of I/O lines can be individually selected by mask (pull-up, open drain, push-pull)
- LCD drive circuit with 16 segment drivers and selectable backplane drive configuration: static or 2/3/4 multiplex, to drive up to 64 graphic elements
- LCD possible during STOP mode
- Single-level vectored interrupts: external and timer/event counter
- Power-on reset and low voltage detector
- Single supply voltage from 2.5 V to 5.5 V
- STOP and IDLE modes
- Clock frequency 100 kHz to 10 MHz
- Operating ambient temperature range: −40 to + 85 °C

PACKAGE OUTLINES

40-lead DIL; plastic (SOT129).
40-lead mini-pack; plastic (VS040; SOT158A).

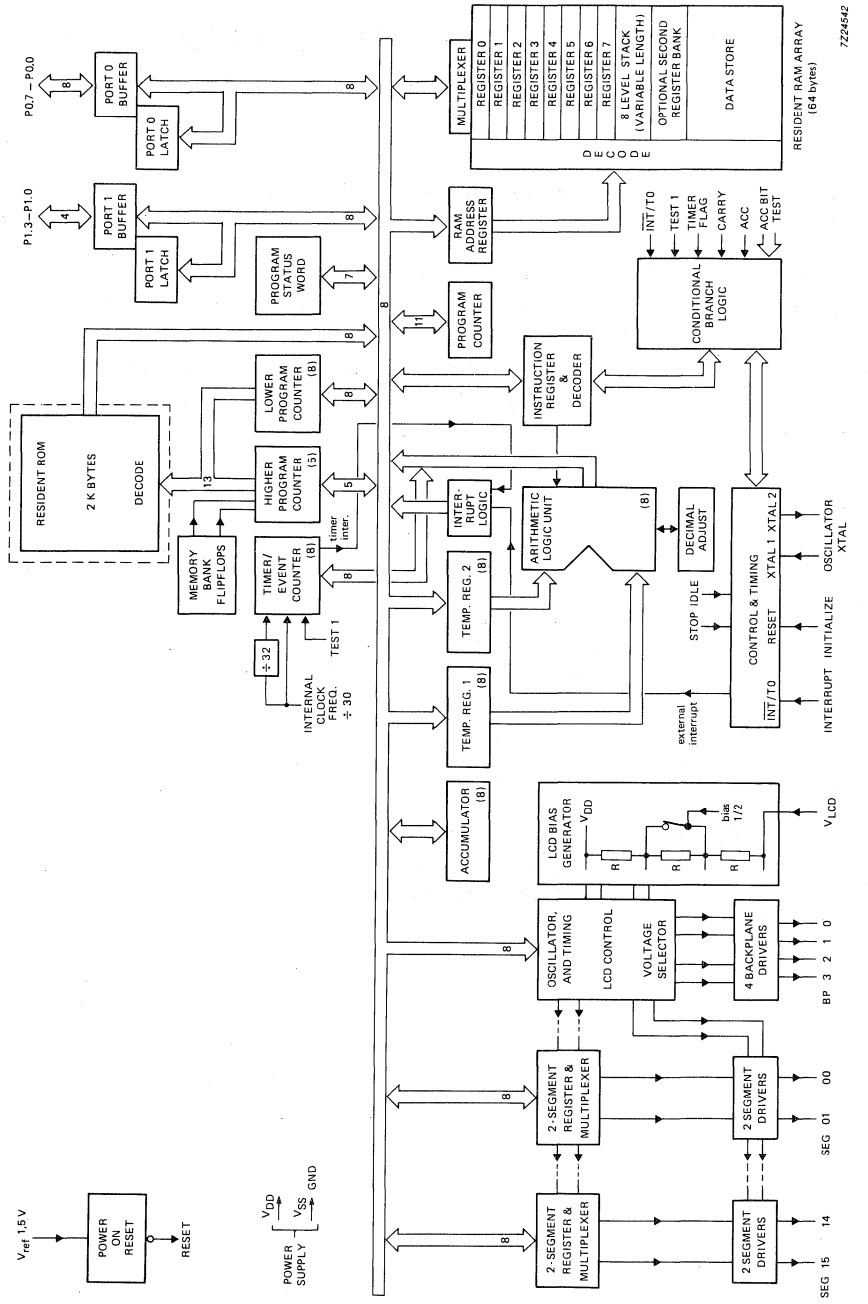


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the 84CXXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the 84CXXX family specification.

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

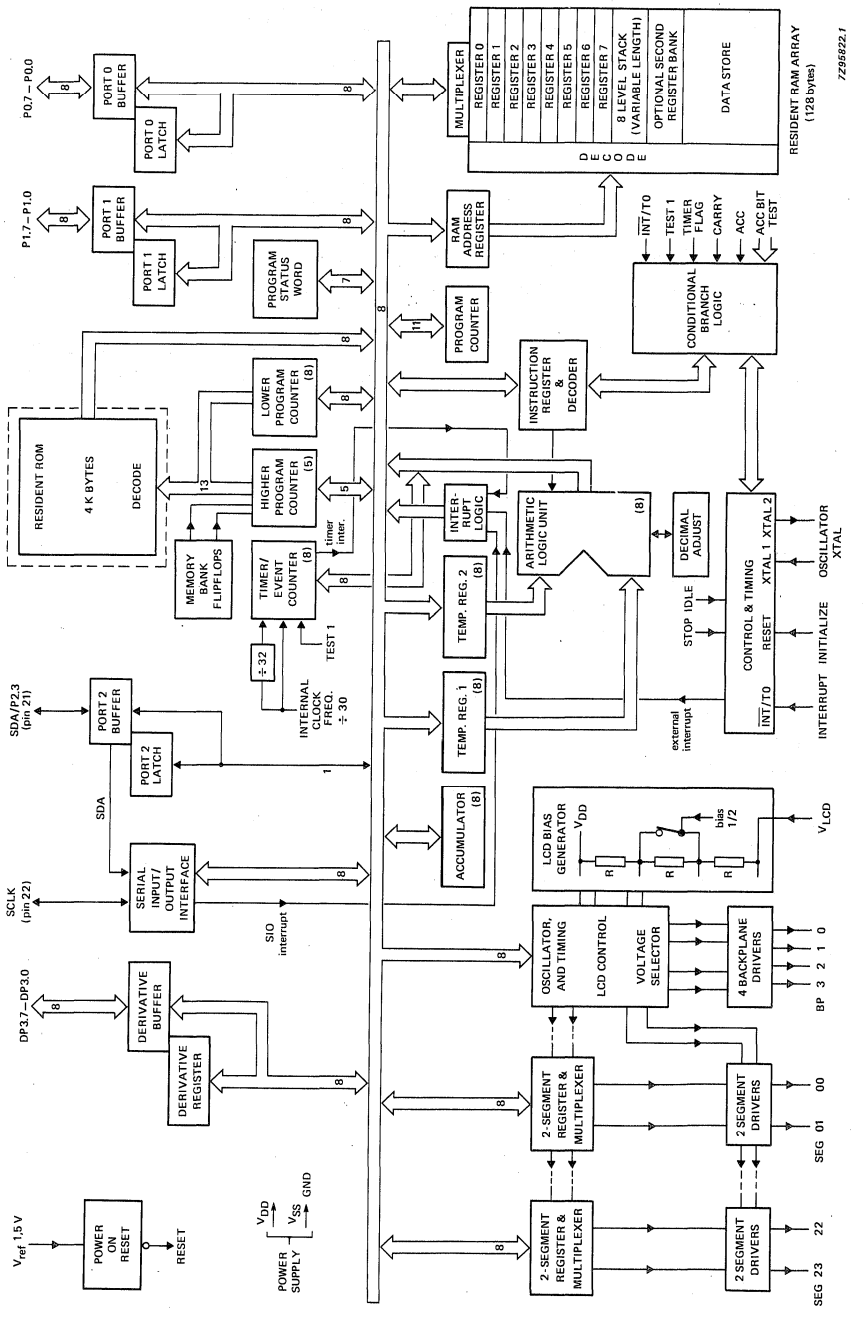


Fig. 1 Block diagram; PCF84C430.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

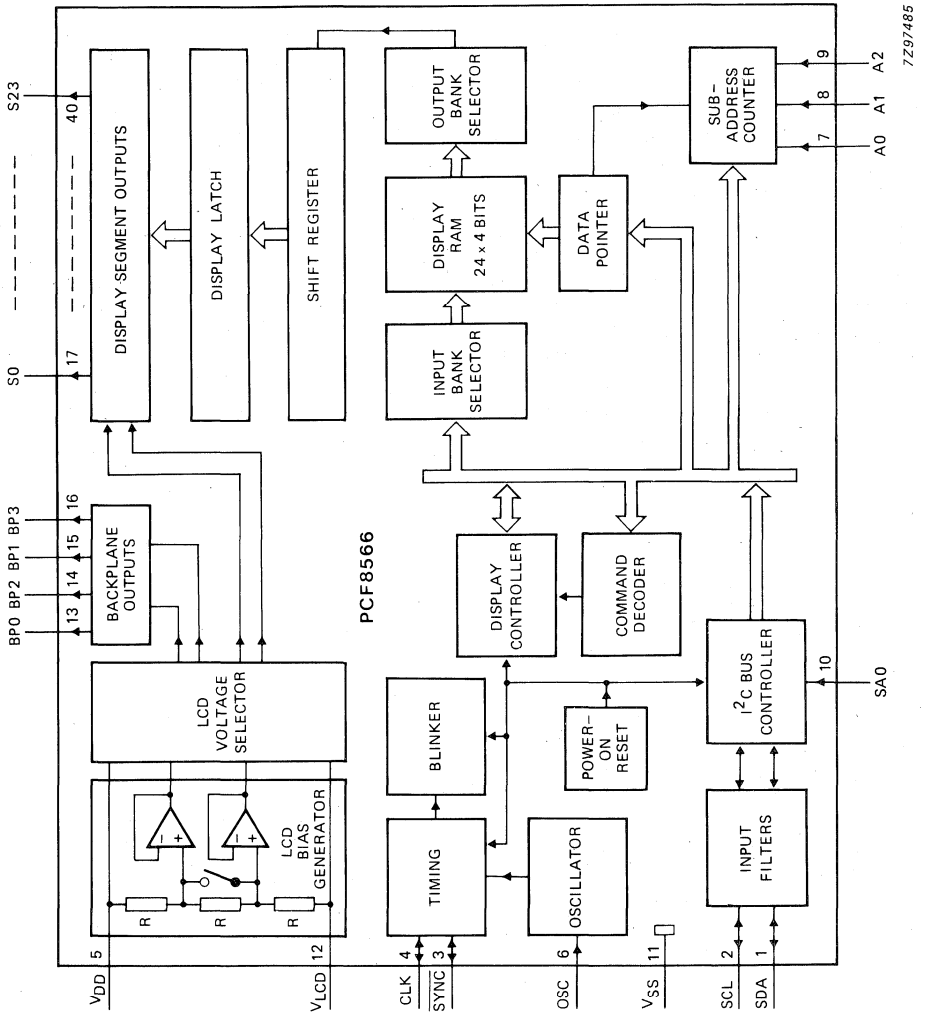


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA SHEET OR DATA BOOK

LCD DIRECT MODE DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8567C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing and hardware subaddressing..

Features

- Direct drive mode with up to 32 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display

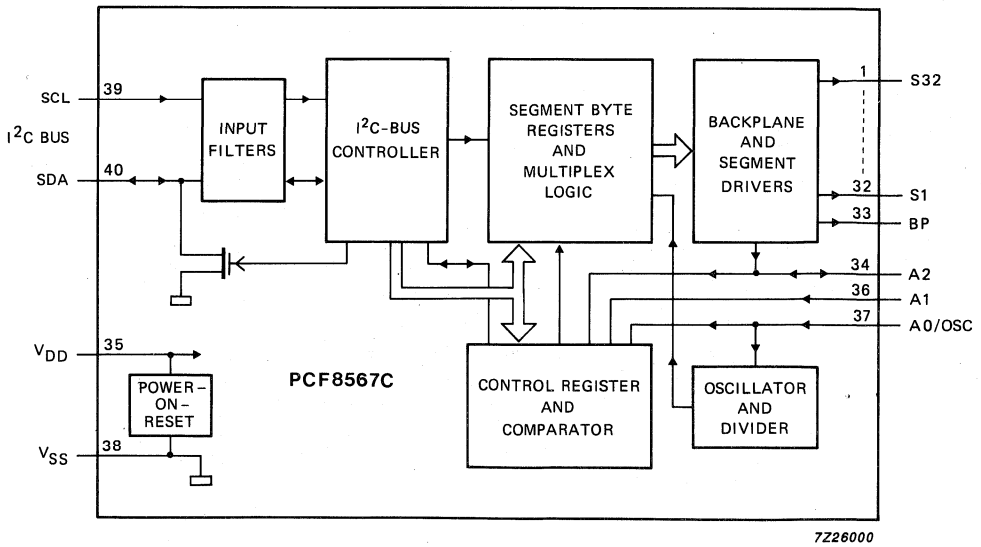


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8567CP: 40-lead DIL; plastic (SOT129).
PCF8567CT: 40-lead mini-pack; plastic (VSO40; SOT158A).

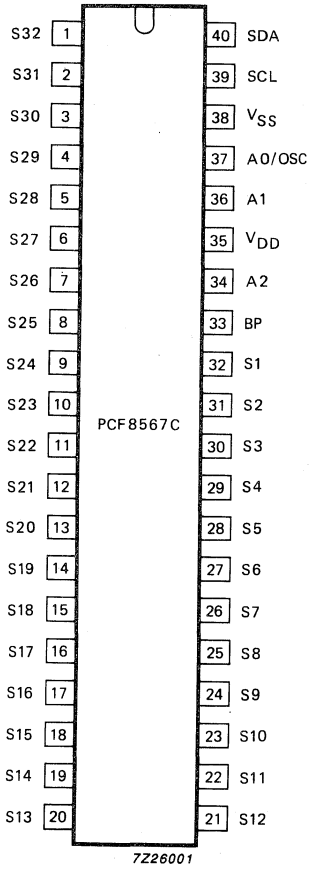


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

39	SCL	I^2C-bus clock line
40	SDA	I^2C-bus data line

Inputs

34	A2	hardware address line
36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

33	BP	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8567C on the bus. Line A0 is shared with OSC to reduce pin-out requirements.

A0/OSC — Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 — Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2 — Line A2 must be defined as LOW (logic 0) by connecting to V_{SS} or leaving unconnected (internal pulldown)), or as HIGH (logic 1) by connection to V_{DD}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

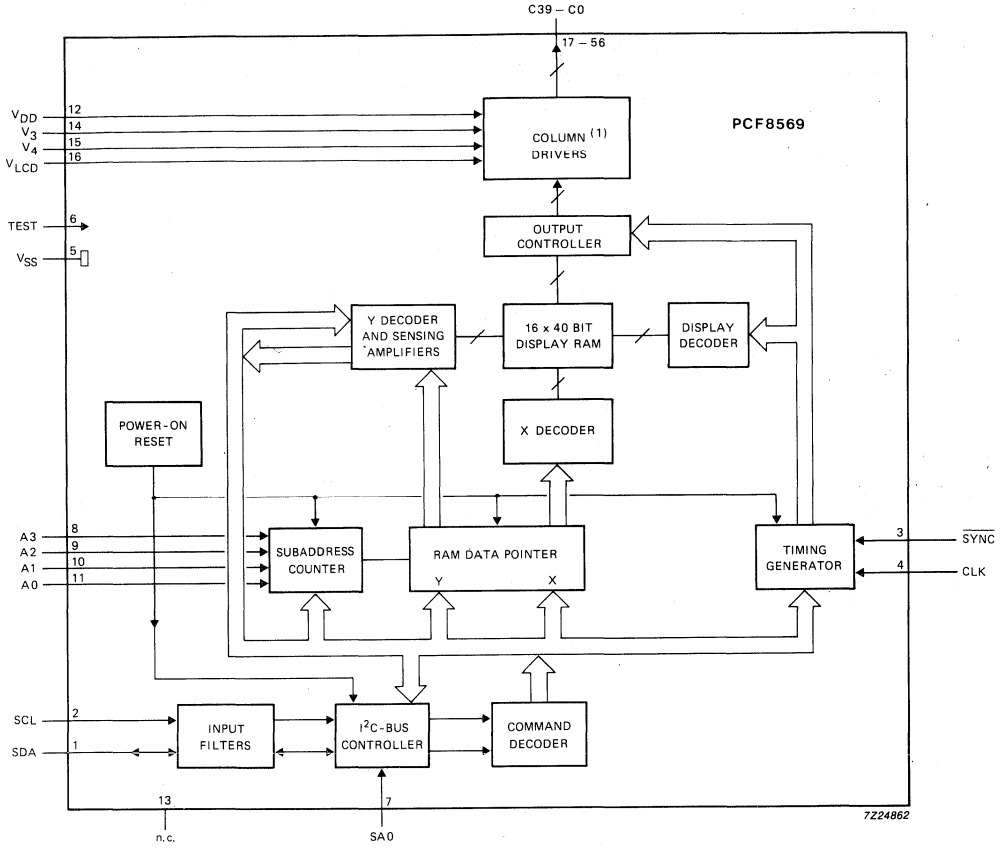
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

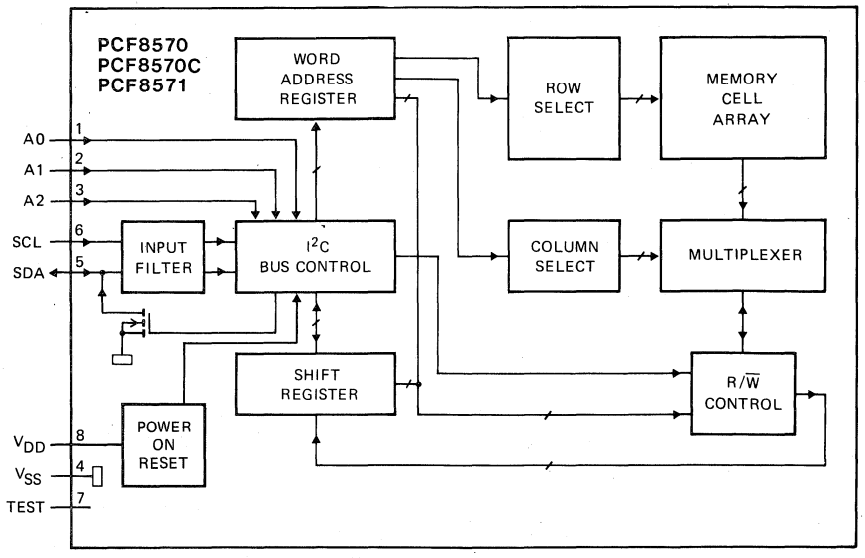


Fig.1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C-bus)
6	SCL	serial clock line (I²C-bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

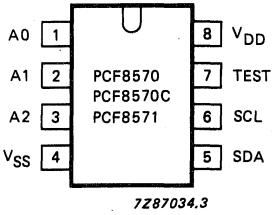


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	−	10	mA
DC output current	$\pm I_O$	−	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	50	mA
Total power dissipation	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

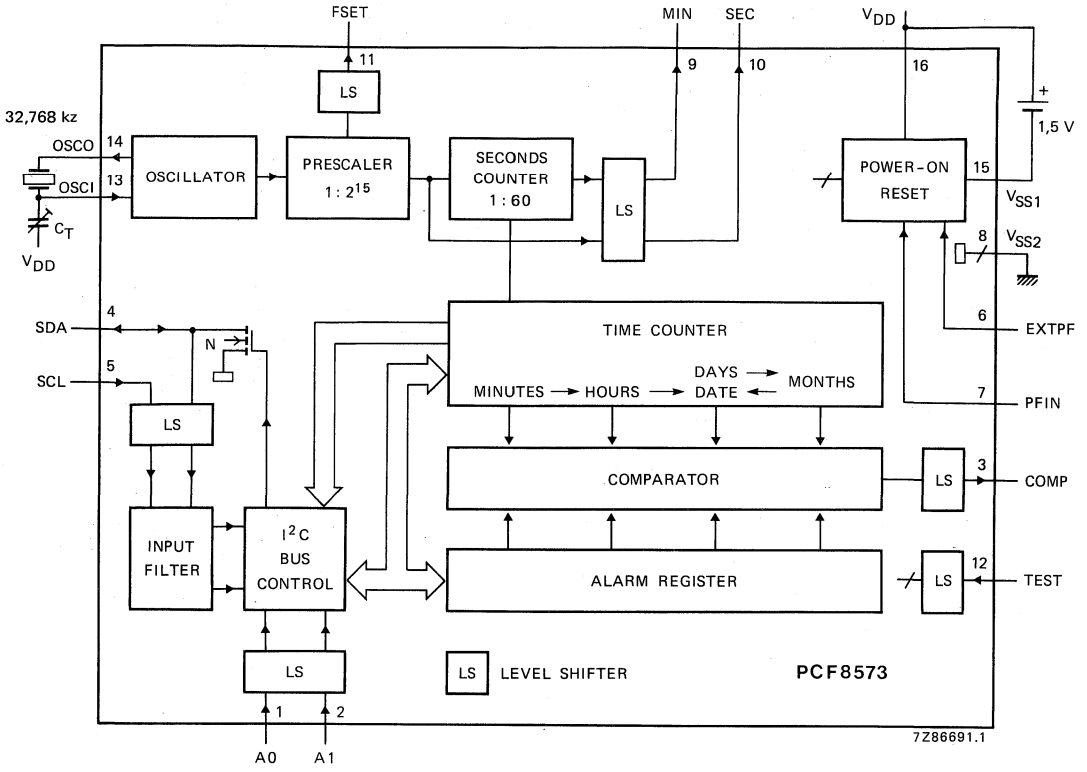


Fig.1 Block diagram.

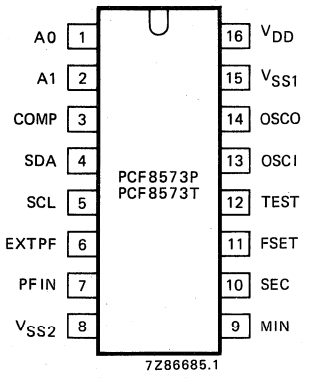


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

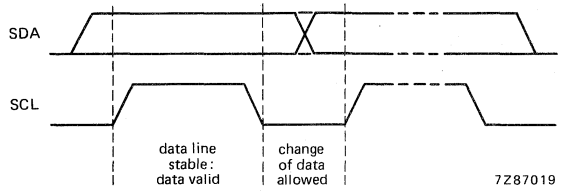


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

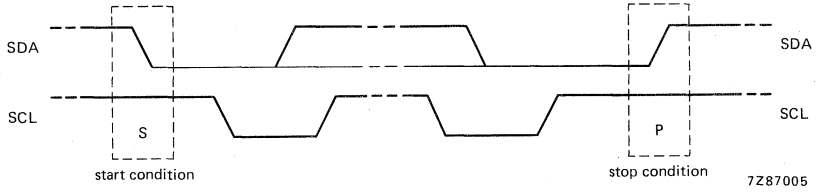


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

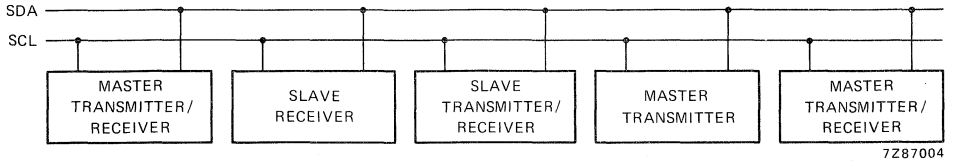


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

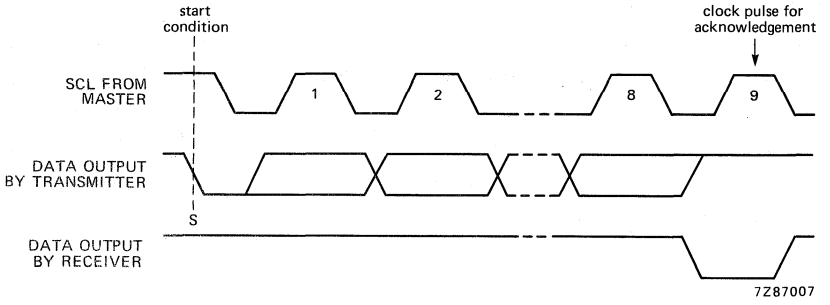


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

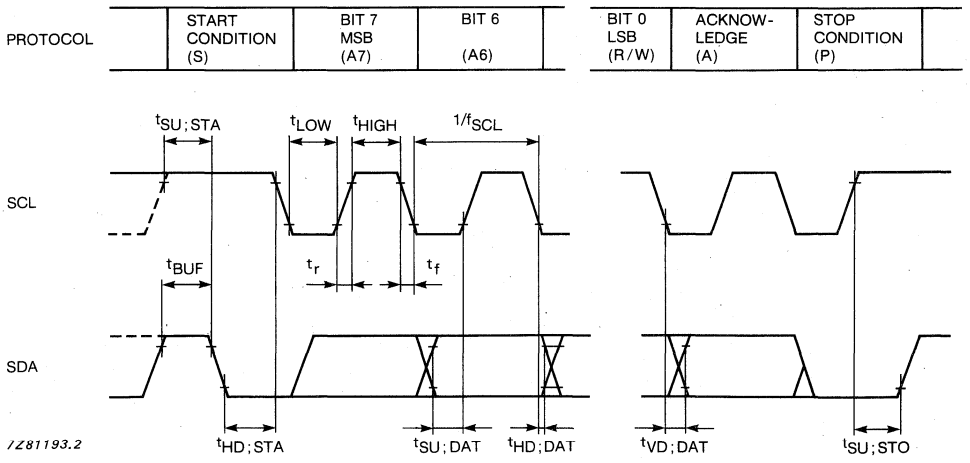


Fig.7 I^2C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

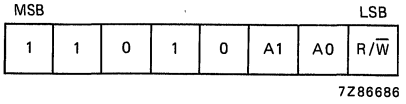


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

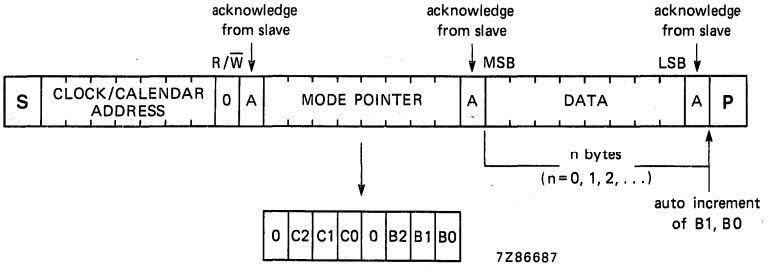


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB			DATA				LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

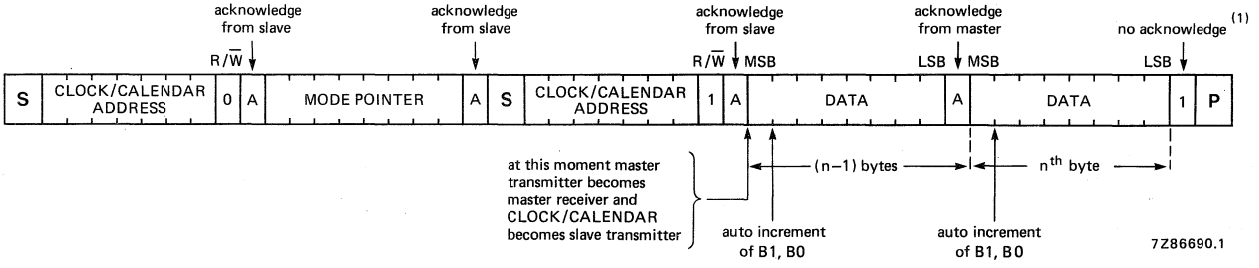
MSB			DATA				LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit

* = minutes

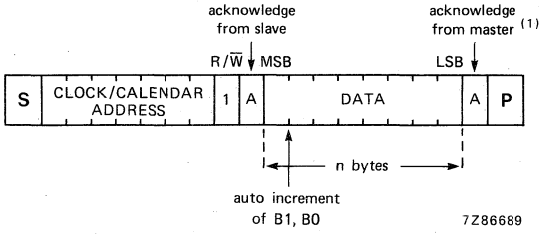
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I^2C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geqslant$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_L\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	1.0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2.5 to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	$\|I_L\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2.5 V; I_O = 0.3 mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2.5 V; $-I_O$ = 0.1 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0.5 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

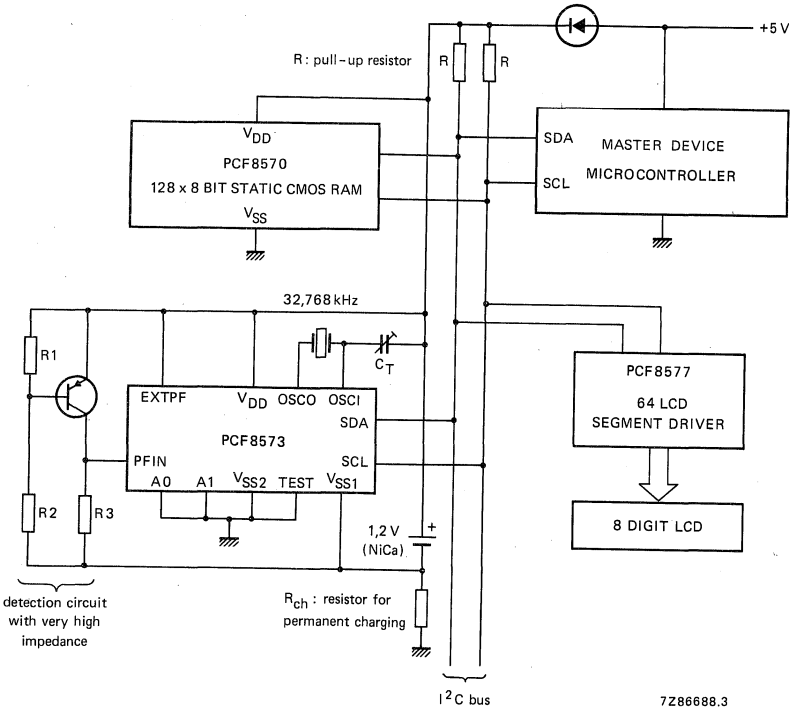


Fig.12 Application example of the PCF8573 clock/calendar.

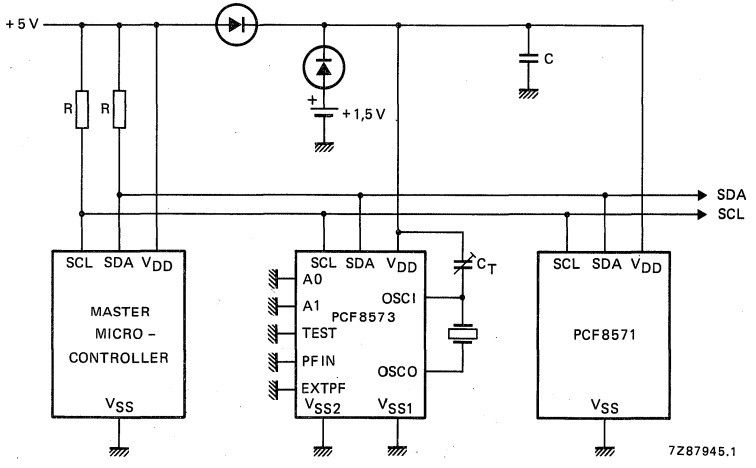


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

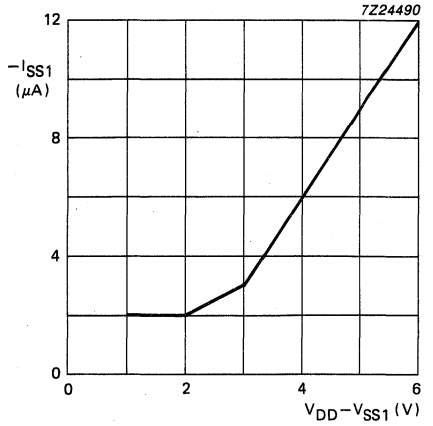


Fig.14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at T_{amb} = −40 to +85 °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

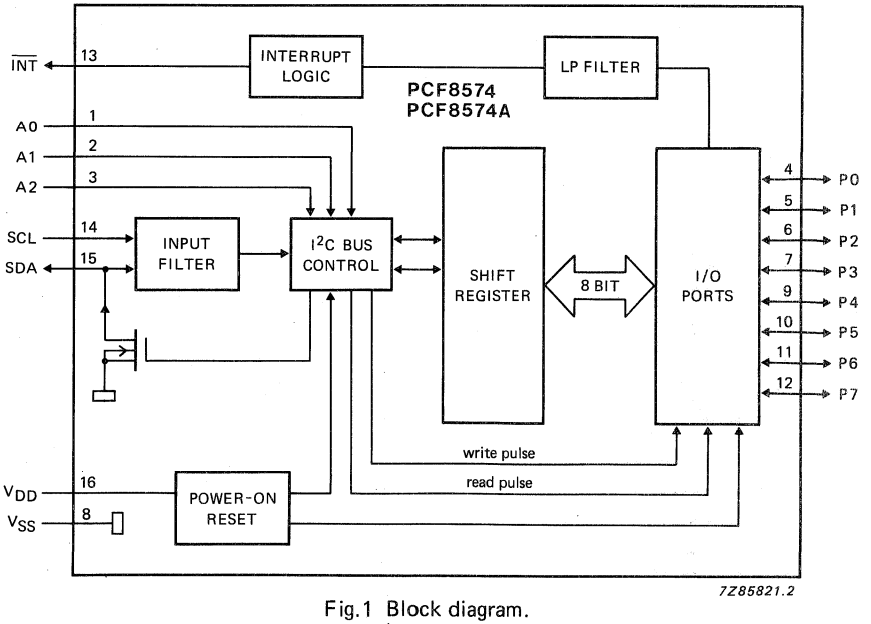


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

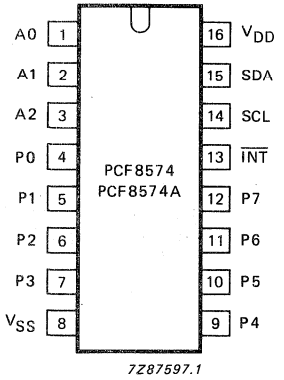


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

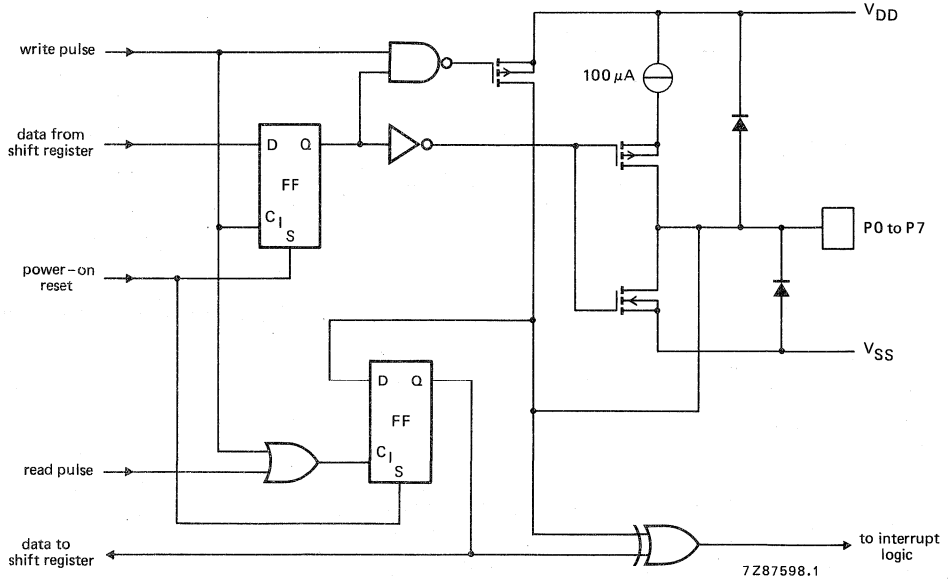


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

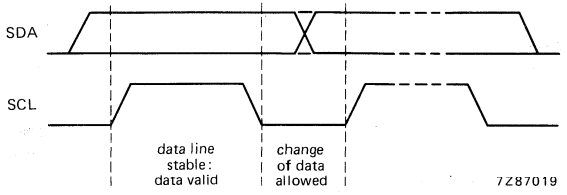


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

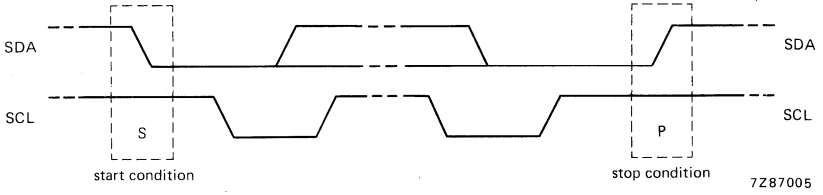


Fig.5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

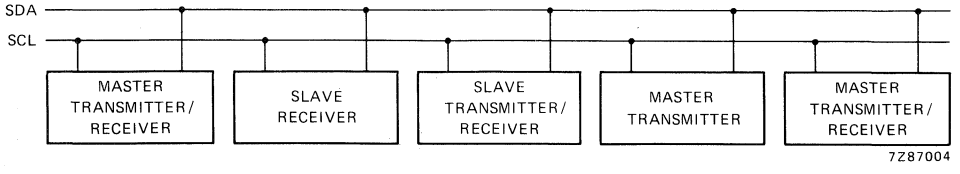


Fig.6 System configuration.

CHARACTERISTICS OF THE I²C-BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

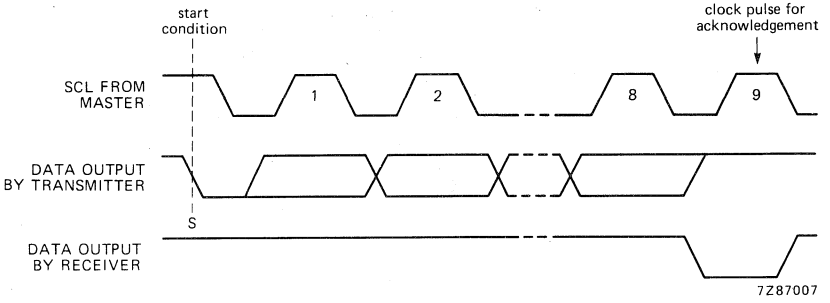


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

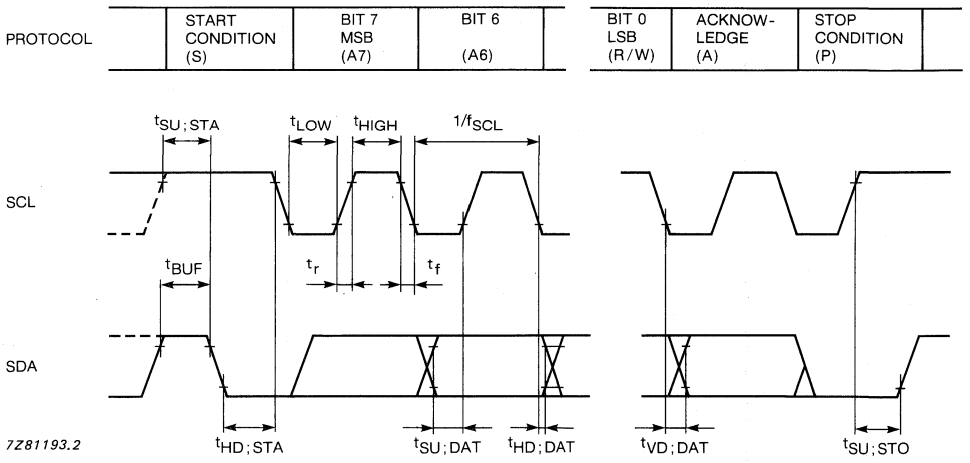
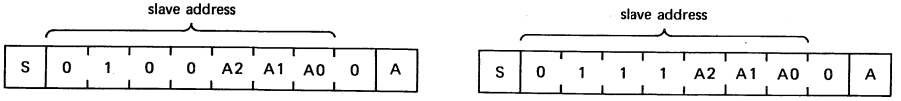


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574. (b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

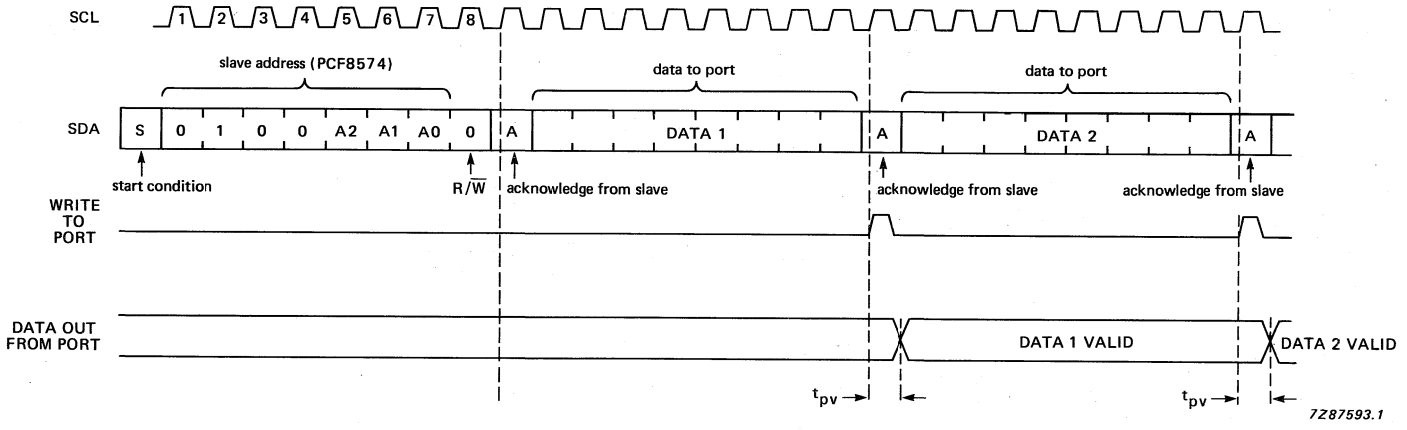


Fig.10 WRITE mode (output port).

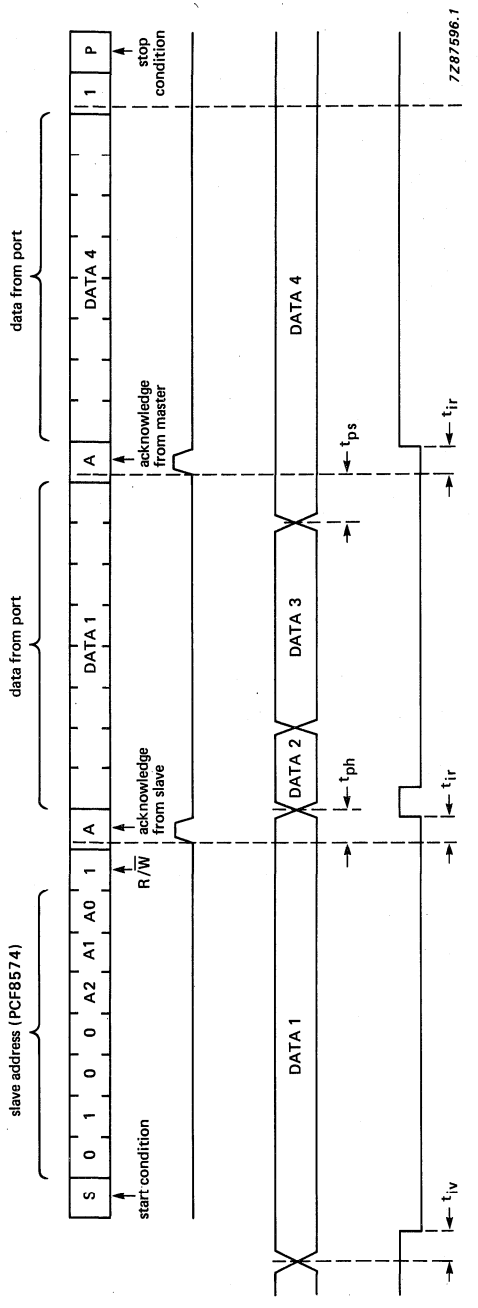


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

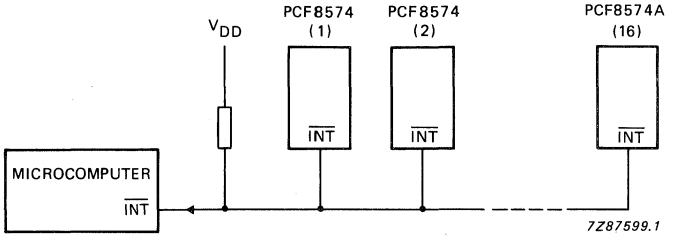


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

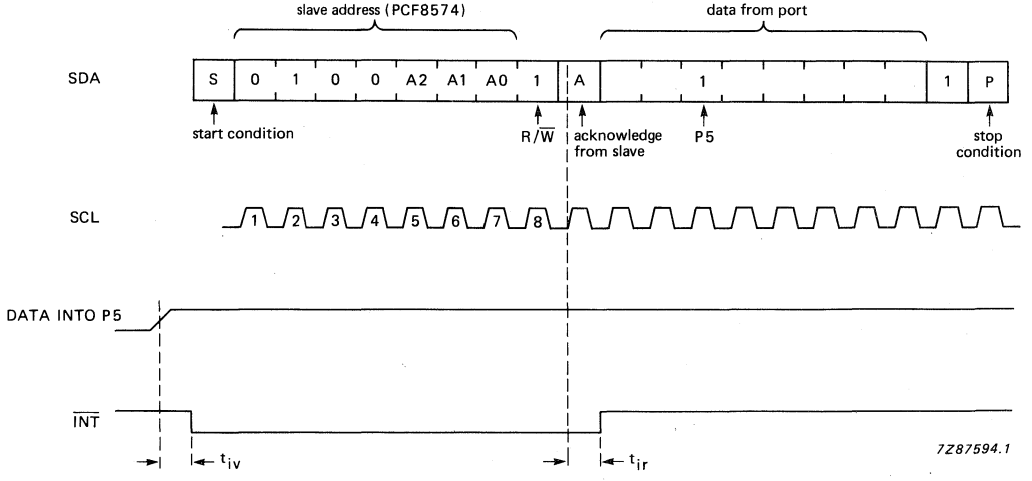


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

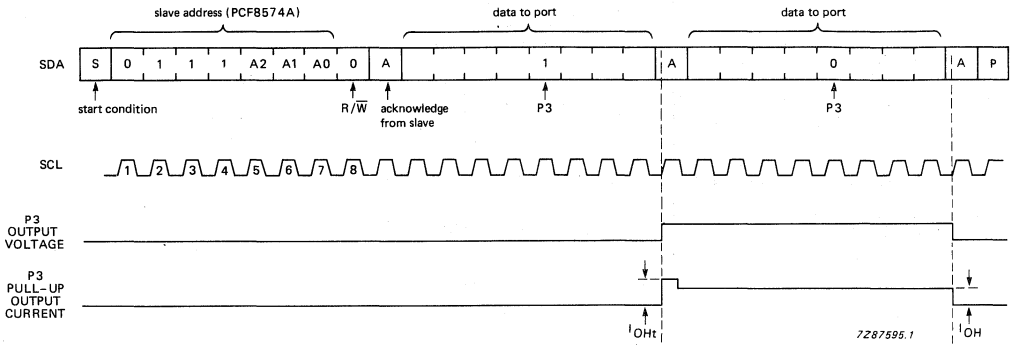


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	−	20	mA
DC output current	$\pm I_O$	−	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	100	mA
Total power dissipation	P_{tot}	−	400	mW
Power dissipation per output	P_O	−	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

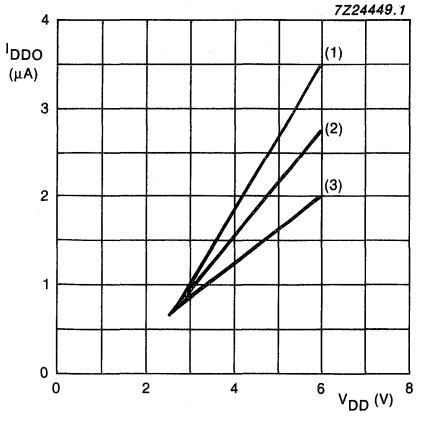
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L \leqslant$ 100 pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_L\|$	–	–	250	nA

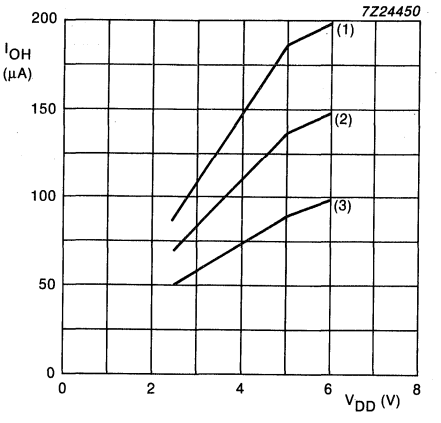
Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).



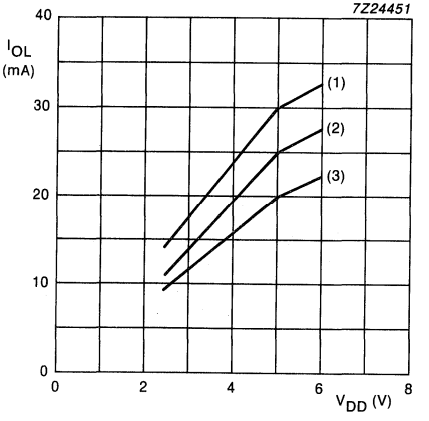
(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.15 Typical standby current (I_{DDO}) as a function of supply voltage (V_{DD}).



(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.16 Typical port output current HIGH (I_{OH}) as a function of supply voltage (V_{DD}); $V_{OH} = V_{SS}$.



(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.17 Typical port output current LOW (I_{OL}) as a function of supply voltage (V_{DD}); $V_{OL} = 1\ V$.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

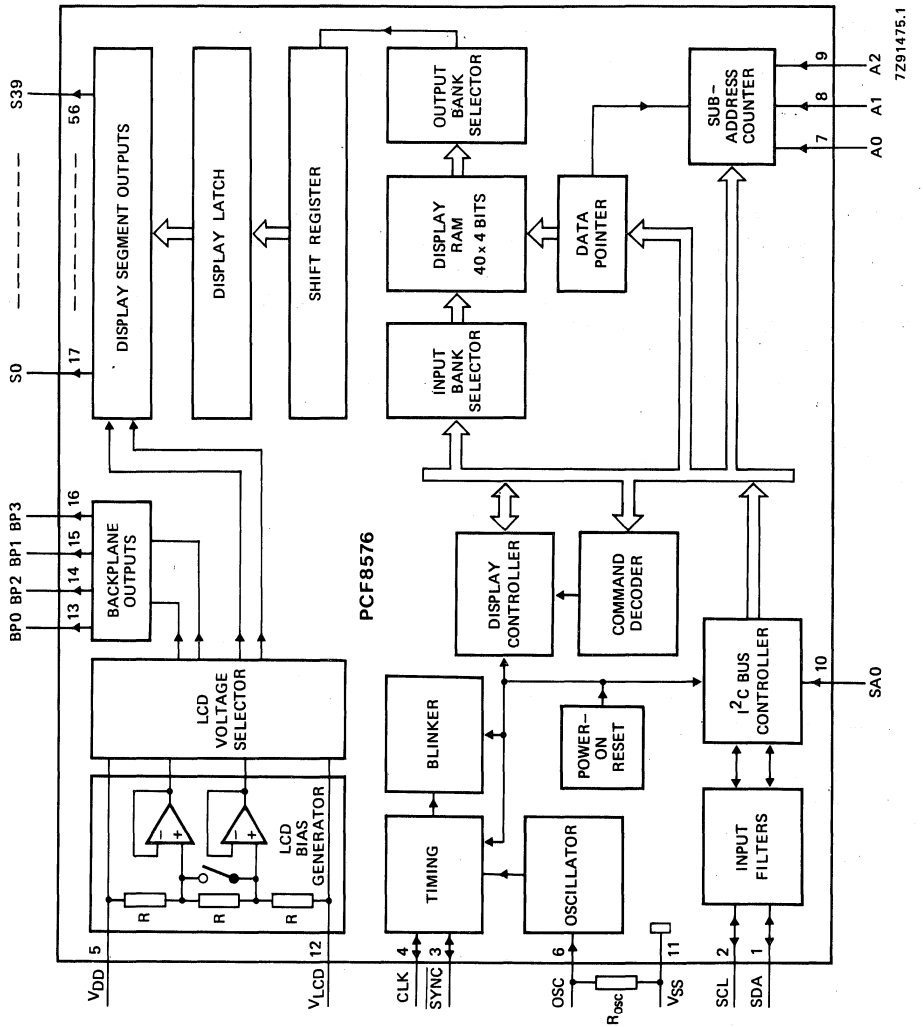


Fig.1 Block diagram; VSO56; SOT190.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

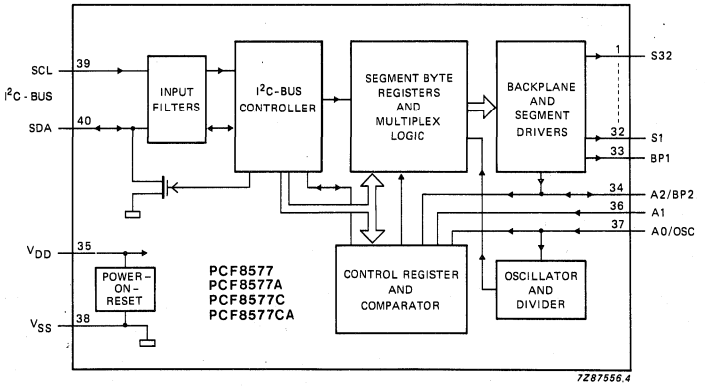


Fig.1 Block diagram.

PAKCAGE OUTLINES

PCF8577P, PCF8577AP PCF8577CP, PCF8577CAP	40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	in blister tape.
PCF8577U/5 PCF8577CU/5	wafer unsawn.
PCF8577U/10 PCF8577CU/10	chip on film-frame-carrier (FFC).

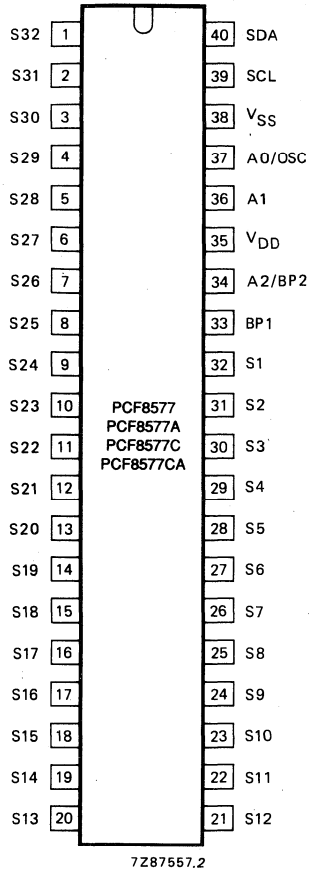


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I²C-bus

40	SDA	I²C-bus data line
39	SCL	I²C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

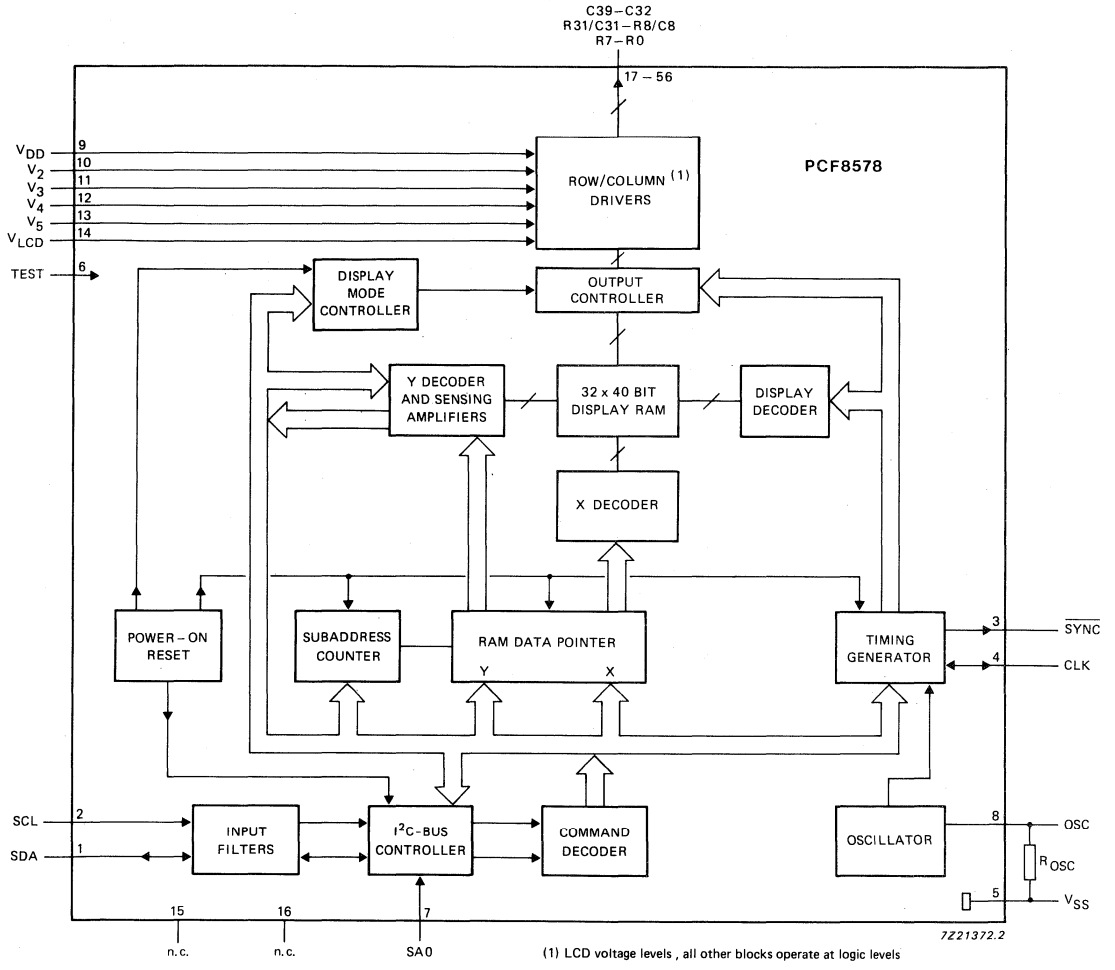


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

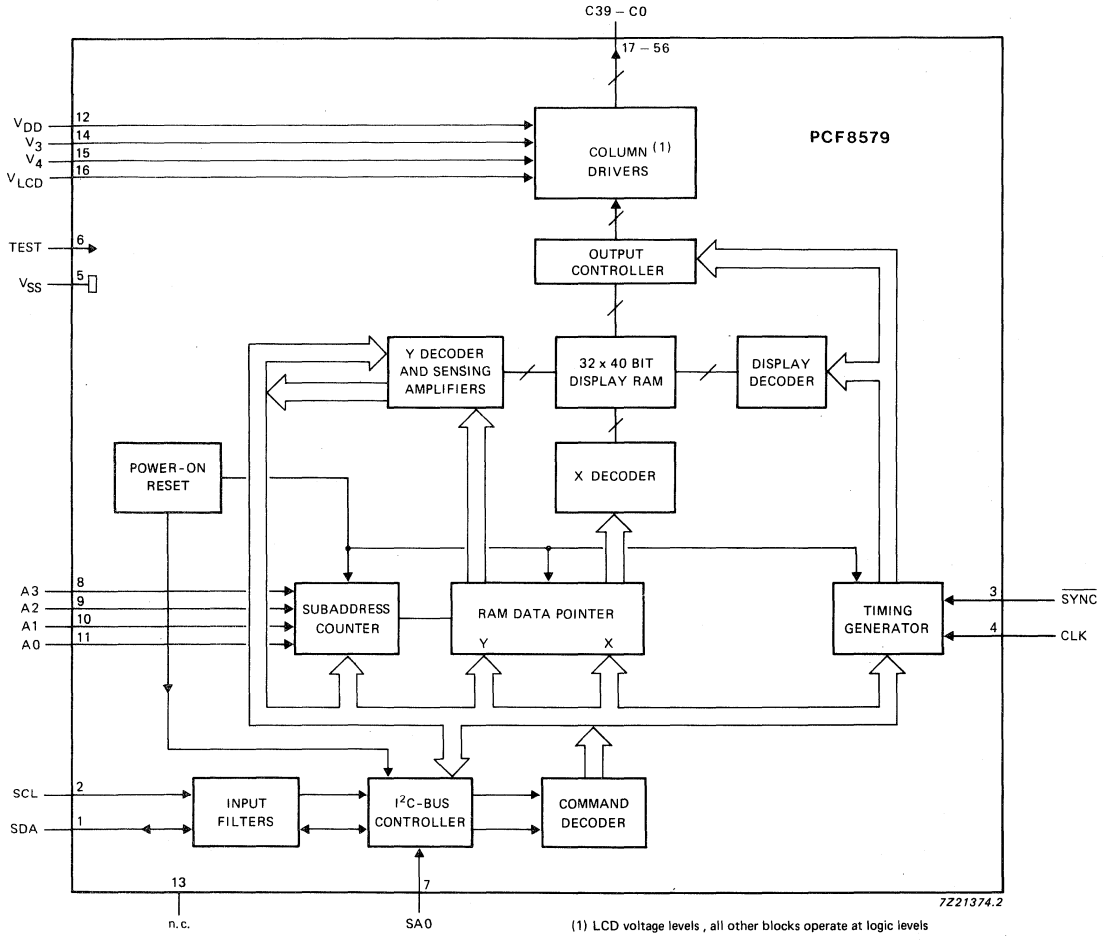


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO8L; SOT176C).

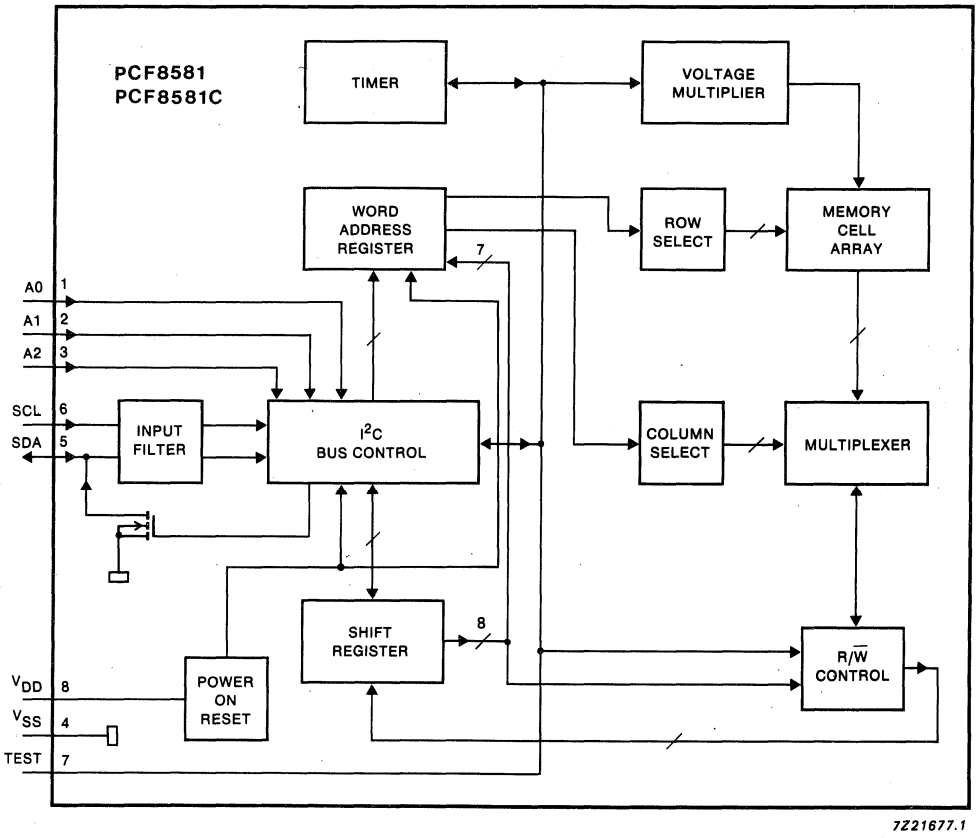


Fig.1 Block diagram.

CLOCK CALENDAR WITH 256 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1.0 V to 6 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

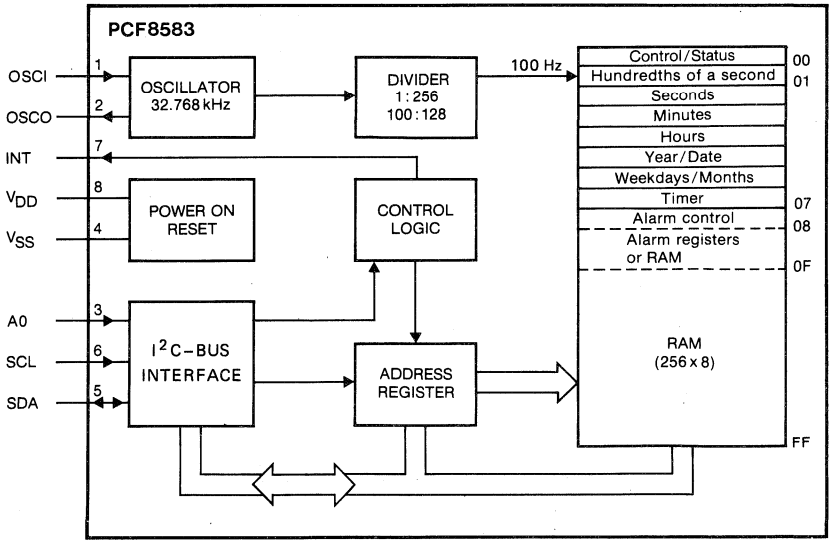


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176A).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C-bus
6	SCL	serial clock line	I^2C-bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

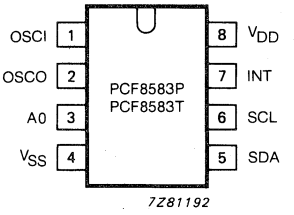


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.8	+ 7.0	V
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	–	50	mA
Input voltage range	V_I	−0.8 to V_{DD}	+ 0.8	V
DC input current	I_I	–	10	mA
DC output current	I_O	–	10	mA
Power dissipation per package	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

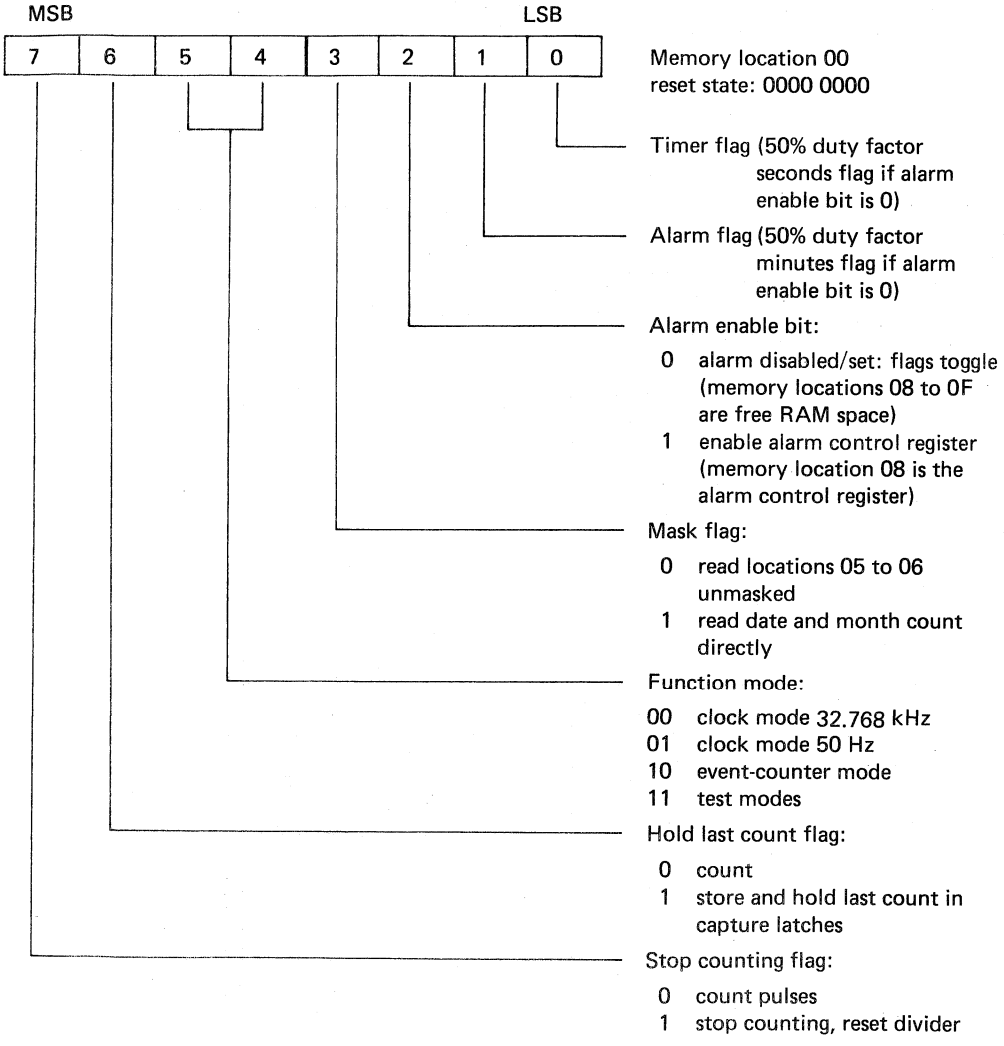


Fig.3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

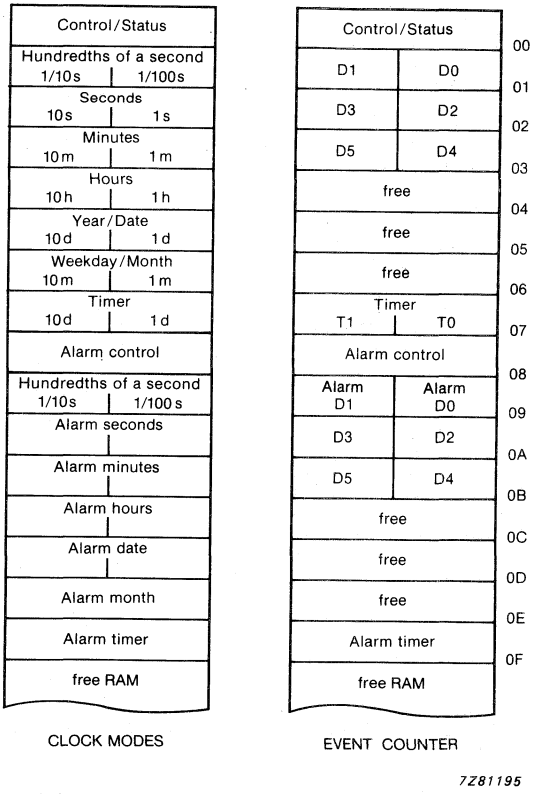
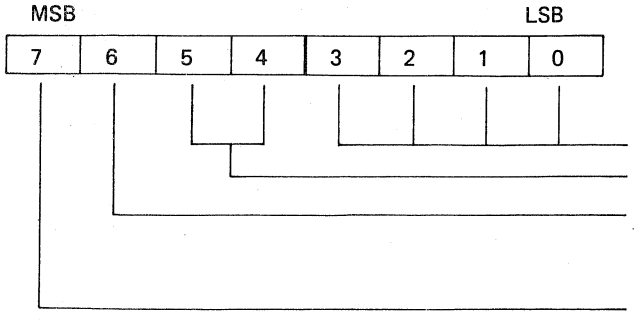


Fig.4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

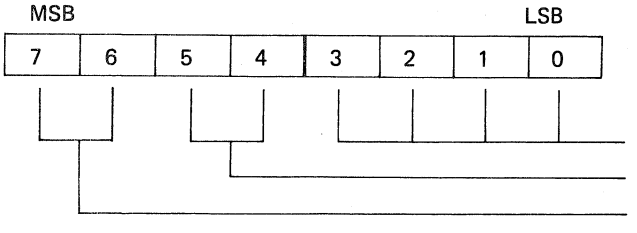
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig.5 Format of the hours counter.



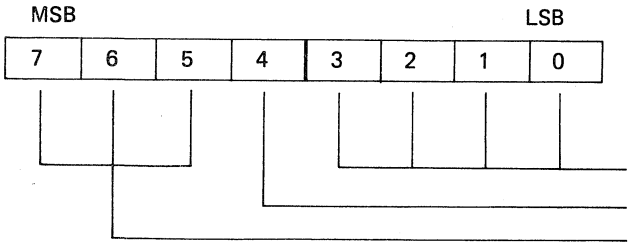
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig.6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

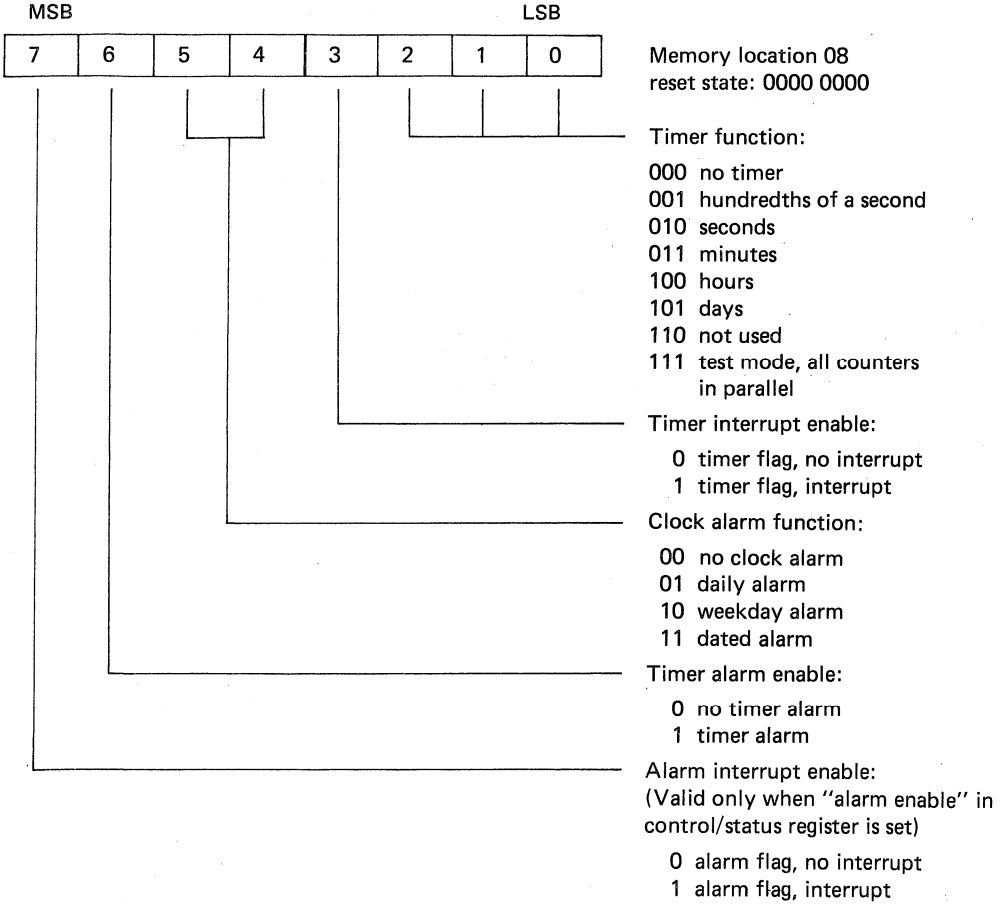


Fig.8a Alarm control register, clock modes.

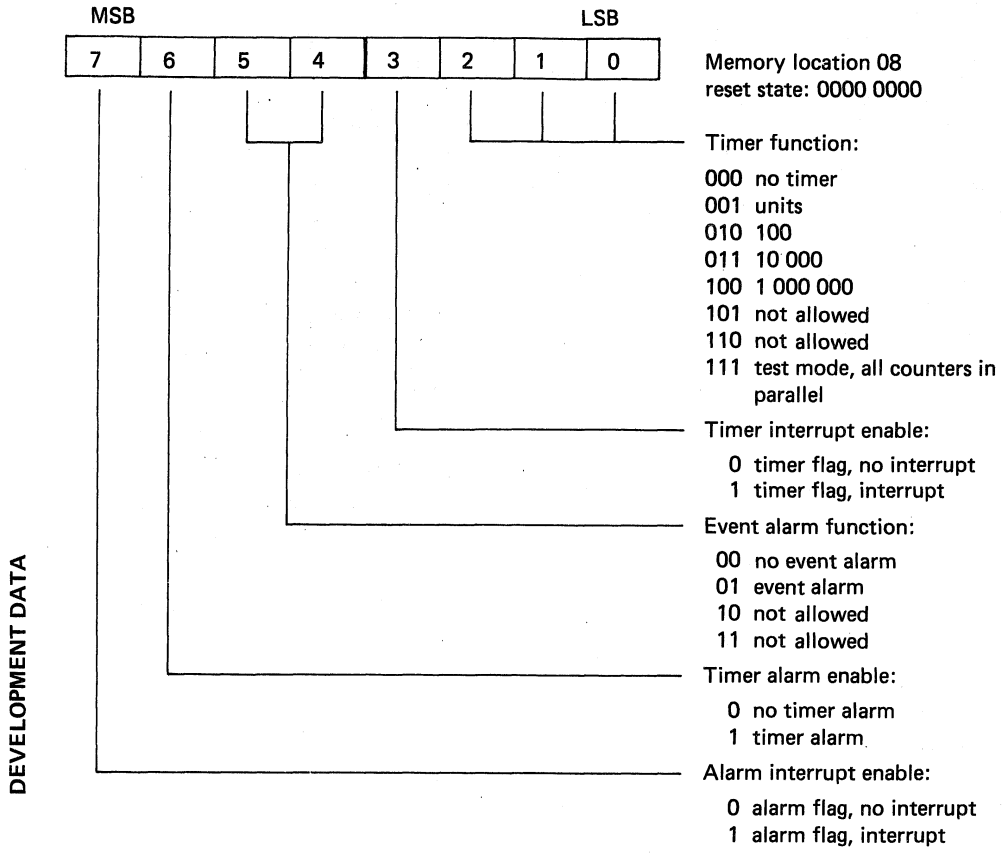


Fig.8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Note: In the 12 h mode bits 6 and 7 of the alarm hours register must be the same as the hours counter.

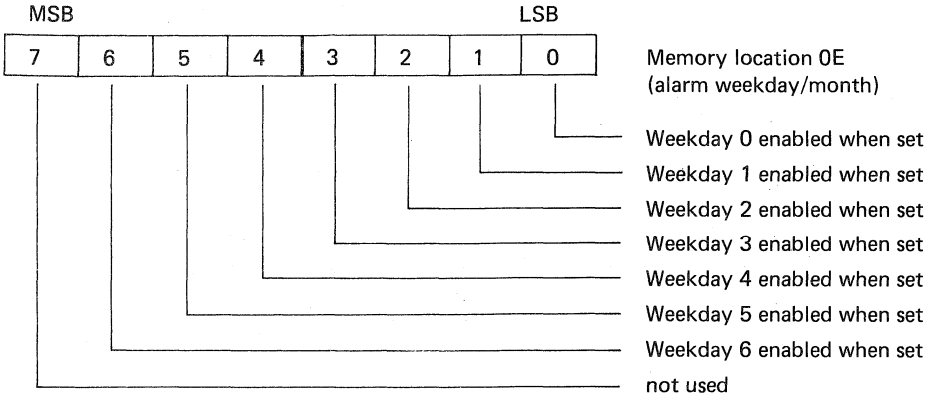


Fig.9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I²C-bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. 1 Hz is output at the interrupt (starts HIGH). This can be disabled by setting the alarm enable bit in the control/status register.

A second level-sensitive reset signal to the I²C-bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

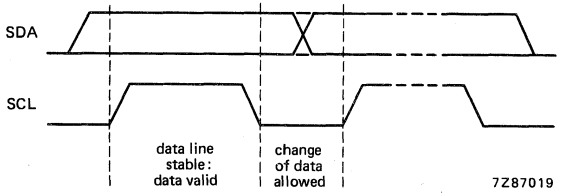


Fig.10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

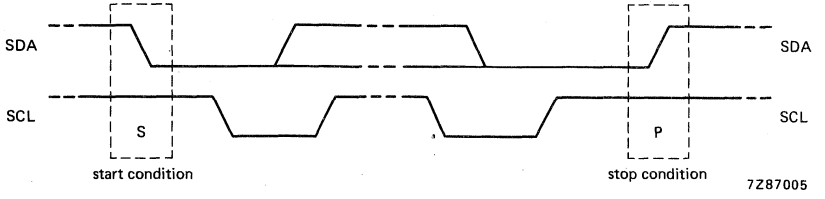


Fig.11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

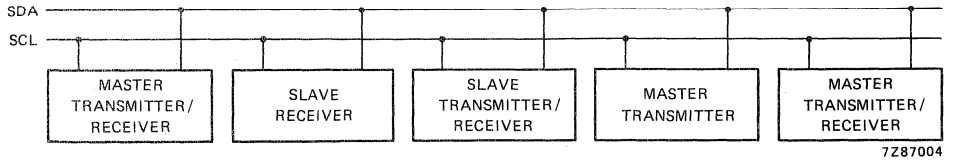


Fig.12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

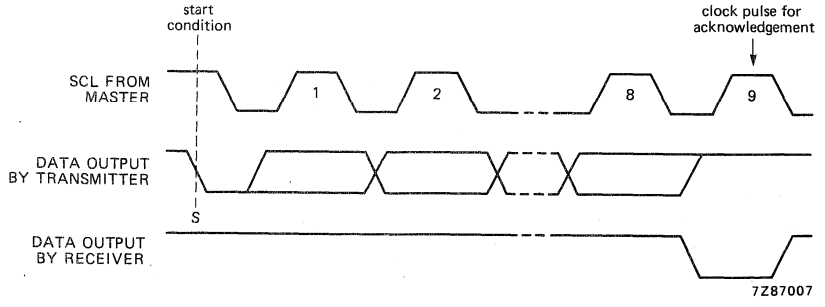


Fig.13 Acknowledgement on the I^2C-bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

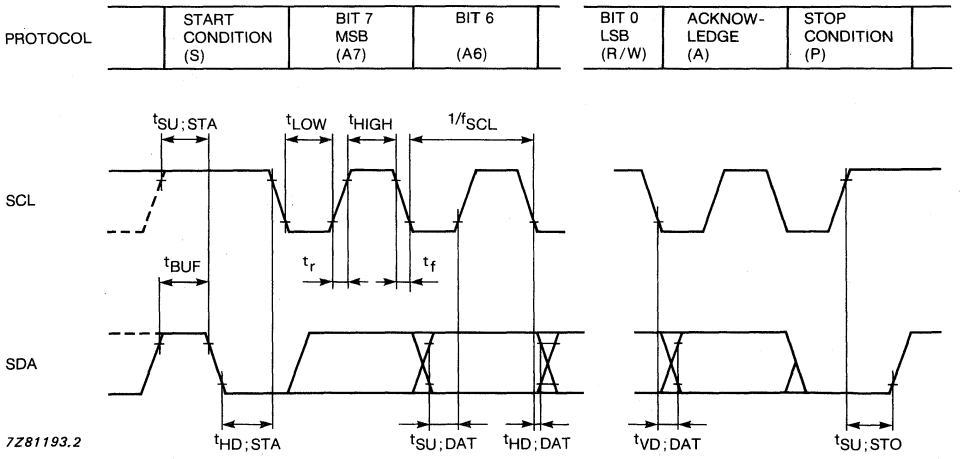


Fig. 14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig.15.

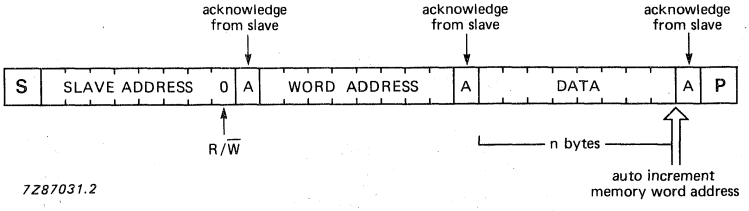


Fig.15a Master transmits to slave receiver (WRITE mode).

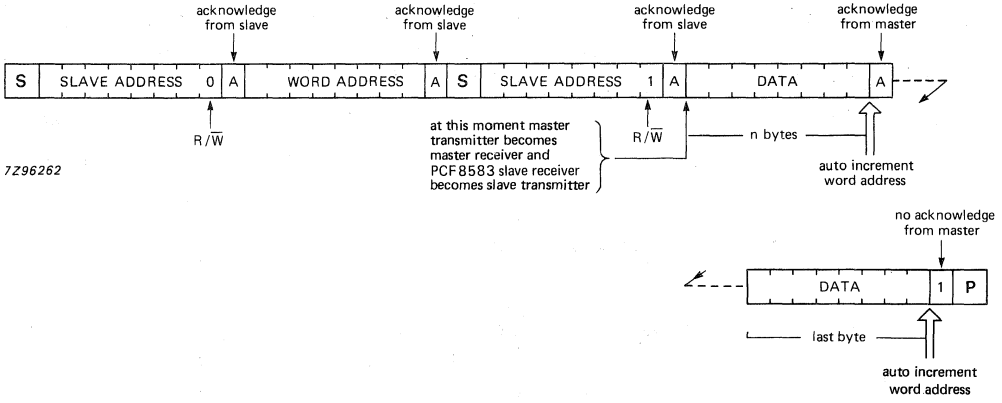


Fig.15b Master reads after setting word address (WRITE word address; READ data).

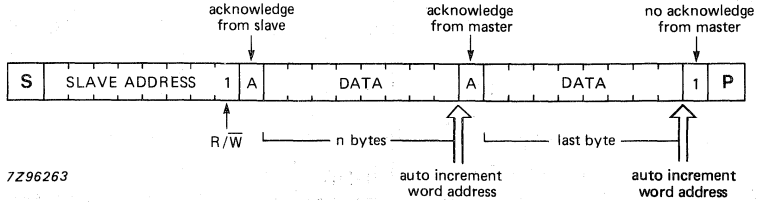


Fig.15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
operating		V_{DD}	2.5	–	6.0	V
clock	T_{amb} = 0 to + 70 °C	V_{DD}	1.0	–	6.0	V
Supply current						
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
clock	V_{DD} = 5 V	I_{DDO}	–	10	50	μA
clock	V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs; Input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	$0.3V_{DD}$	V
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
A0; OSCI						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	250	nA
SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
Output INT						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	note 3					
	V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C;	I_{DDR}	–	–	5	μA
	V_{DDR} = 1 V	I_{DDR}	–	–	2	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OSC}	–	40	–	pF
Oscillator stability for ΔV_{DD} = 100 mV	T_{amb} = 25 °C; V_{DD} = 1.5 V	f/fOSC	–	2×10^{-7}	–	
Input frequency	note 4	f_i	–	–	1	MHz
Quartz crystal parameters						
Frequency = 32.768 kHz						
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.
3. Event or 50 Hz mode only (no Quartz).
4. Event mode only.

APPLICATION INFORMATION

Quartz frequency adjustment

Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ± 5 x 10^{-6}). Average deviations of ± 5 minutes per year can be achieved.

Method 2: OSCI Trimmer

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

Power-on
Initialization (alarm function)

Routine:

Set clock to time T and set alarm to time T + dT.
At time T + dT (interrupt) repeat routine.

If time dT is approximately 10 ms a frequency of approximately 40 Hz is obtained.

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

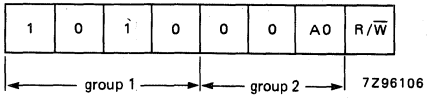
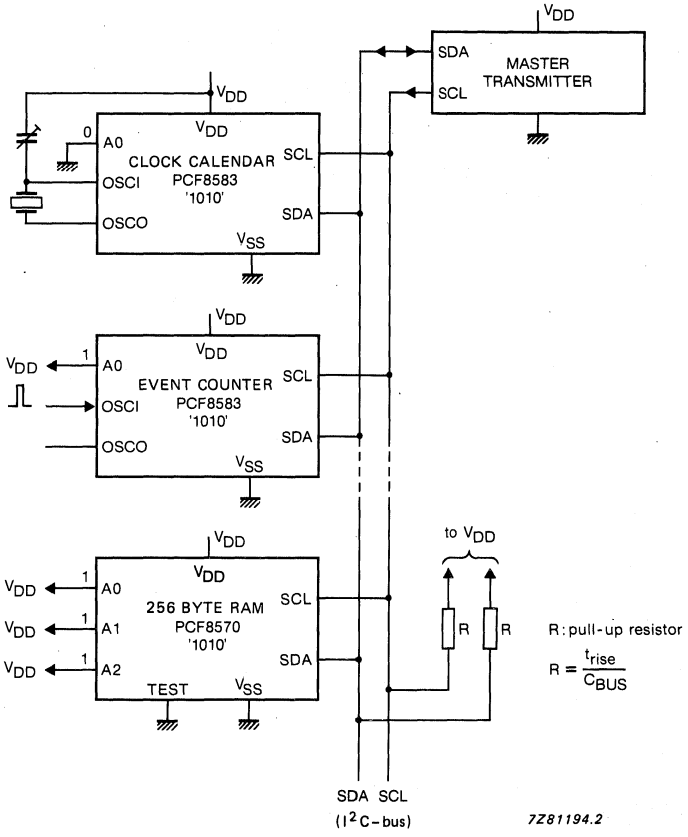


Fig.16 PCF8583 address.



Recommendation:
Connect a 4.7 μF 10 V solid aluminium (SAL) capacitor between V_{DD} and V_{SS}.

Fig.17 PCF8583 application diagram.

DEVELOPMENT DATA

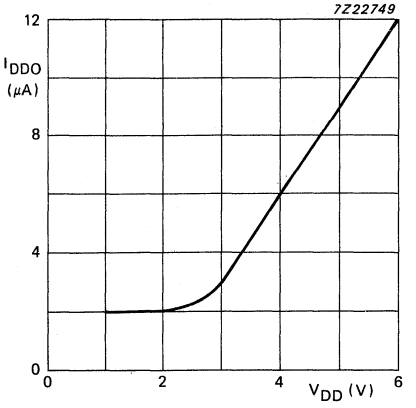


Fig.18 Typical supply current as a function of supply voltage (clock); $T_{amb} = -40$ to $+85$ °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

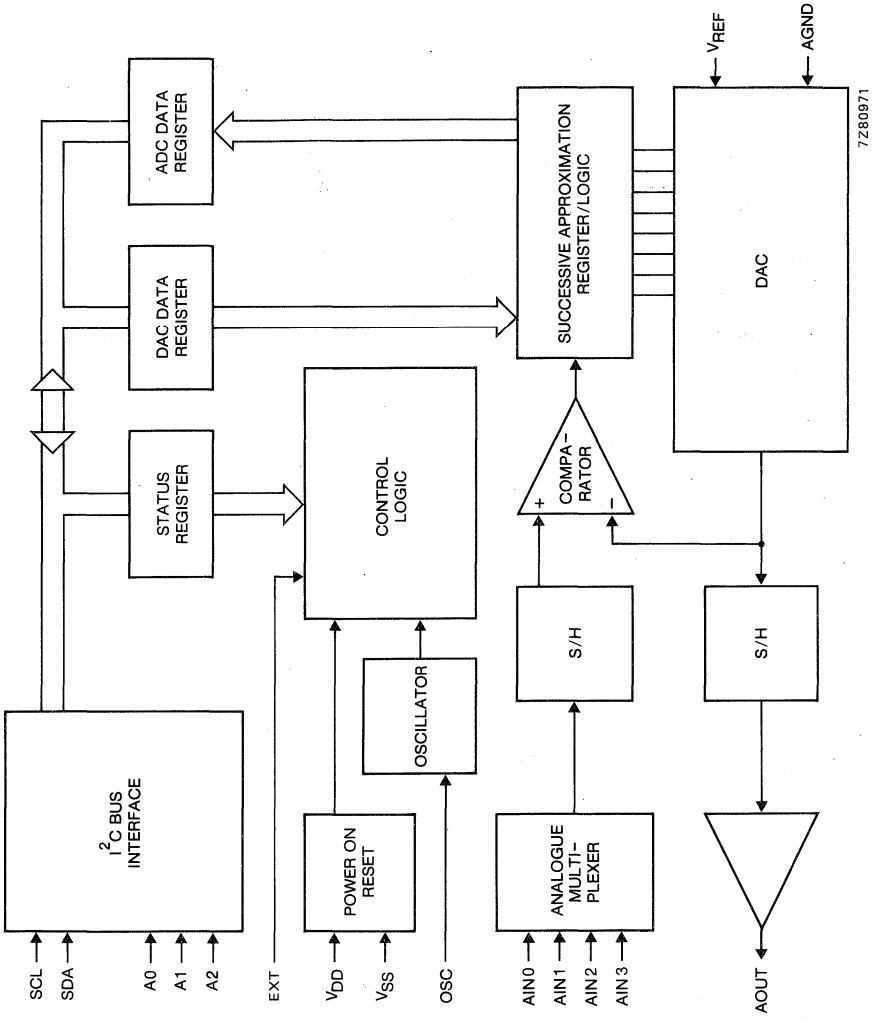


Fig. 1 Block diagram.

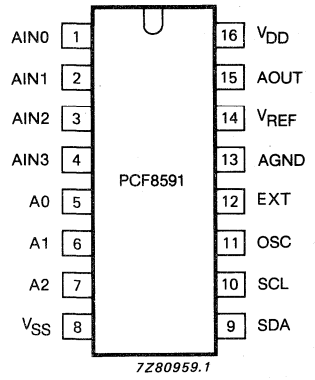


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

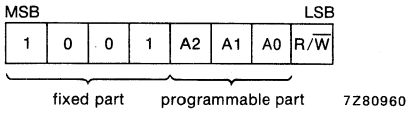


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

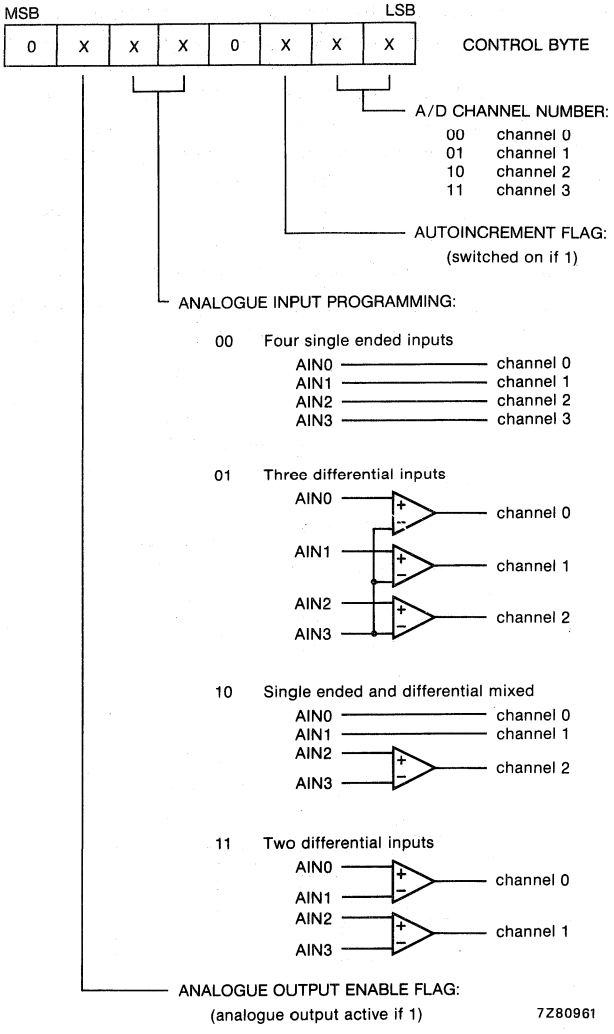


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

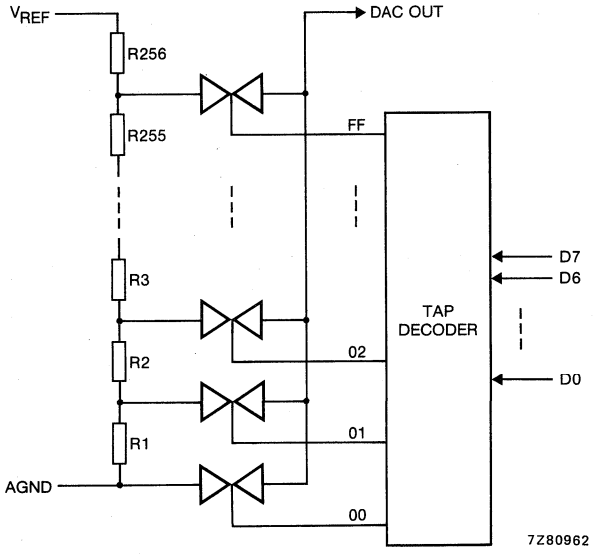


Fig. 5 DAC resistor divider chain.

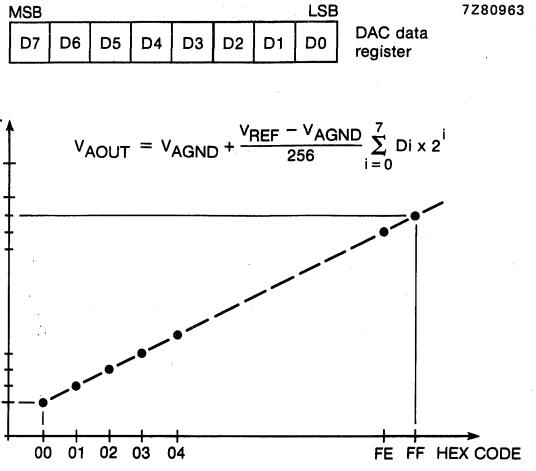


Fig. 6 DAC data and d.c. conversion characteristics.

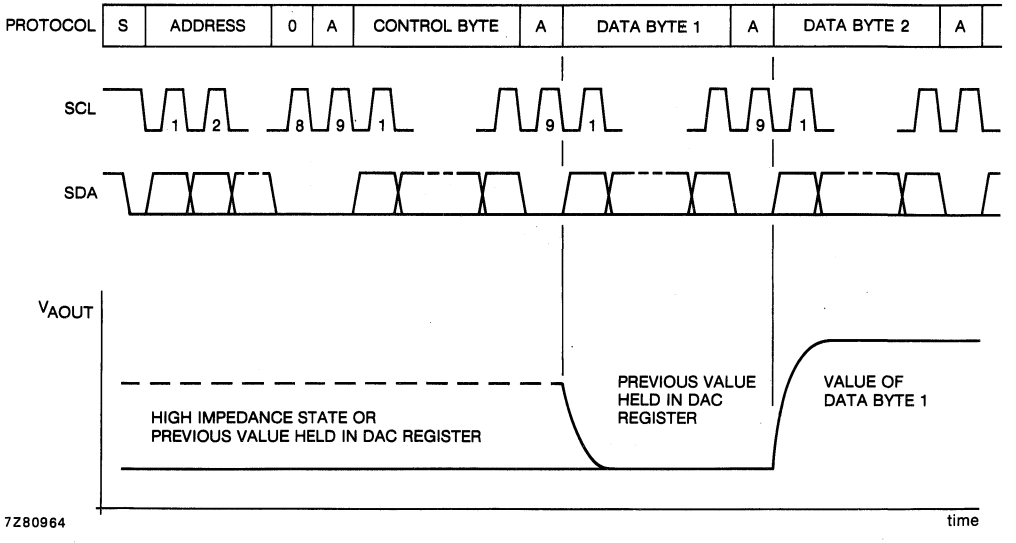


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

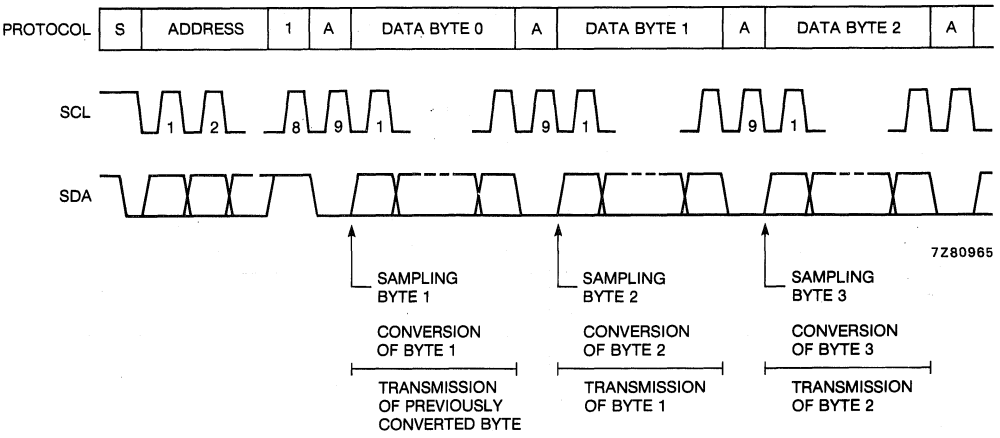


Fig. 8 A/D conversion sequence.

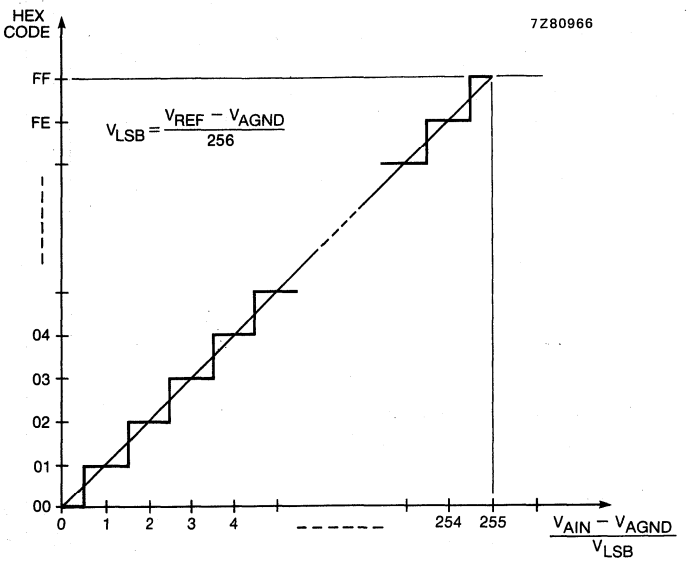


Fig. 9a A/D conversion characteristics of single-ended inputs.

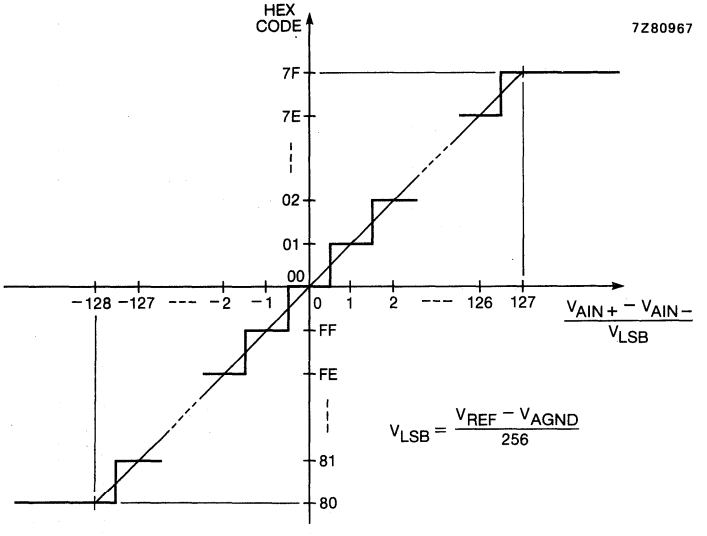


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

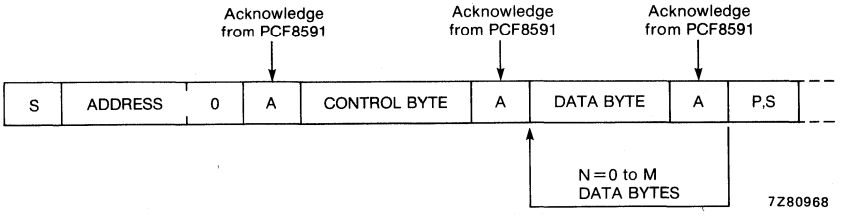


Fig. 10a Bus protocol for write mode, D/A conversion.

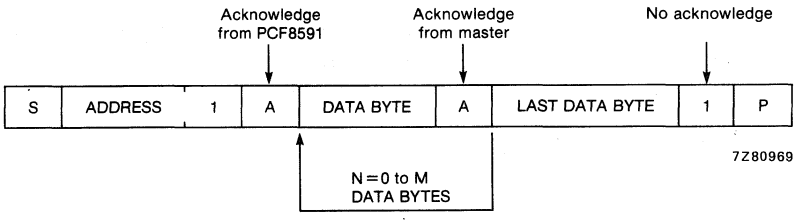


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

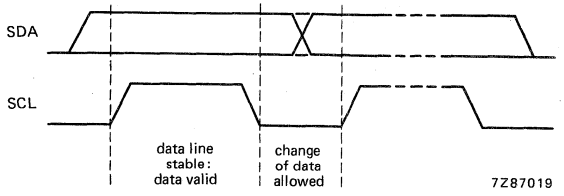


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

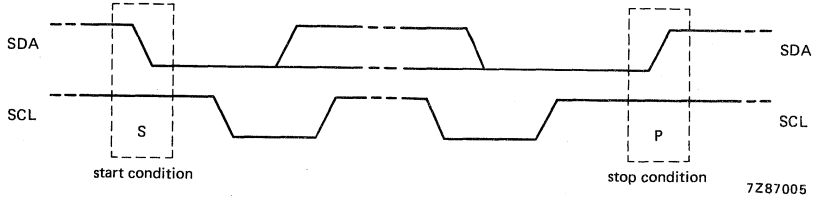


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

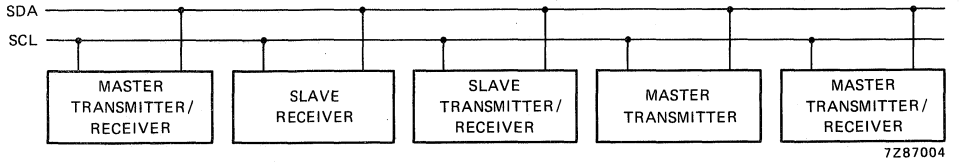


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

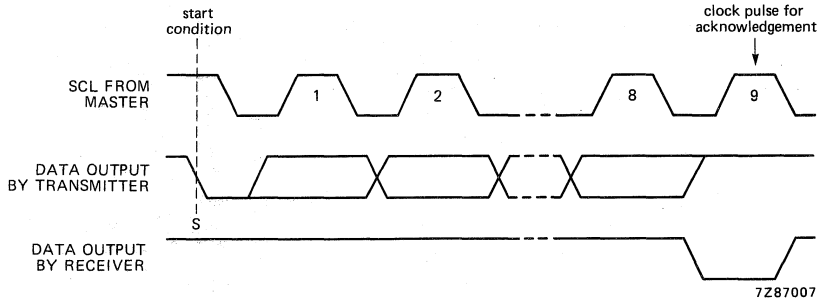


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,0	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

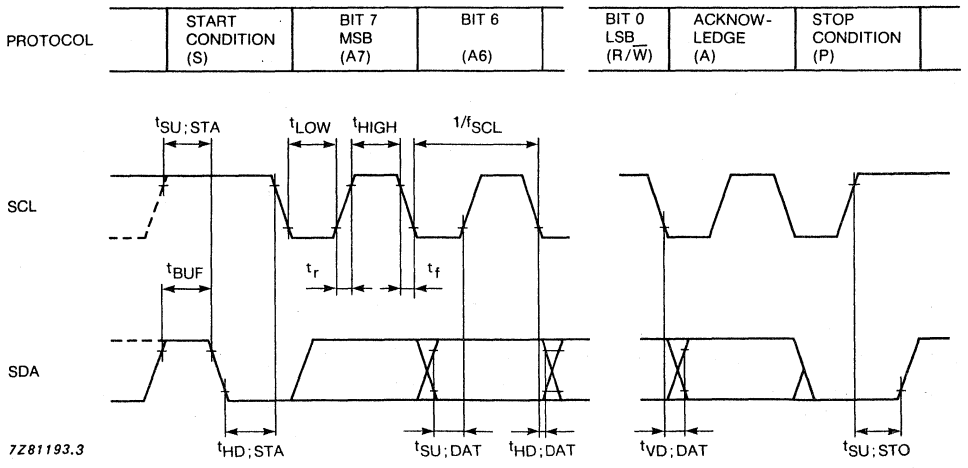


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Leakage current A0–A2	V_I = V_{SS} to V_{DD}	$\|I_L\|$	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
Leakage current SCL, SDA	V_I = V_{SS} to V_{DD}	$\|I_L\|$	–	–	1	μA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8 \text{ V and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4 \text{ V.}$$

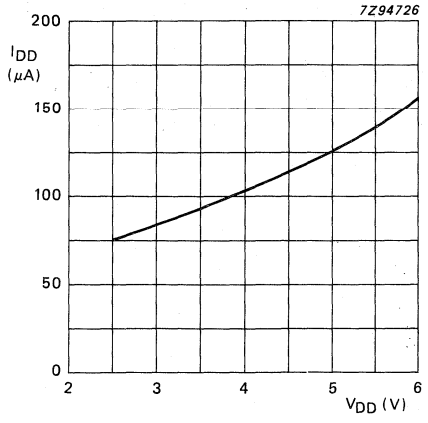
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

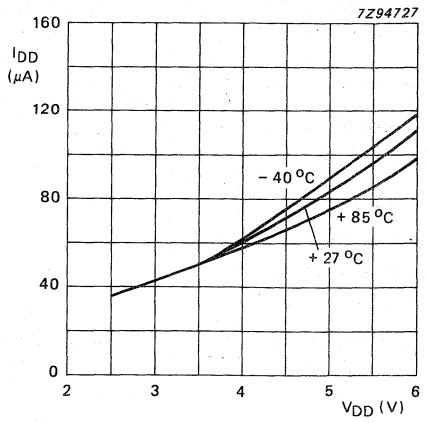
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



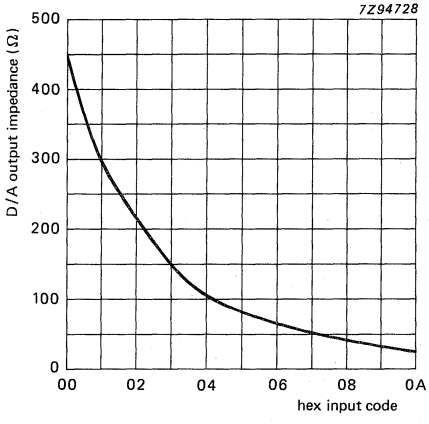
(a) internal oscillator; T_{amb} = + 27 °C.



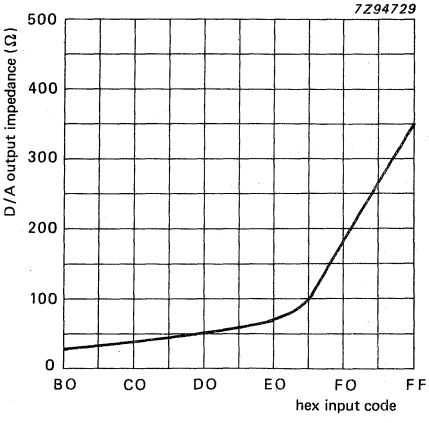
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

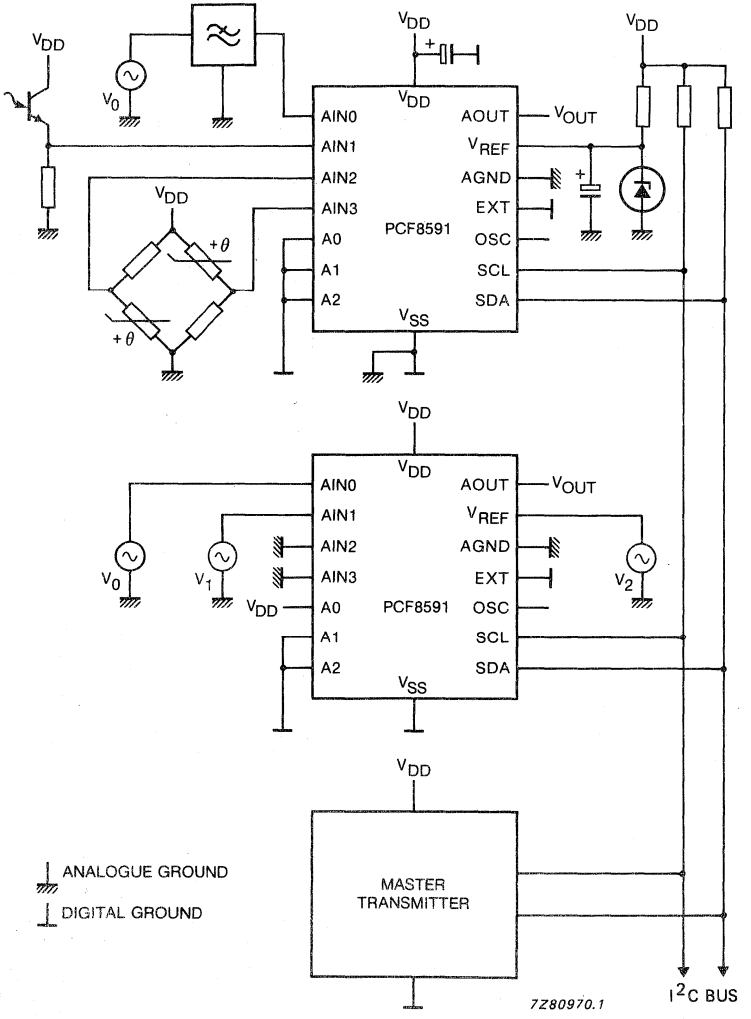


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

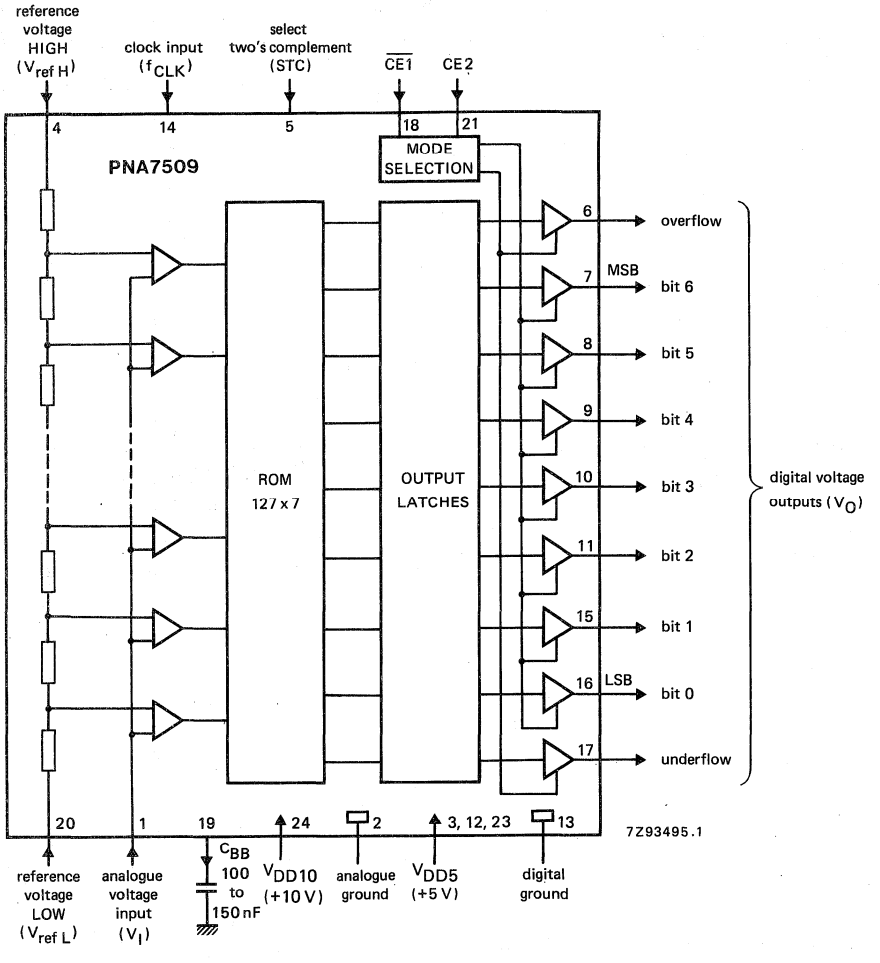
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)		V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)		V_{refH}	5,0	5,1	5,2	V
Non-linearity	f_i = 1,1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

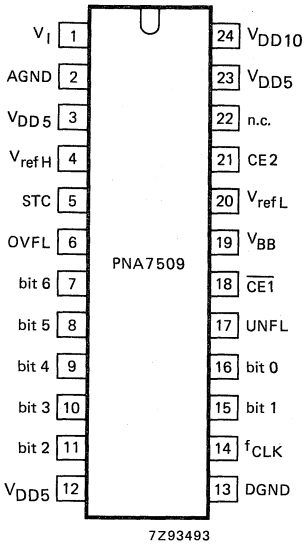


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ to 10,5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH (note 1)	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5,0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0,4	V
Output voltage HIGH at $-I_O$ = 0,5 mA	V_{OL}	2,4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2,50 V; V_{refH} = 5,08 V)

step	$V_{1\text{-}2}$ (1)	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2,51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2,51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2,53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
126	5,03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5,05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5,07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2-125

DEVELOPMENT DATA

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE\ 1}$	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 4{,}5$ V to 5,5 V; $V_{DD10} = V_{24-2} = 9{,}5$ V to 10,5 V; $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

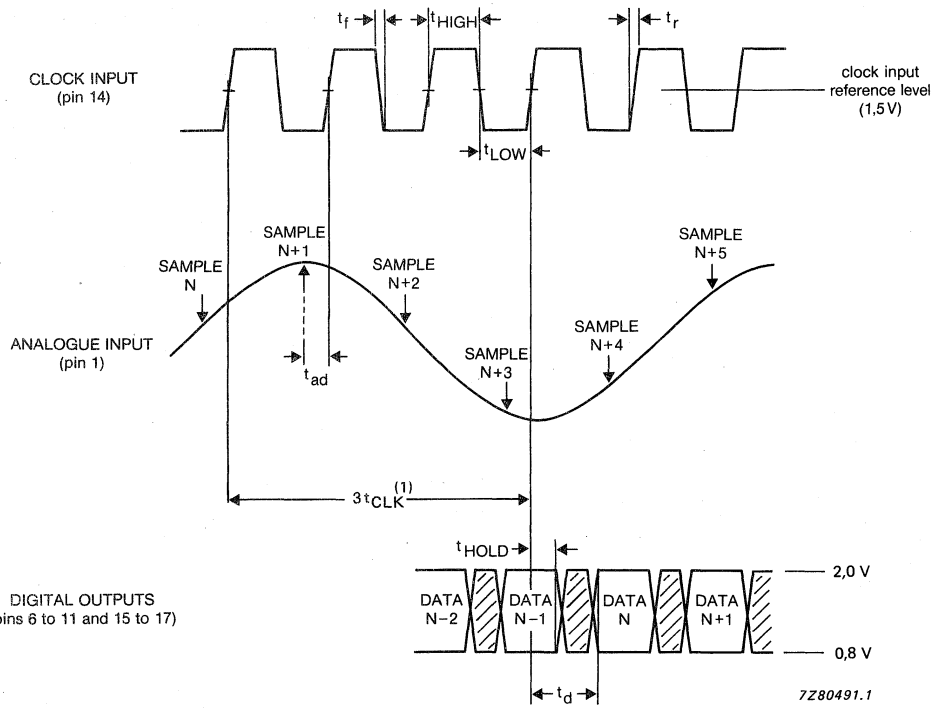
parameter	symbol	min.	max.	unit
Switching characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	3	ns
fall time	t_f	–	3	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Differential gain (note 2)	dG	–	± 5	%
Differential phase (note 2)	d_p	–	± 2,5	deg
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise) (note 3)		–	3	LSB
Harmonics (full scale)				
fundamental (note 3)	f_0	–	0	dB
r.m.s. (2nd + 3rd harmonic)	$f_{2,3}$	–	–28	dB
r.m.s. (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	–35	dB

parameter	symbol	min.	max.	unit
Digital outputs (notes 1 and 4)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at C_L = 15 pF	t_d	–	38	ns
Output delay time at C_L = 50 pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at f_i = 1,1 kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sinewave (peak-to-peak value of the analogue input voltage at $V_{I(p-p)}$ = 1,8 V) combined with a sinewave voltage ($V_{I(p-p)}$ = 0,7 V) at f_i = 5 MHz.
3. Analogue frequency $f_{i(A)}$ = 5 MHz
   Amplitude $V_{i(A)}$ = 2.42 V (peak-to-peak value).
4. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

DEVELOPMENT DATA



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION NOTE

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V, T_{amb} = 22 °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1,5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching). Even a spike duration of less than 1 μs can destroy the device.

DEVELOPMENT DATA

APPLICATION NOTE (continued)

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Fig. 5, 6, 7 and 8).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.

After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.

To calculate differential non-linearity a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation (Fig. 7).

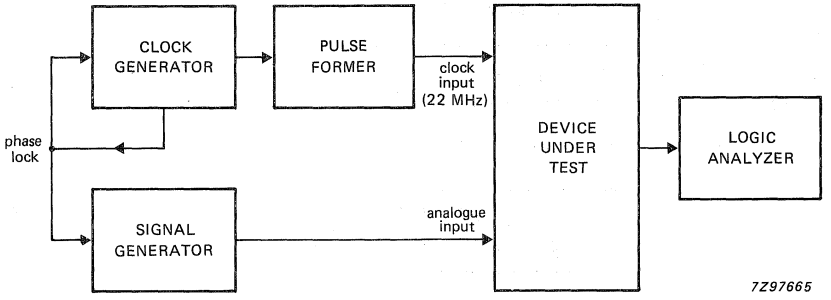
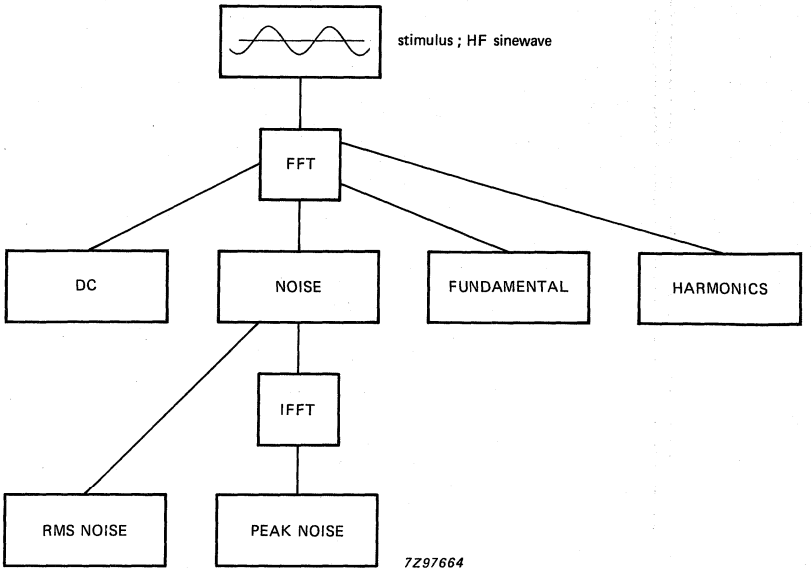


Fig. 4 Analogue-to-digital converter testing with locked signal source.



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.

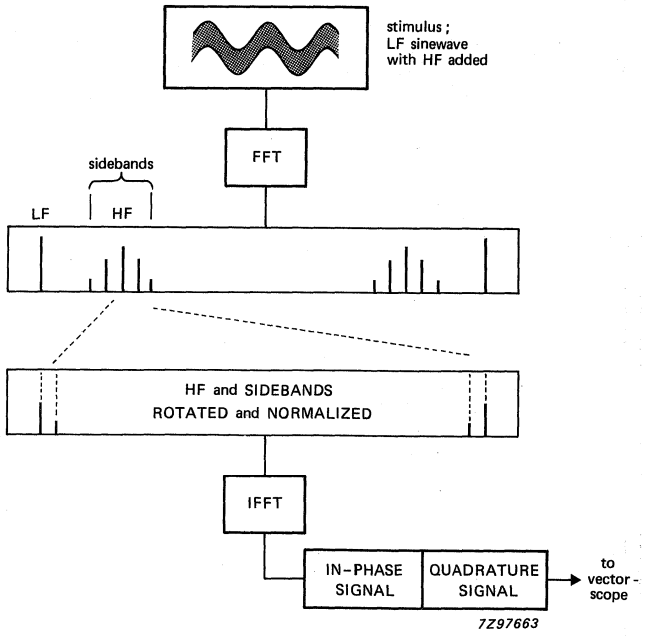
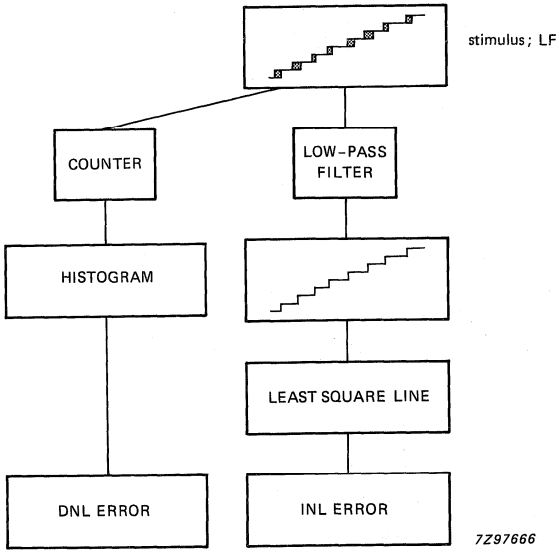


Fig. 6 Differential gain and phase.

APPLICATION NOTE (continued)



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 7 Low frequency ramp test; linearity.

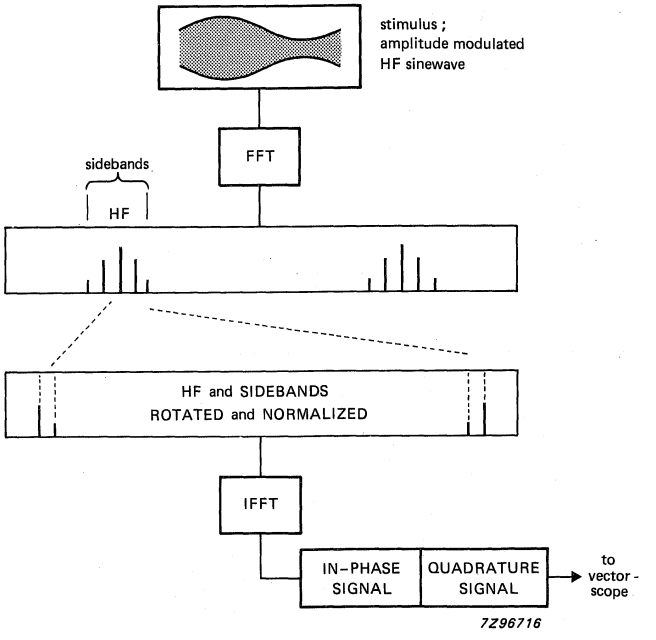


Fig. 8 Large signal phase error.

8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain. The multiplying capability is obtained by using the independent reference voltages.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected. STC inverts the most significant bit (MSB).

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB
- Multiplying capability
- 12 MHz bandwidth
- 8-bit resolution

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Reference voltage LOW		V_{refL}	0	–	2,0	V
Reference voltage HIGH		V_{refH}	0	–	2,0	V
Static non-linearity	note 1		–	–	± 0,5	LSB
Bandwidth at –3 dB	note 2	B	12	–	–	MHz
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Total power consumption		P	–	–	470	mW

For explanation of notes see "Notes to the characteristics".

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38D)

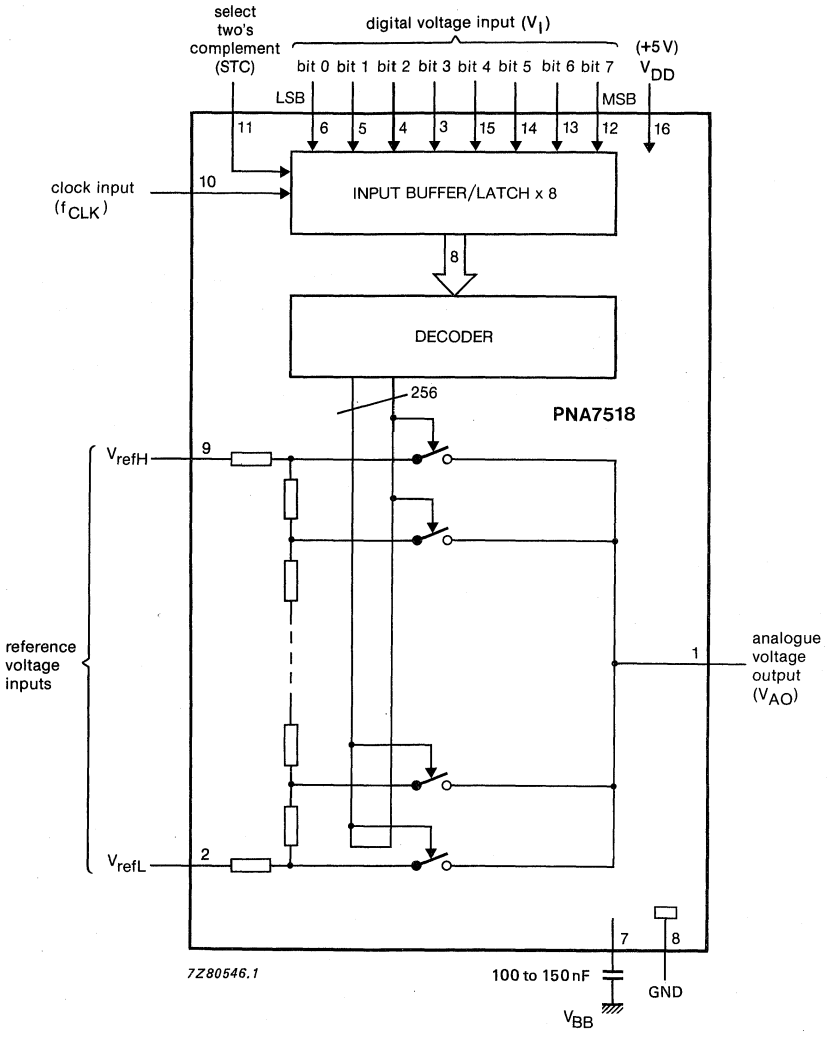


Fig. 1 Block diagram.

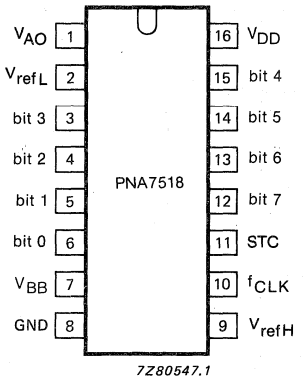


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	GND	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,5	7,0	V
Input voltage B0 to B7 and STC	V_I	−0,5	7,0	V
Output voltage	V_{AO}	−0,5	7,0	V
Total power dissipation	P_{tot}	–	800	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Temperature range with back bias	T_{BB}	−10	+ 80	°C
Clock frequency	f_{CLK}	10	–	kHz

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Inputs B0 to B7, CLK, and STC						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input leakage current (except STC)		I_{LI}	–	–	10	μA
STC input current		I_I	–	–	100	μA
Reference voltages						
Reference voltage LOW		V_{refL}	0	–	2	V
Reference voltage HIGH		V_{refH}	0	–	2	V
Reference ladder between V_{refL} and V_{refH}		R_{ref}	150	–	300	Ω
Linearity						
Static non-linearity	note 1		–	–	± 0,5	LSB
Clock input						
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Bandwidth						
Bandwidth at –3 dB	note 2	B	12	–	–	MHz

Notes to the characteristics

1. Measured at R_{AO} = 200 kΩ; V_{refL} = 0 V; V_{refH} = 2 V and f_{CLK} = 28 MHz.
2. Measured at V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2 V; f_{CLK} = 30 MHz; duty cycle = 0,5; rise and fall time = 3 ns and a 6 pF load at the analogue output. The analogue output signal is scanned by an external sample and hold circuit.

APPLICATION INFORMATION

This section provides additional information to the characteristics. The values are measured on a sampling basis.

Table 1 Application characteristics

parameter	symbol	typ.	unit
Supply current	I_{DD}	50	mA
Power consumption	P	270	mW
Minimum clock frequency	f_{CLK}	10	kHz
Maximum clock frequency	f_{CLK}	45	MHz
Static non-linearity		± 0,25	LSB
Reference ladder	R_{ref}	210	Ω
Bandwidth	B	15	MHz
Set-up time	t_{SU}	3	ns
Input hold time	t_{HD}	4	ns
Propagation delay	t_{PD}	$1 \times t_{CLK} + 30$	ns

Where:

V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2,0 V.

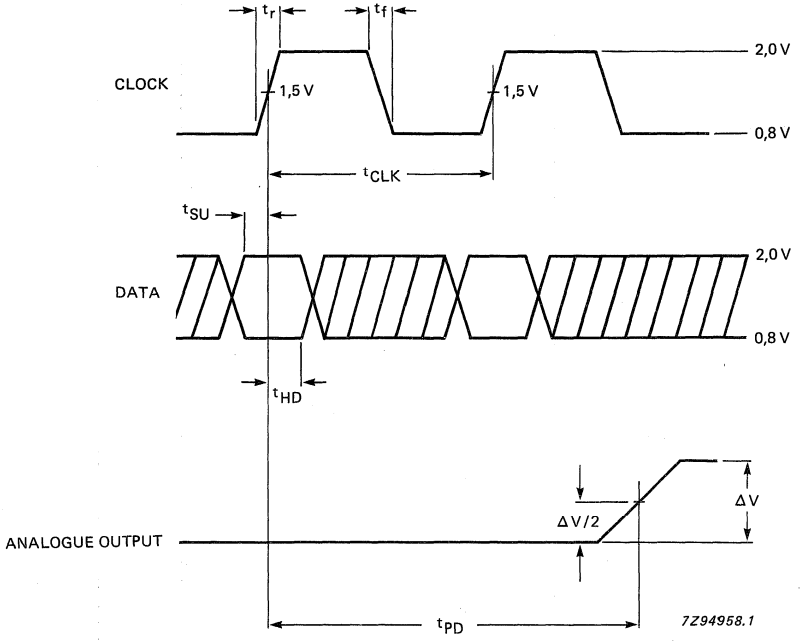


Fig. 3 Switching characteristics.

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM1, SECAM2, PAL/CCIR, NTSC1, NTSC2 and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 28)	V_{DD}	5.7	–	7.5	V
Supply current range (quiescent)	I_{DD}	–	–	10	μA
Oscillator frequency	f_{OSC}	–	–	5.1	MHz
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINES

SAA1043 : 28-lead DIL; plastic (SOT117).
SAA1043T: 28-lead mini-pack; plastic (SO28; SOT136A).

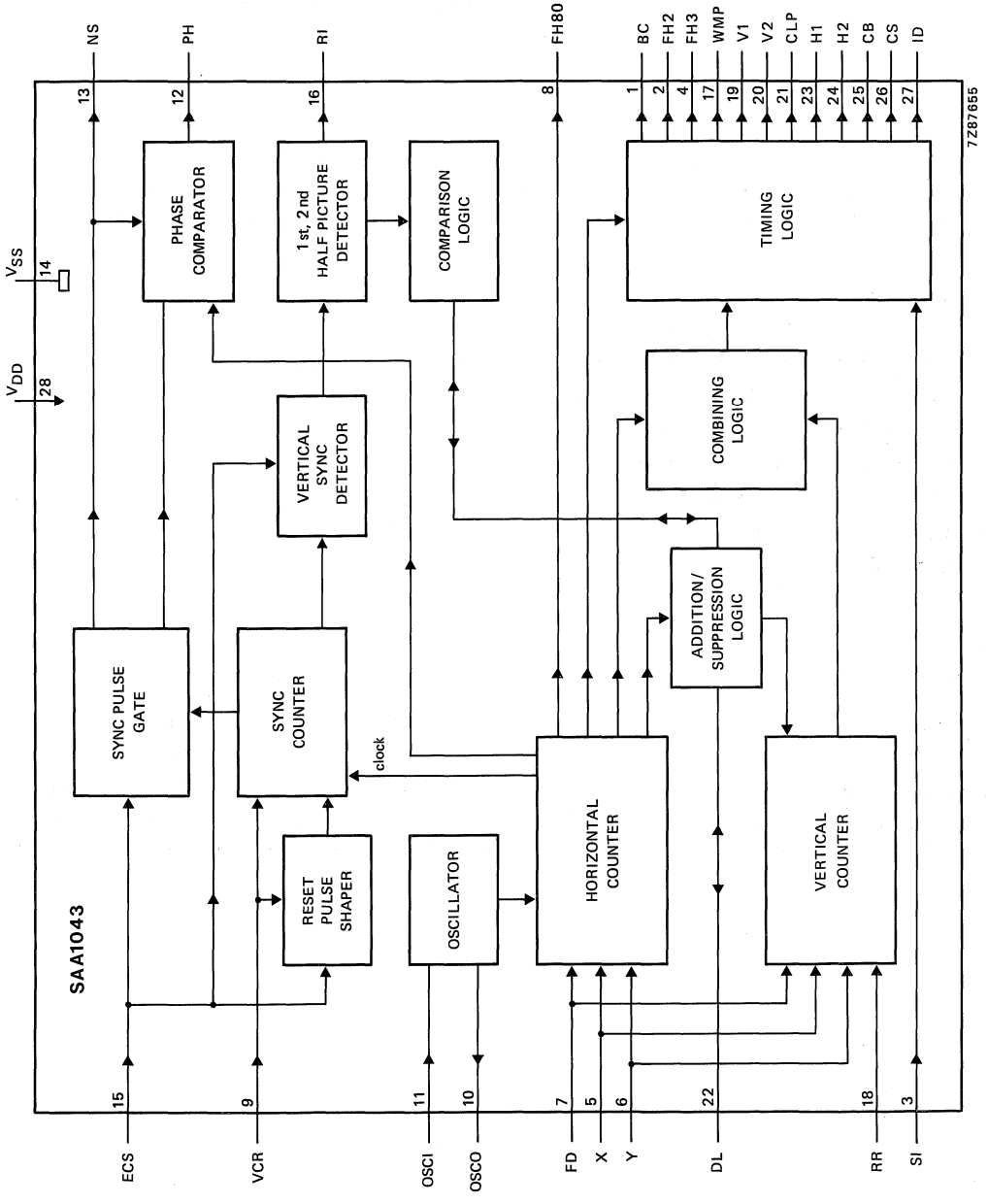


Fig. 1 Block diagram.

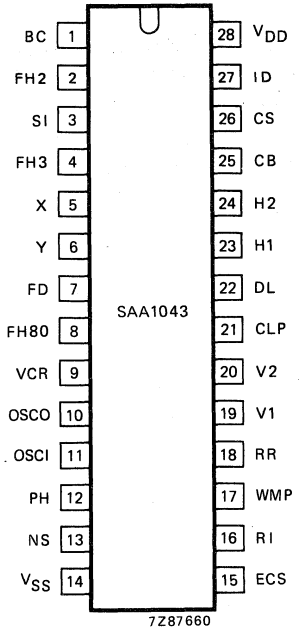


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chrominance blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1.25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

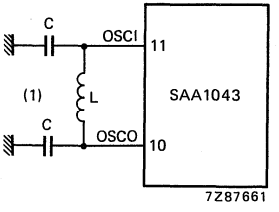
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

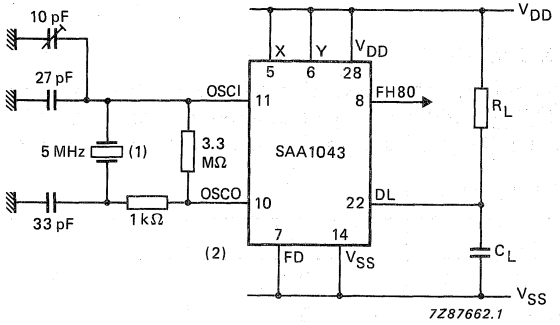
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5.0	0	50	15625
NTSC, PAL-M, 524	5.034964	1	59.94	15734.26
PAL, SECAM, 624	2.5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2.51782	H1 (pin 23)	59.94	15734.26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

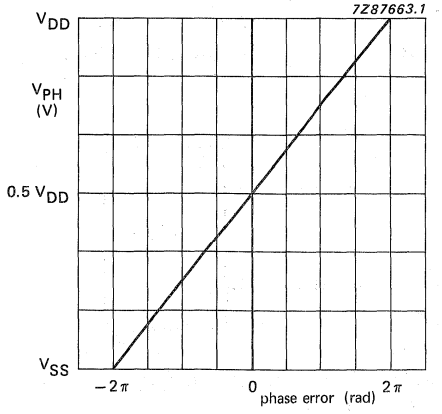


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15.2 <$ reset time $< 64 + 15.2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6.4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Vertical reset input (RR)

The RR is used when external synchronization runs on separate vertical (V) and horizontal (H) pulses instead of composite sync (CS) pulses.

- RR = LOW : no external sync or external CS to ECS input
- RR = V-pulses: external sync with H and V requires H-pulses to ECS input
  duration of H-pulse < 5 μs
  duration of V-pulse 1 μs $< t_V < 3$ μs

VCR standard input (VCR)

The VCR input sets the synchronization standard for VCRs.

- VCR = HIGH: normal mode

Then the ECS input expects a 64 μs ± 16 μs H-part of the CS pulse.
If the pulse fits inside the window, the SAA1043 will continue to take synchronizing pulses only inside the window.
If the pulse does not occur inside the window, the synchronizing circuit will take off the window and accept pulses at any time.

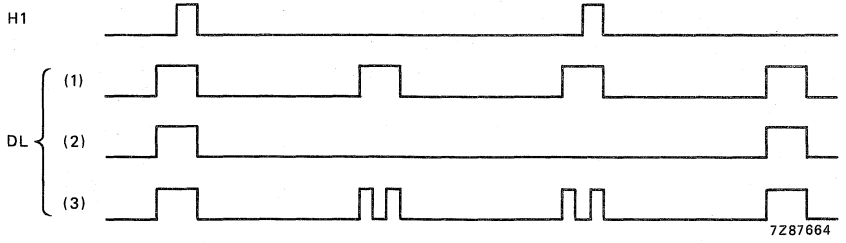
- VCR = LOW: VCR mode

The window ± 16 μs is always applied.

If the colour burst is not present in the correct position, or FH2 is not in phase with the incoming signal, the set identification input (SI) must be set to logic HIGH on line 2 for the duration of 1 line.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

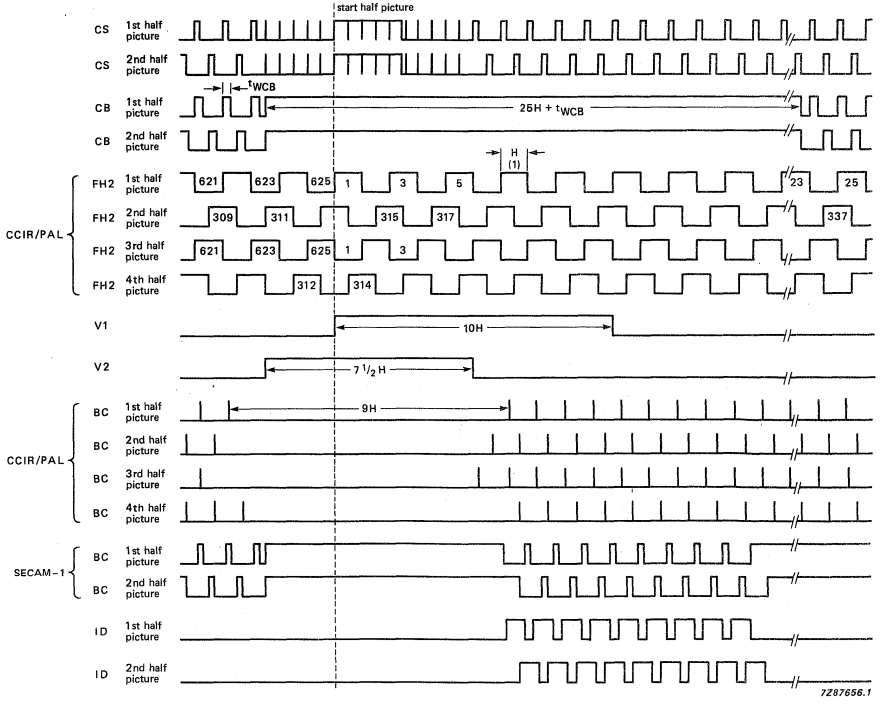
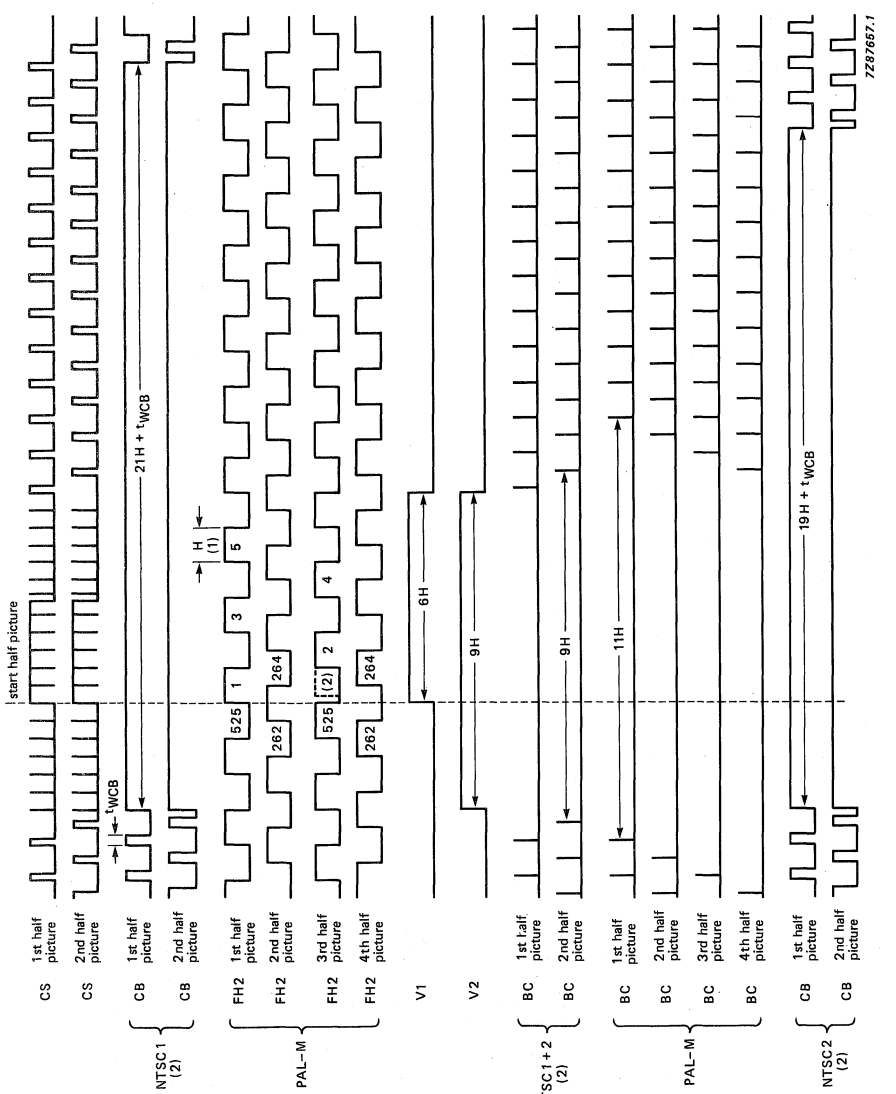


Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0.5 H subtracted from the waveform timing).



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0.5 H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from $n \times t_{OSCI} \pm 100$ ns. One horizontal scan (H) = $320 \times t_{OSCI} = 1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4.8	4.77	4.77	4.8	μs	24
Equalizing pulse width	t_{WSC2}	2.4	2.38	2.38	2.4	μs	8
Serration pulse width	t_{WSC3}	4.8	4.77	4.77	4.8	μs	24
Duration of pre-equalizing pulses		2.5	3	3	2.5	H	
Duration of post-equalizing pulses		2.5	3	3	2.5	H	
Duration of serration pulses		2.5	3	3.5	2.5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11.12	12	μs	60
NTSC 1	t_{WCB}	–	11.12	–	–	μs	56
NTSC 2	t_{WCB}	–	10.53*	–	–	μs	53
Front porch	t_{PCBCS}	1.6	1.59	1.59	1.6	μs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2.4	2.38	2.38	–	μs	12
Sync to burst delay	t_{PCSBC}	5.6	5.56	5.76	–	μs	28
Burst suppression		9	9	11	–	H	
Position of burst suppression: 1st half picture		H623 to H6	H523 to H6	H523 to H8	– –		
2nd half picture		H310 to H318	H261 to H269	H260 to H270	– –		
3rd half picture		H622 to H5	H523 to H6	H522 to H7	– –		
4th half picture		H311 to H319	H261 to H269	H259 to H269	– –		

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chrominance pulse width	t_{WBC}	–	–	–	7.2	µs	36
Chrominance to sync delay	t_{PBCCS}	–	–	–	1.6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture : 25H + t_{WBC} except H320 to H328 2nd half picture: 24.5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture : 25H + t_{WBC} 2nd half picture: 24.5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2.4	2.38	2.38	2.4	µs	12
Sync to clamp delay	t_{PCSCLP}	2.4	2.38	2.38	2.4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H		
Pulse width	t_{WDL}	9.6	9.53	9.53	9.6	µs	48
DL to sync delay	t_{PCLCS}	5.6	5.56	5.56	5.6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H		
Sync to FH80 delay		0.2	0.2	0.2	0.2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7.2	7.15	7.15	7.2	µs	36
H2 pulse width	t_{WH2}	7.2	7.15	7.15	7.2	µs	36
H1 to sync delay	t_{PH1CS}	0.8	0.79	0.79	0.8	µs	4
Sync to H2 delay	t_{PCSH2}	0.8	0.79	0.79	0.8	µs	4
Repetition period		64	63.56	63.56	64	µs	
V1, V2							
V1 duration		10	6	6	10	H	
V2 duration		7.5	9	9	7.5	H	
V1 to sync delay	t_{PV1CS}	1.6	1.59	1.59	1.6	µs	8
Sync to V2 delay	t_{PV2CS}	1.6	1.59	1.59	1.6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$		
Sync to FH2 delay		0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$		
Sync to FH3 delay		–	–	–	0	µs	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width		2.4	2.38	2.38	2.4	μs	12
Sync to WMP delay		34.4	34.16	34.16	34.4	μs	172
Duration of WMP		10	9	9	10	H	
Position of WMP							
1st half picture:		H163 to H173	H134 to H143	H134 to H143	H163 to H173		
2nd half picture:		H475 to H485	H396 to H405	H396 to H405	H475 to H485		
RI							
Frequency		$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$		
Position of edges		H6 and H318	H7 and H269	H7 and H269	–		
ID							
ID pulse width	t_{WID}	12.0	11.12	11.12	12.0	μs	60
ID to sync delay	t_{PIDCS}	1.6	1.59	1.59	1.6	μs	8
Position of ID							
1st half picture:		H7 to H15	H8 to H22	H8 to H22	H7 to H15		
2nd half picture:		H320 to H328	H271 to H285	H271 to H285	H320 to H328		

* Horizontal blanking pulse width for NTSC 2 can be 11.12 μs maximum.

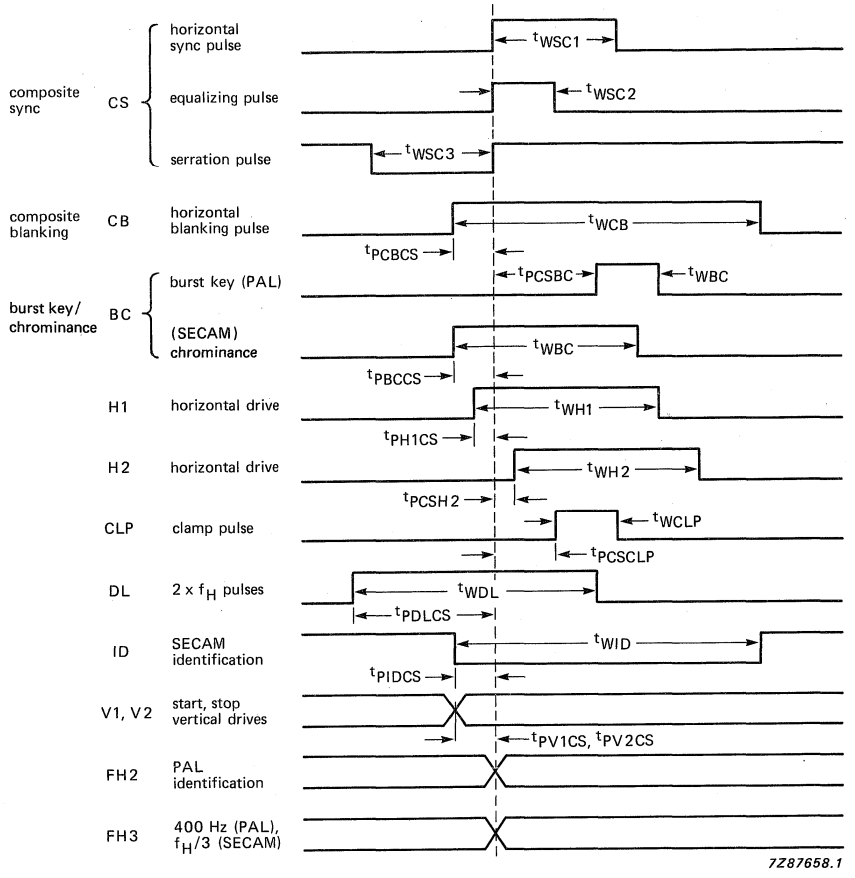


Fig. 9 Waveform timings; PAL/CCIR; SECAM; 624-line modes.

WAVEFORM TIMING (continued)

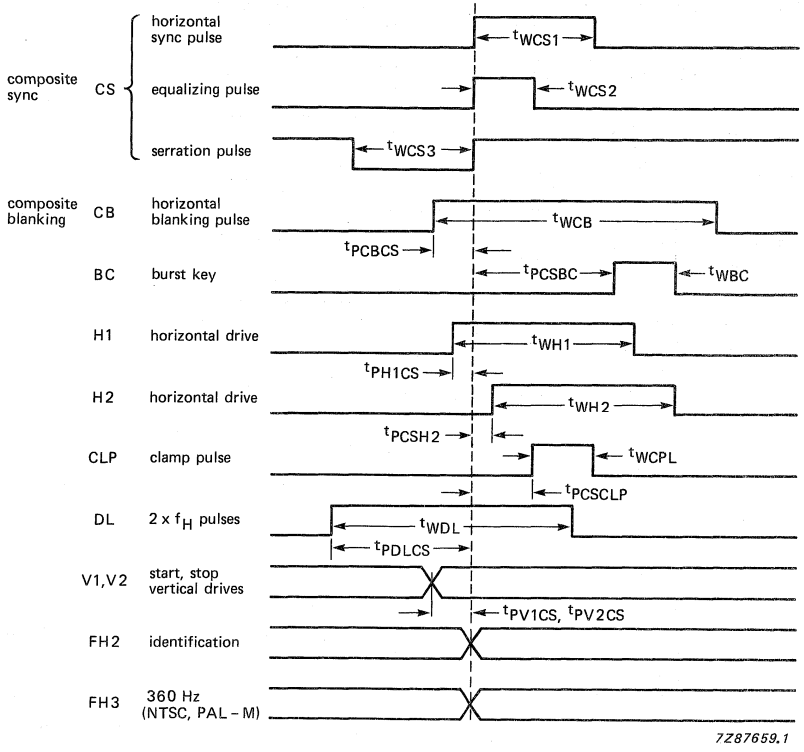


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	−	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	−	10	mA
Total power dissipation per package	P_{tot}	−	200	mW
Power dissipation per output	P_O	−	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V	$-I_{LO}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LO}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5.7 V	R_L	1.4	–	–	kΩ
at V_{DD} = 7.5 V	R_L	0.82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5.7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7.5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5.7 V	f_{OSC}	5.1	–	–	MHz

* An external pull-up resistor (3.9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

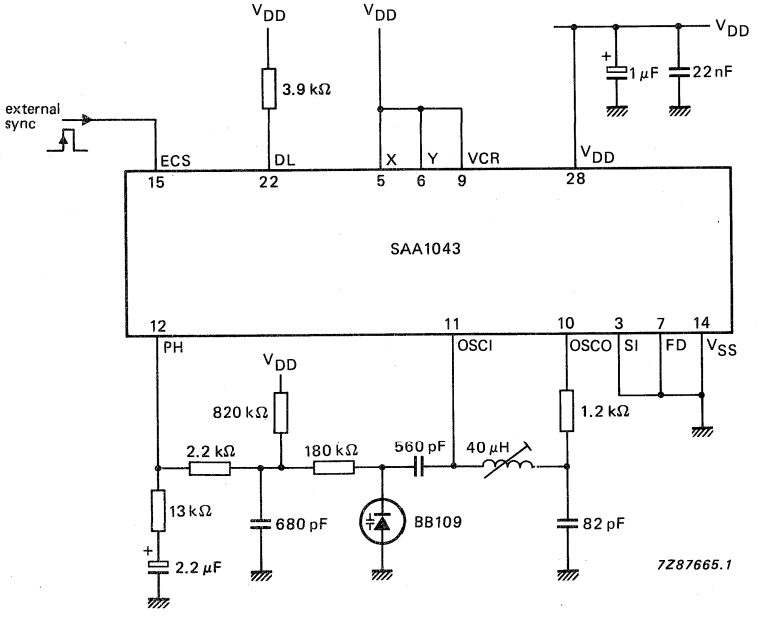


Fig. 11 Synchronizing circuit using passive filter network.

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

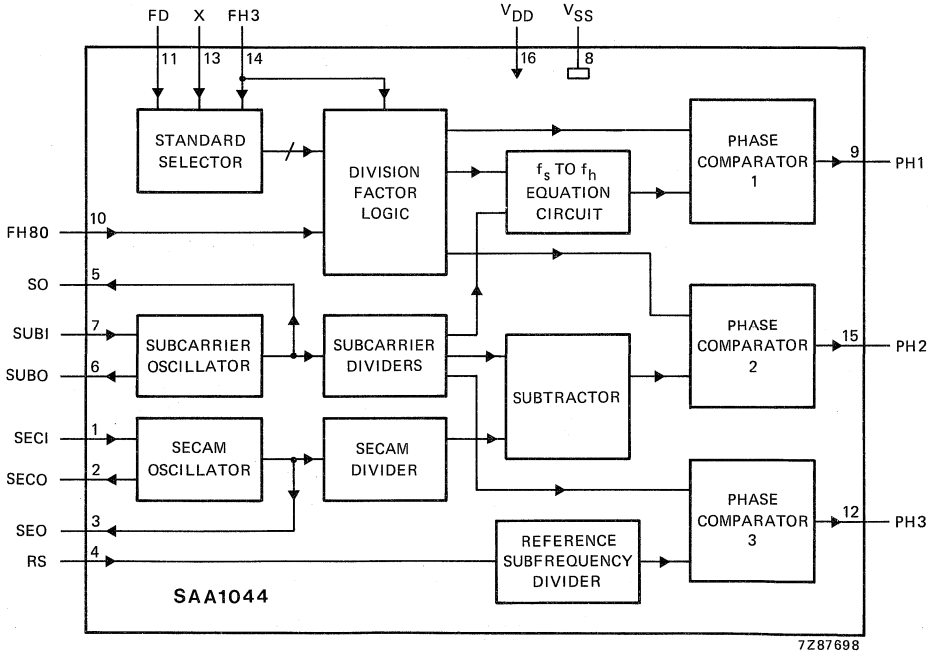


Fig.1 Block diagram.

PACKAGE OUTLINES

SAA1044: 16-lead DIL; plastic (SOT38).
SAA1044T: 16-lead mini-pack; plastic (SO16L; SOT162A).

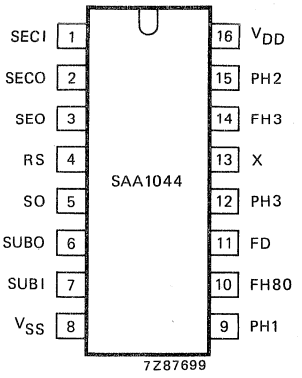


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1.25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283.7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229.2516f_H$
PAL-M	1	0	1	$f_S = 227.25f_H$
NTSC	1	0	0	$f_S = 227.5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty factor of between 12.5% and 62.5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	200	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

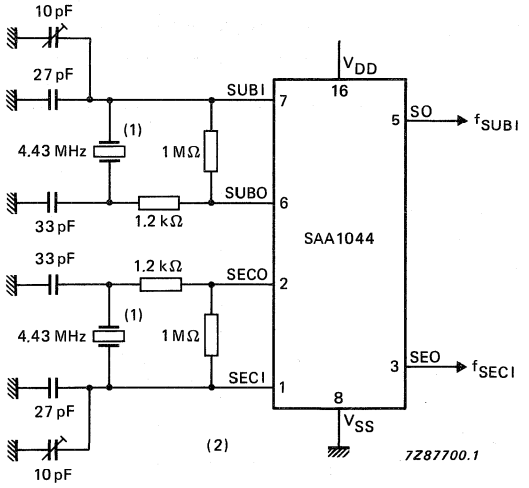
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

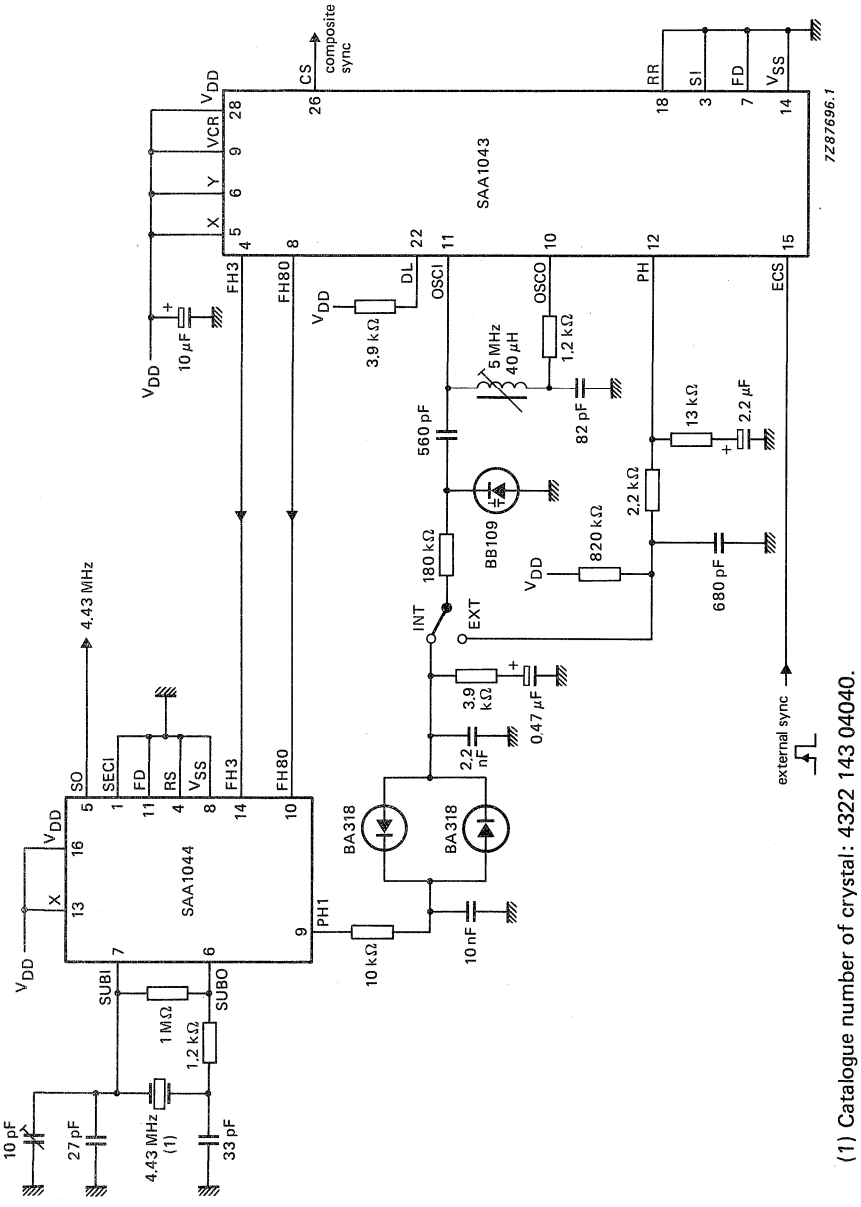
parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Oscillator frequency (Fig.3)					
Maximum oscillator frequency at V_{DD} = 5.7 V					
pin 1	f_{SECI}	5.1	–	–	MHz
pin 7	f_{SUBI}	5.1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

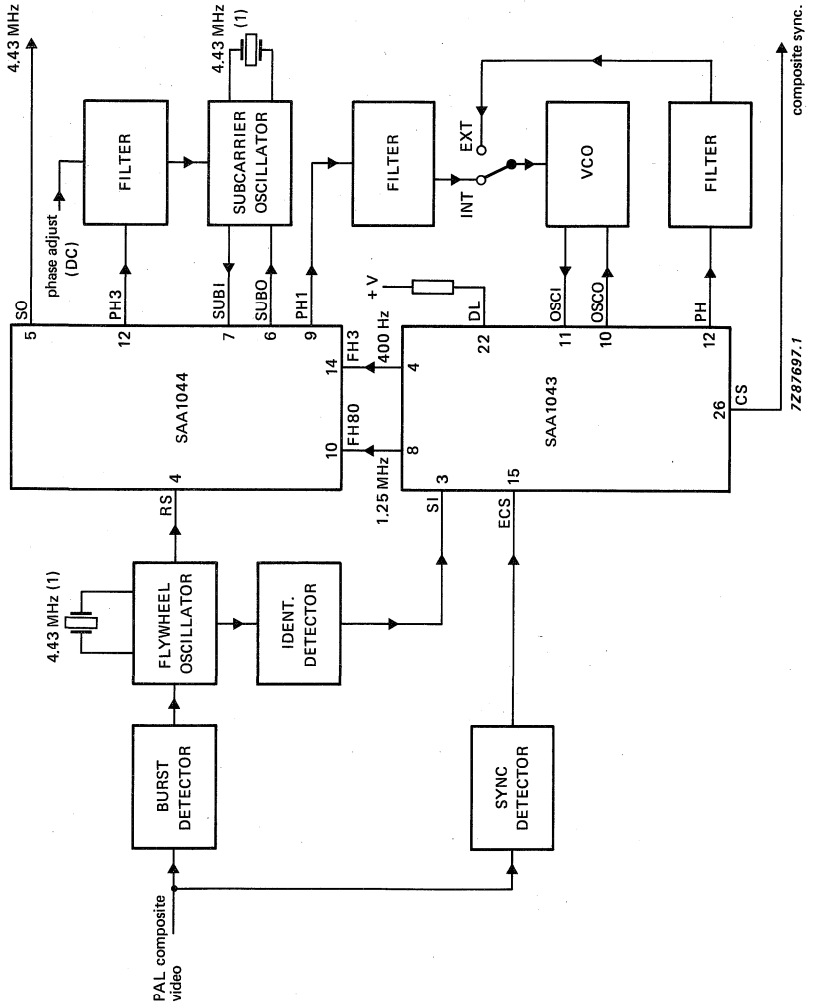
Fig.3 Test set-up for oscillator frequency measurement.

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig.4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig.5 Subcarrier coupling for PAL GENLOCK application.

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation 24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

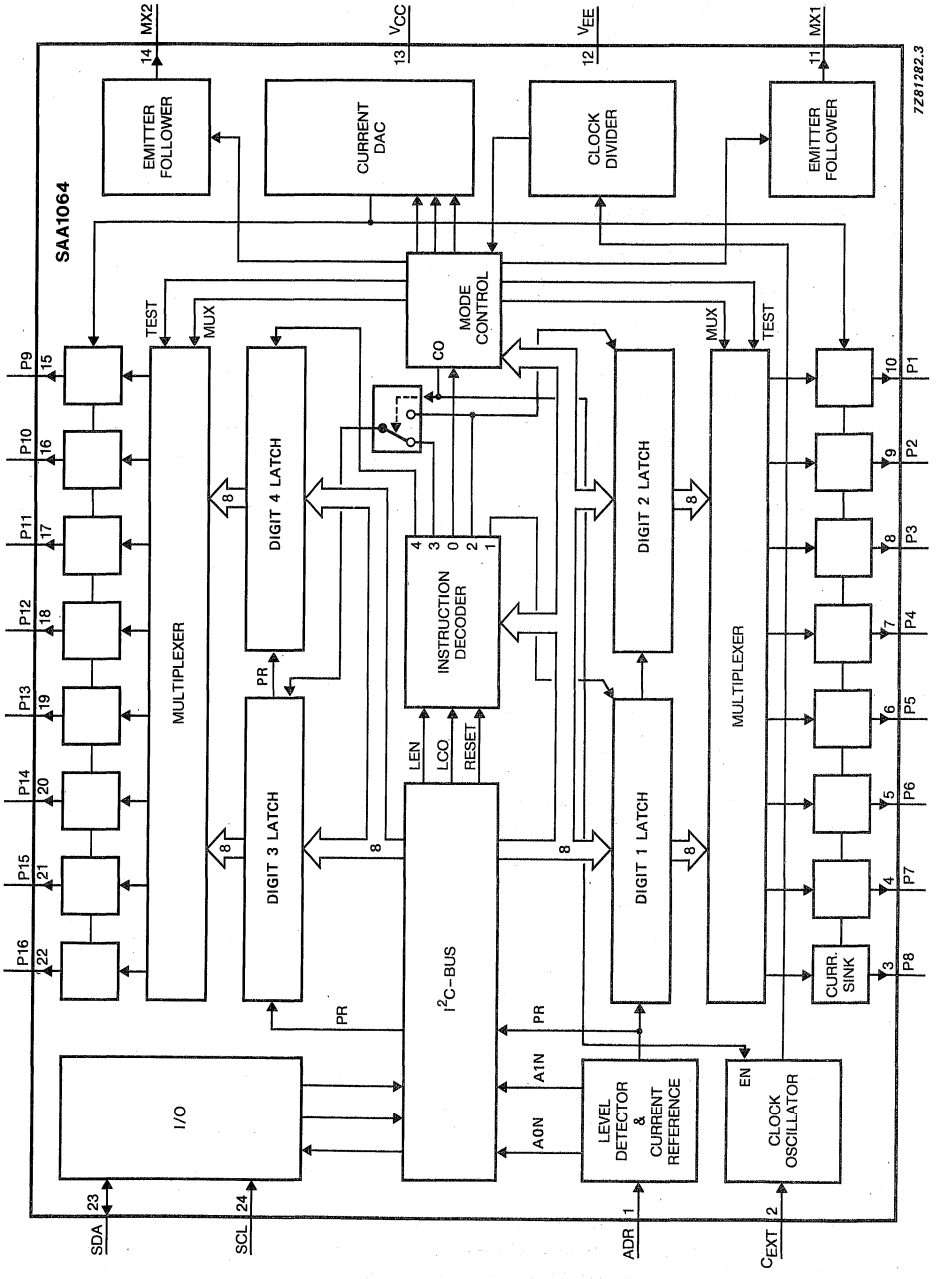


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ADR	1	I²C-Bus slave address input
C_{EXT}	2	external control
P8 to P1	3-10	segment output
MX1	11	multiplex output
V_{EE}	12	ground
V_{CC}	13	positive supply
MX2	14	multiplex output
P9 to P16	15-22	segment output
SDA	23	I²C-Bus serial data line
SCL	24	I²C-Bus serial clock line

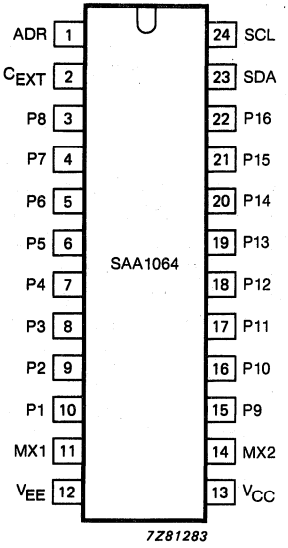
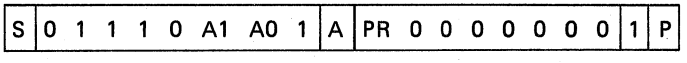


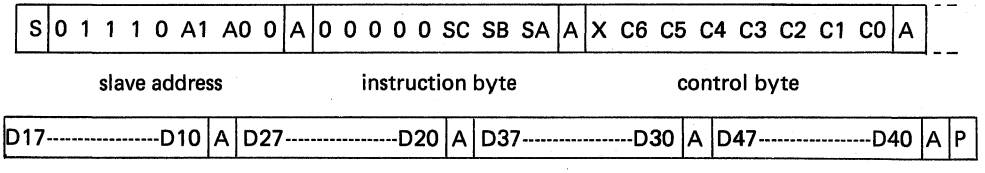
Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION



slave address status byte

Fig. 3a I²C-Bus format; READ mode.



slave address instruction byte control byte

data digit 1 data digit 2 data digit 3 data digit 4

Fig. 3b I²C-Bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I²C-Bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)	V_{EE} = 0 V	V_{CC}	−0.5	18	V
Supply current (pin 13)		I_{CC}	−50	200	mA
Total power dissipation					
24-lead DIL (SOT101B)		P_{tot}		1000	mW
24-lead SO (SO137A)		P_{tot}		500	mW
SDA, SCL voltages	V_{EE} = 0 V	$V_{23,24}$	−0.5	5.9	V
Voltages ADR-MX1 and MX2-P16	V_{EE} = 0 V	$V_{1\text{-}11}$, $V_{14\text{-}22}$	−0.5	V_{CC} + 0.5	V
Input/output current all pins	outputs OFF	$\pm I_{I/O}$	−	10	mA
Operating ambient temperature range		T_{amb}	−40	+ 85	°C
Storage temperature range		T_{stg}	−55	+ 150	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\,j\text{-}a}$	35 K/W
24-lead SO (on ceramic substrate)	$R_{th\,j\text{-}a}$	75 K/W
24-lead SO (on printed circuit board)	$R_{th\,j\text{-}a}$	105 K/W

CHARACTERISTICS

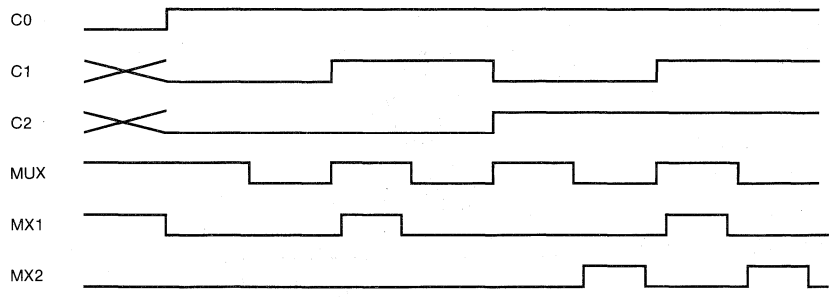
V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	$-I_{IL}$	–	–	10	μA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	μA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_{SDA}	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	3/16V_{CC}	V
A0 = 1; A1 = 0		V_1	5/16V_{CC}	3/8V_{CC}	7/16V_{CC}	V
A0 = 0; A1 = 1		V_1	9/16V_{CC}	5/8V_{CC}	11/16V_{CC}	V
A0 = 1; A1 = 1		V_1	13/16V_{CC}	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	$-I_1$	–	–	10	μA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	μA
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}–3,3	V
Input voltage HIGH		V_{IH}	V_{CC}–1,5	–	–	V
Input current	V_2 = 2 V	I_2	–140	–160	–180	μA
	V_2 = 4 V	I_2	140	160	180	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs (P8 to P1; pins 3 to 10) P9 to P16; pins 15 to 22)						
Output voltages	I_O = 15 mA	V_O	–	–	0.5	V
Output leakage current HIGH	$V_O = V_{CC}$ = 15 V	I_{LO}	–	–	± 10	μA
Output current LOW						
All control bits (C4, C5 and C6) are HIGH	V_{OL} = 5 V	I_{OL}	17.85	21	25.2	mA
Contribution of:						
control bit C4		I_O	2.55	3.0	3.6	mA
control bit C5		I_O	5.1	6.0	7.2	mA
control bit C6		I_O	10.2	12.0	14.4	mA
Relative segment output current accuracy						
with respect to highest value		ΔI_O	–	–	7.5	%
Multiplex 1 and 2 (pins 11 and 14)						
Maximum output voltage (when ON)	$-I_{MPX}$ = 50 mA	V_{MPX}	V_{CC}–1.5	–	–	V
Maximum output current HIGH (when ON)	V_{MPX}= 2 V	$-I_{MPX}$	50	–	110	mA
Maximum output current LOW (when OFF)	V_O = 2 V	+ I_{MPX}	50	70	110	μA
Multiplex output period	C_{EXT} = 2.7 nF	T_{MPX}	5	–	10	ms
Multiplexed duty factor			–	48.4	–	%

* Value to be fixed.



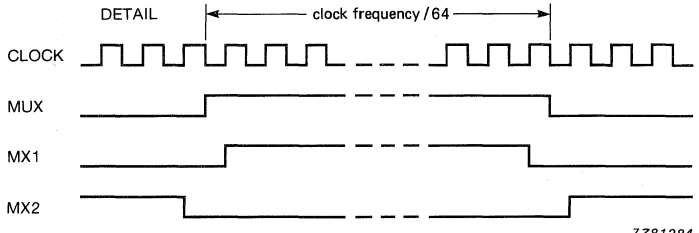


Fig. 4 Timing diagram.

APPLICATION INFORMATION

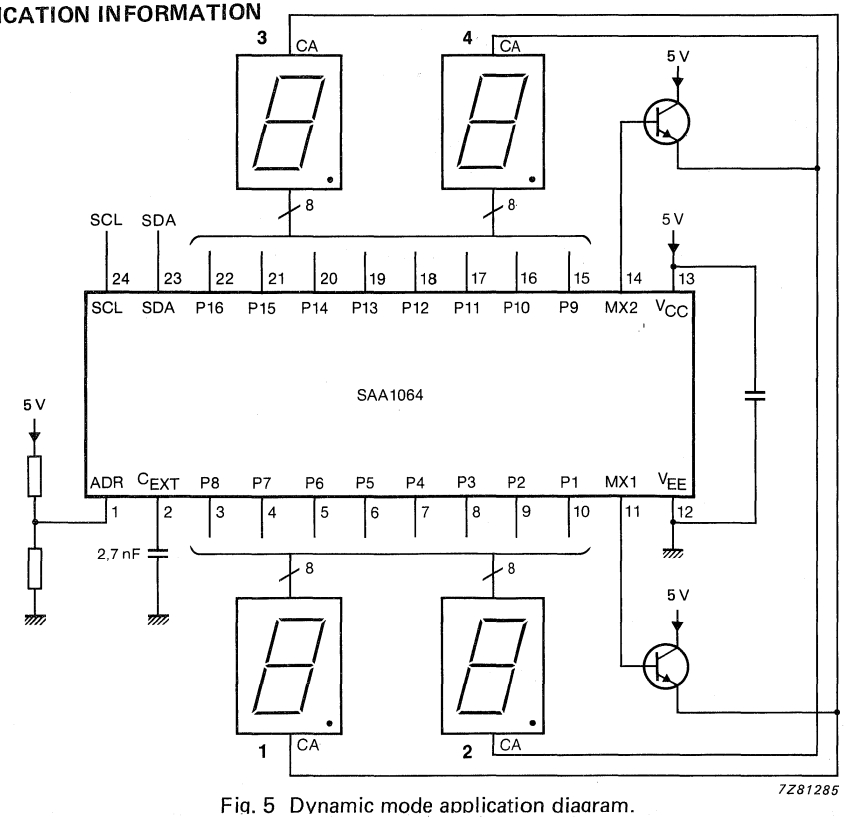


Fig. 5 Dynamic mode application diagram.

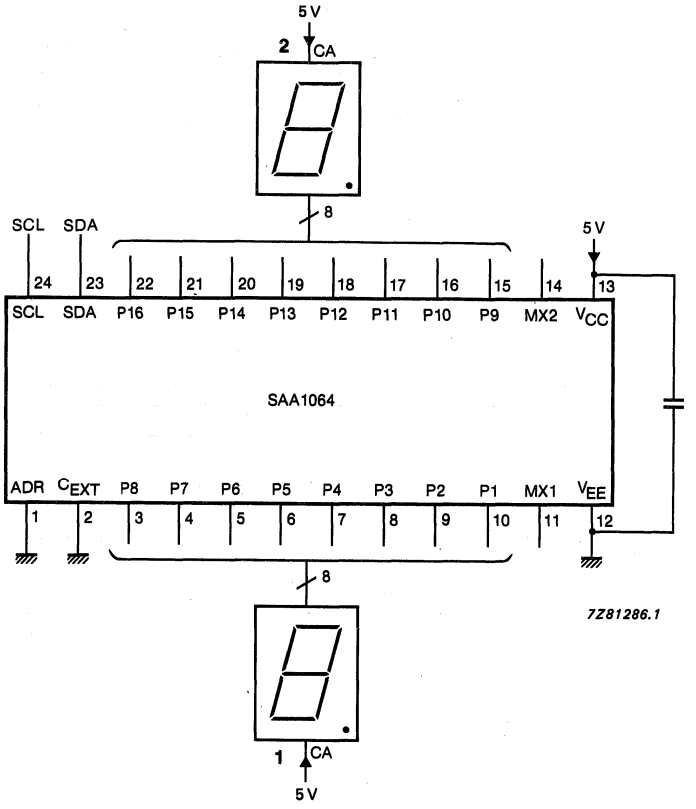


Fig. 6 Static mode application diagram.

POWER DISSIPATION

The total maximum power dissipation of the SAA1064 is made up by the following parts:

1. Maximum dissipation when none of the outputs are programmed (continuous line in Fig.7).
2. Maximum dissipation of each programmed output. The dashed line in Fig.7 visualises the dissipation when **all** the segments are programmed (max. 16 in the static, and max. 32 in the dynamic mode). When less segments are programmed one should take a proportional part of the maximum value.
3. Maximum dissipation of the programmed segment drivers which can be expressed as: $P_{add} = V_o \times I_o \times N$.

Where:
- P_{add} = The additional power dissipation of the segment drivers
- V_o = The low state segment driver output voltage
- I_o = The programmed segment output current
- N = The number of programmed segments in the static mode, or half the number of programmed segment drivers in the dynamic mode.

Under no conditions the total maximum dissipation (500 mW for the SO and 1000 mW for the DIL package) should be exceeded.

Example: V_{cc} = 5 V

V_o = 0.25 V

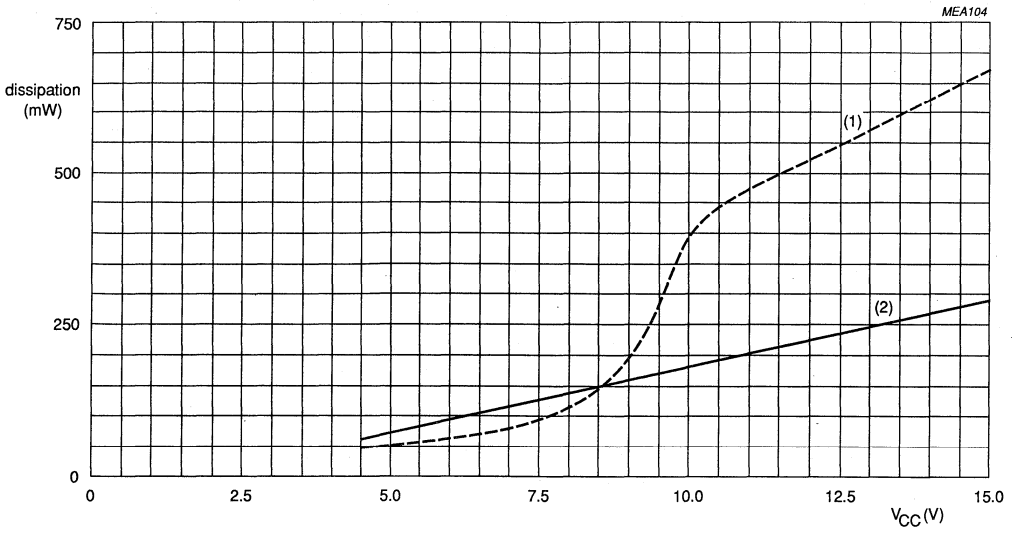
I_o = 12 mA

24 programmed segments in dynamic mode

$P_{tot} = P_1 + P_2 + P_3$

$= 75\ mW + (50 * 24/32)\ mW + (0.25 * 12.10^{-3} * 12)\ mW$

$= 148.5\ mW$



(1) All outputs programmed (no segment current sink).

(2) Outputs not programmed.

Fig.7 SAA1064 power dissipation as a function of supply voltage.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	70 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		500 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

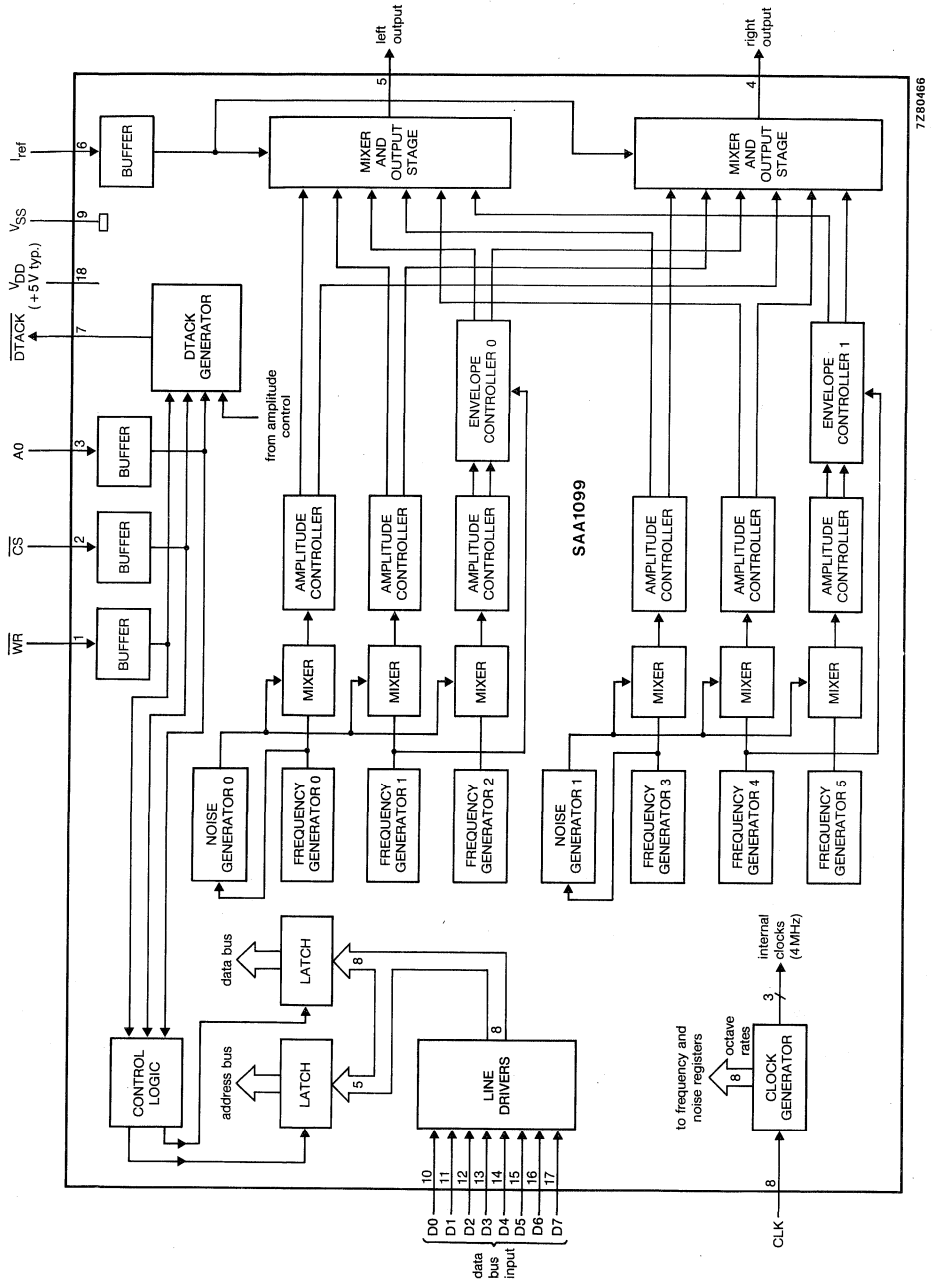


Fig. 1 Block diagram.

PINNING

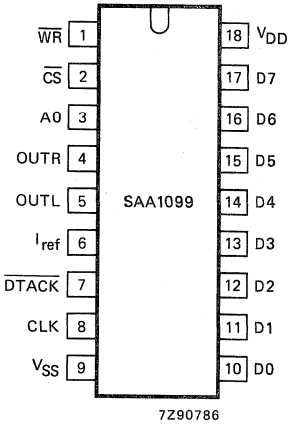


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 31 Hz to 7,81 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required. The frequency generators may be synchronized using the frequency reset bit.

The frequency ranges per octave are:

Octave	Frequency range
0	31 Hz to 61 Hz
1	61 Hz to 122 Hz
2	122 Hz to 244 Hz
3	245 Hz to 488 Hz
4	489 Hz to 977 Hz
5	978 Hz to 1,95 kHz
6	1,96 kHz to 3,91 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.

In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to + 7,5	V
Maximum input voltage	V_I	−0,3 to + 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to + 7,5	V
Maximum output current	I_O	max. 10	mA
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	70	100	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	120	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	110	%
With I_{ref} = 250 μA; R_L = 1,5 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	90	–	110	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	105	%
Output current one channel on	I_{01}	225	–	275	μA
Output current six channels on	I_{06}	1,3	–	1,6	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	150	–	350	μA
Output current six channels on	I_{06}	0,9	–	1,9	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	$4t_{CLK}$	–	–	
Bus cycle time (note 9)	t_{CY}	$16t_{CLK}$	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{LOW}	55	–	–	ns
Clock HIGH time	t_{HIGH}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E12 (5%) in all applications via:

$$R_L = 0{,}6\ [I_{ref}]^{-1} - 16\ [I_{ref}]^{-0{,}5} \pm 12\%$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 1,5 kΩ (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of four clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of 16 clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

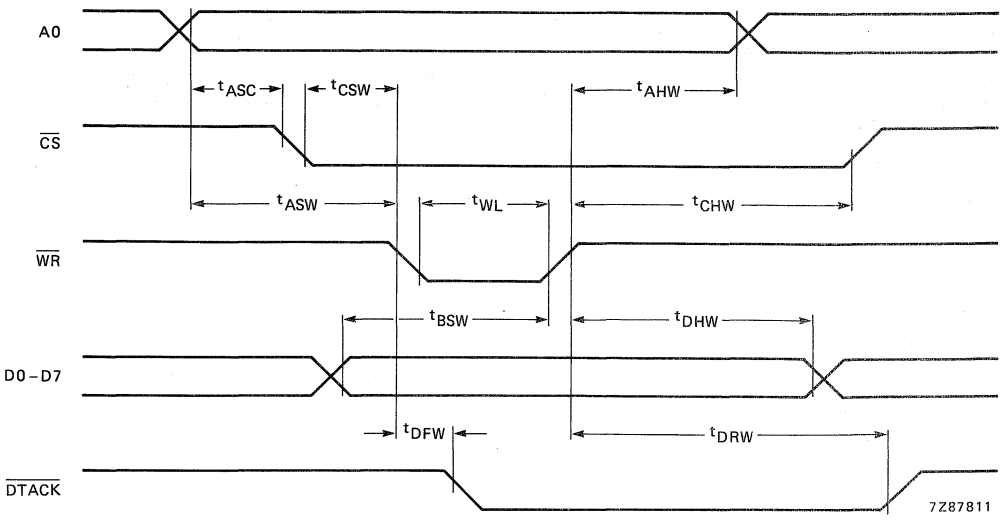


Fig. 3 Bus interface waveforms.

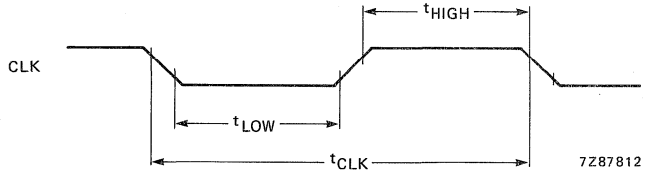


Fig. 4 Clock input waveform.

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,81 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	frequency reset (all channels) / sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (31 Hz to 61 Hz) 0 0 1 (61 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (245 Hz to 488 Hz) 1 0 0 (489 Hz to 977 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,96 kHz to 3,91 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency 0 0 31,3 kHz 0 1 15,6 kHz 1 0 7,6 kHz 1 1 61 Hz to 15,6 kHz (frequency generator 0/3)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 977 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled
RST	Reset signal to all frequency generators 0 all generators enabled 1 all generators reset and synchronized

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

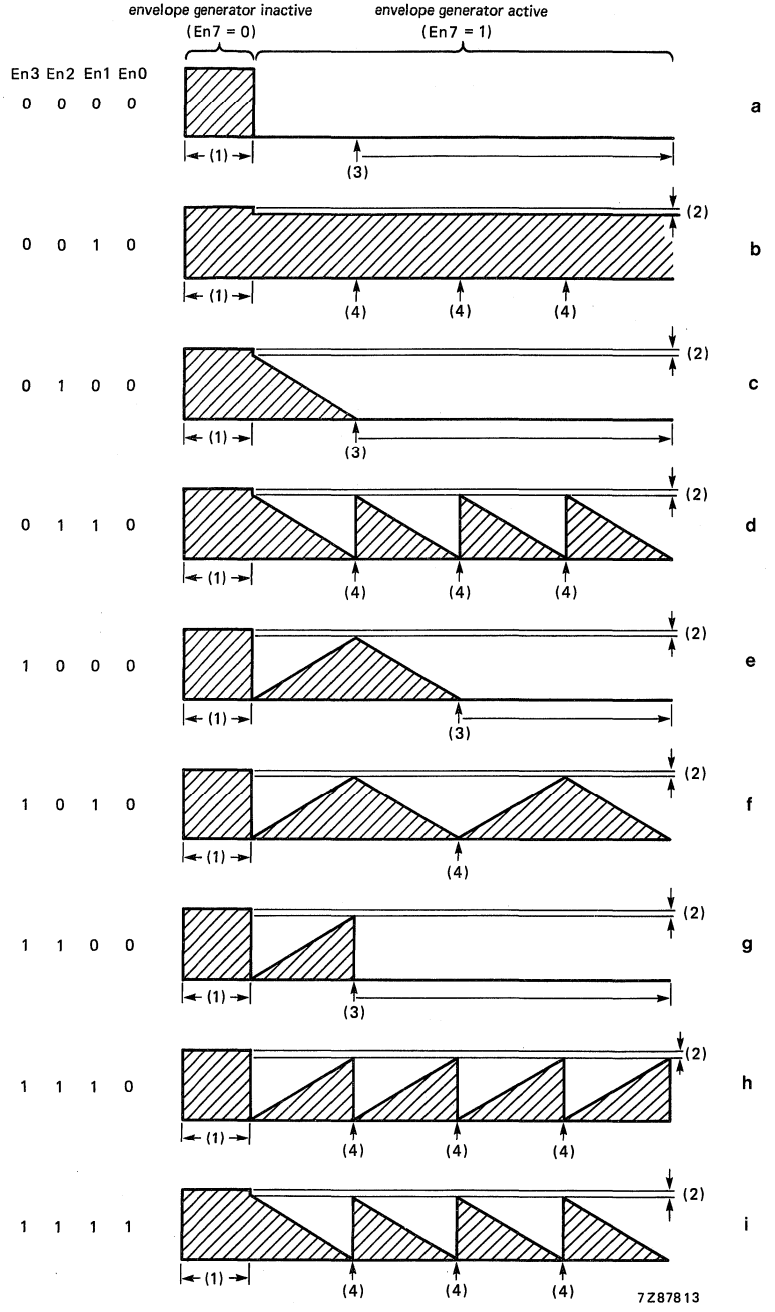


Fig. 5 Envelope waveforms.

DEVELOPMENT DATA

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 7/8ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

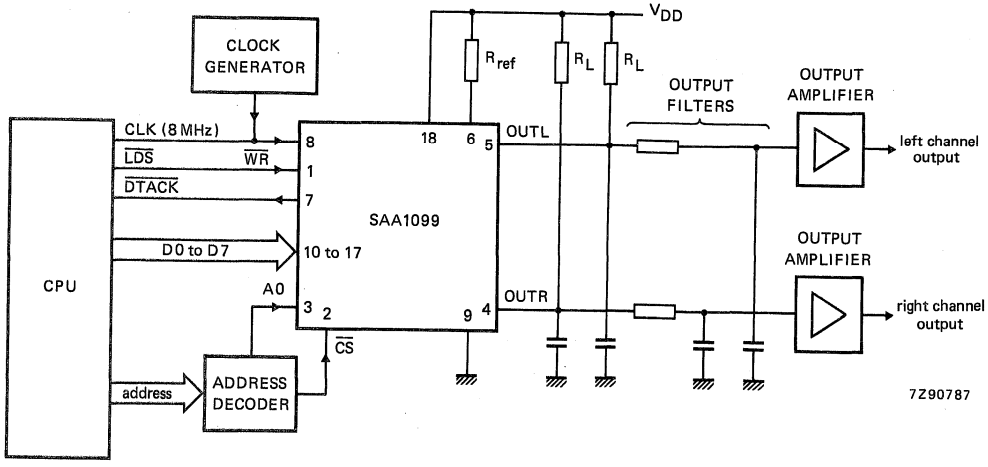


Fig. 6 Typical application circuit diagram.

Data sheet	
status	Product specification
code	
date of issue	January 1990

SAA1101
Universal sync generator (USG)

FEATURES

- Programmable to seven standards
- Additional outputs to simplify signal processing
- Can be synchronized to an external sync. signal
- Option to select the 524/624 line mode instead of the 525/625 line mode
- Lock from subcarrier to line frequency

GENERAL DESCRIPTION

The SAA1101 is a Universal Sync Generator (USG) and is designed for application in video sources such as cameras, film scanners, video generators and associated apparatus. The circuit can be considered as a successor to the SAA1043 sync generator and the SAA1044 subcarrier coupling IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range (pin 28)	4.5	5.5	V
I_{DD}	quiescent supply current	–	10	µA
f_{OSC}	clock oscillator frequency	–	24	MHz

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1101P	28	DIL	plastic	SOT117
SAA1101T	28	SO28	plastic	SOT136A

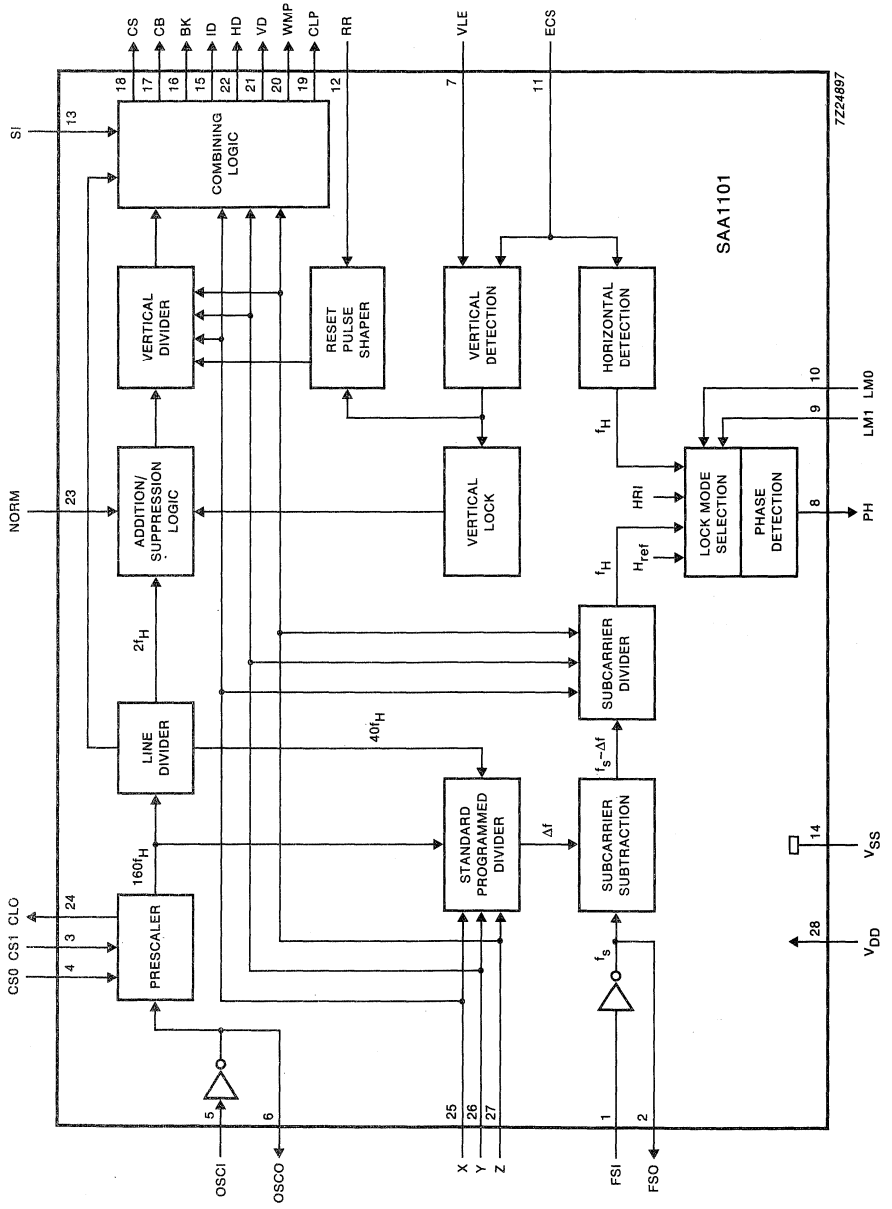


Fig.1 Block diagram.

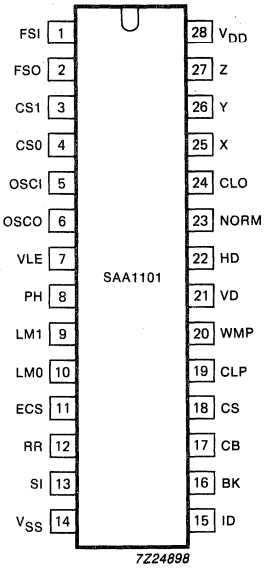


Fig.2 Pinning configuration; SOT117.

FUNCTIONAL DESCRIPTION

Generation of pulses

Generation of standard pulses such as sync, blanking and burst for TV systems: PAL B/G, PALN, PALM, SECAM and NTSC. In addition a number of non-standard pulses have been supplied to simplify signal processing. These signals include – horizontal drive, vertical drive, clamp pulse, identification etc. It is possible to select the 524/624 line mode instead of the 525/625 line mode for all the above TV systems for applications such as robotics, games and computers.

PINNING

SYMBOL	PIN	DESCRIPTION
FSI	1	subcarrier oscillator input, where f_{max} = 5 MHz
FSO	2	subcarrier oscillator output
CS1	3	clock frequency selection – CMOS input
CS0	4	clock frequency selection – CMOS input
OSCI	5	clock oscillator input, where f_{max} = 24 MHz
OSCO	6	clock oscillator output
VLE	7	vertical in-lock enable – CMOS input
PH	8	phase detector output – 3-state output
LM1	9	lock mode selection – CMOS input
LM0	10	lock mode selection – CMOS input
ECS	11	external composite sync. signal – CMOS Schmitt-trigger input
RR	12	frame reset – CMOS Schmitt-trigger input
SI	13	set identification, used to set the correct field sequence in PAL-mode. The correction (inversion of fH2) is done at the left-hand slope of the SI-pulse. Minimum pulse width is 800 ns. CMOS Schmitt-trigger input.
V_{SS}	14	ground
ID	15	identification – push-pull output
BK	16	burst key (PAL/NTSC), chroma-blanking (SECAM) – push-pull output
CB	17	composite blanking – push-pull output
CS	18	composite sync. – push-pull output
CLP	19	clamp pulse – push-pull output
WMP	20	white measurement pulse – 3-state output
VD	21	vertical drive pulse – push-pull output
HD	22	horizontal drive pulse – push-pull output
NORM	23	used with X, Y and Z to select TV system; NORM = 0, 625/525 line mode (standard); NORM = 1, 624/524 line mode – CMOS input
CLO	24	clock output – push-pull output
X	25	TV system selection input – CMOS input
Y	26	TV system selection input – CMOS input
Z	27	TV system selection input – CMOS input
V_{DD}	28	voltage supply

Lock modes

The USG offers four lock modes:

- Lock from the subcarrier
- Slow sync. lock, external H_{ref}
- Slow sync. lock, internal H_{ref}
- Fast sync. lock, internal H_{ref}

LOCK FROM SUBCARRIER

Lock from subcarrier to the line frequency for the above mentioned TV systems is given below; the horizontal frequency (f_H) = 15.625 kHz for 625 line systems and 15.734264 kHz for 525 line systems.

SECAM (1 and 2)	$282f_H$
PALN	$229.2516f_H$
NTSC (1 and 2)	$227.5f_H$
PALM	$227.25f_H$
PAL B/G	$283.7516f_H$

These relationships are obtained by the use of a phase locked loop and the internal programmed divider chain, see Fig. 3(a).

LOCK TO AN EXTERNAL SIGNAL SOURCE

The following methods can be used to lock to an external signal source:

1. Sync. lock slow; the line frequency is locked to an external signal. The line and frame information are extracted from the external sync. signal and used separately in the lock system. The line information is used in a phase-locked loop where external and internal line frequencies are compared by the same phase detector as is used for the subcarrier lock. The external frame information is compared with the internal frame in a slow lock system; mismatch of internal and external frames will result in the addition or suppression of one line depending on the direction of the fault. The maximum lock time for frame lock is 6.25 s, see Fig. 3(b).
2. Sync. lock fast. A fast lock of frames is possible with a frame reset which is extracted out of the incoming external sync. signal, see Fig. 3(c).
3. Sync. lock with external reference. Lock of an external sync. signal to the line frequency with an external line reference to make possible a shifted lock. The subcarrier input is, in this case, used as an external input for the horizontal reference, see Fig. 3(d).

SELECTION OF LOCK MODE

Lock mode is selected using the inputs LM0 and LM1 as illustrated in the Table below.

LM0	LM1	SELECTION
0	0	lock to subcarrier
0	1	slow sync. lock external H_{ref}
1	0	slow sync. lock internal H_{ref}
1	1	fast sync. lock internal H_{ref}

The different lock modes are illustrated by the following figures:

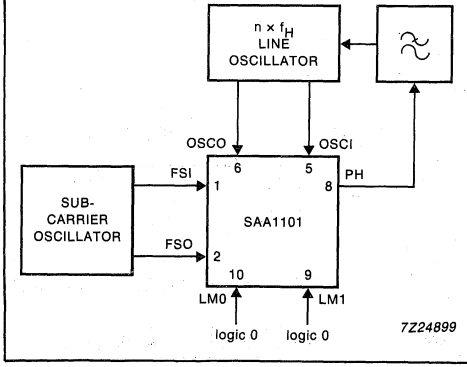


Fig.3(a) Lock to subcarrier

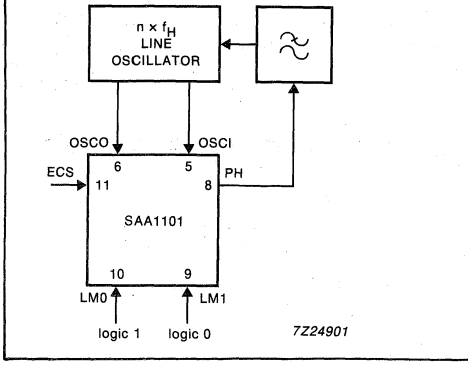


Fig.3(b) Slow sync lock, internal H_{ref}

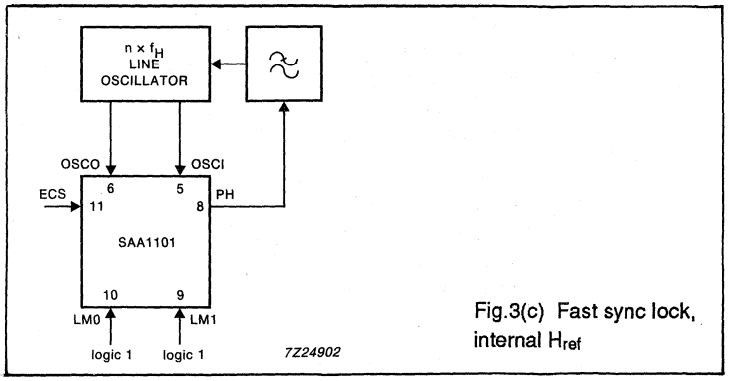


Fig.3(c) Fast sync lock, internal H_{ref}

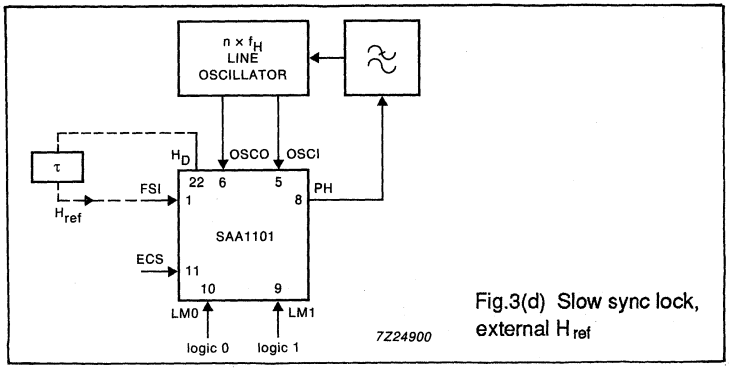


Fig.3(d) Slow sync lock, external H_{ref}

LOCK WITH HORIZONTAL AND VERTICAL SIGNALS

(slow lock modes only)

It is possible to use horizontal and vertical signals instead of composite sync signals. The connections in this situation are: the external horizontal signal is connected to the ECS input (pin 11) and the vertical signal to the RR input (pin 12). The HIGH time of the horizontal pulse must be less than 14.4 μs, otherwise it will be detected as being a vertical pulse and will corrupt the vertical slow lock system.

Selection of Clock Frequency

The clock frequency is selected using the CS0 and CS1 inputs as illustrated below.

CS0	CS1	FREQUENCY	625 LINES	525 LINES	UNITS
0	0	$160f_H$	2.5	2.517482	MHz
0	1	$320f_H$	5	5.034964	MHz
1	0	$960f_H$	15	15.104893	MHz
1	1	$1440f_H$	22.5	22.657340	MHz

Where the horizontal frequency, f_H = 15.625 kHz for 625 lines and 15.734264 kHz for 525 lines.

Oscillators

The subcarrier oscillator has FSI as its input and FSO as its output. It is always used as a crystal oscillator with a series resonance crystal with parallel load capacitor. The maximum frequency, $f_{max} = 5$ MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

The clock oscillator has OSCI as its input and OSCO as its output. It can be used with an LC oscillator or a series resonance crystal with parallel load capacitor (Fig.4). The maximum frequency, $f_{max} = 24$ MHz and the load capacitor, $C_L = 10 < C_L < 35$ pF.

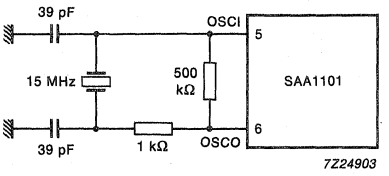


Fig.4 Crystal oscillator circuit.

Selection of TV System

Selection of the required TV system is achieved by the X, Y and Z inputs as illustrated by the following Table.

SYSTEM	X	Y	Z
SECAM1	0	0	0
PALN	0	0	1
NTSC1	0	1	0
PALM	0	1	1
SECAM2	1	0	0 (with identifier)
PAL B/G	1	0	1
NTSC2	1	1	0 (short blanking)

Selection of 625/525 (standard; interlaced mode) or 624/524 lines (non-interlaced mode)

Selection is achieved using the NORM input. When NORM = 0, 625/525 (standard) lines are selected; when NORM = 1, 624/524 line are selected.

Output Dimensions

All push-pull outputs: standard output 2 mA.

White measurement pulse, WMP: 3-state output 2 mA.

Phase detector, PH: 3-state output 2 mA.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7	V
V_I	input voltage	−0.5	$V_{DD} + 0.5$ *	V
I_I	maximum input current	–	±10	mA
I_O	maximum output current	–	±10	mA
I_{DD}	maximum supply current in V_{DD}	–	25	mA
P_{tot}	maximum power dissipation	–	400	mW
T_{stg}	storage temperature range	−55	+150	°C

* Input voltage should not exceed 7 V.

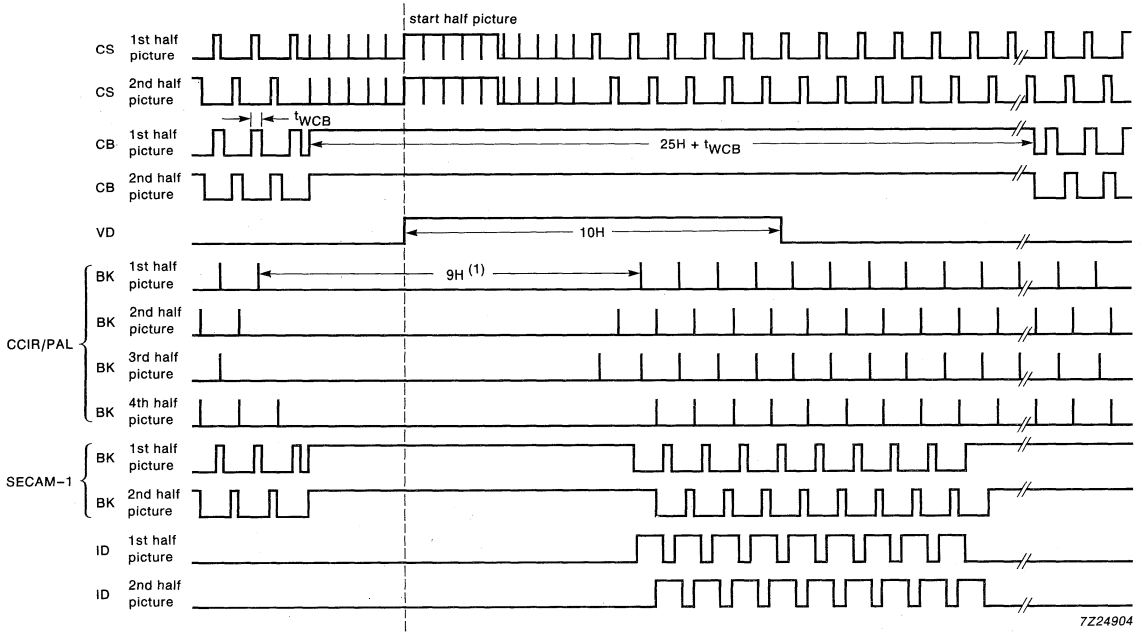
CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = -25 to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	–	5.5	V
I_{DD}	supply current (quiescent)	T_{amb} = 25 °C	–	–	10	µA
Inputs						
$\pm I_I$	input leakage current	T_{amb} = 25 °C	–	–	100	nA
CMOS COMPATIBLE; X, Y, Z, NORM, CS0, CS1, LM0, LM1 AND VLE						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	–	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
SCHMITT TRIGGER INPUTS; ECS, RR AND SI						
V_{T+}	positive-going threshold		–	2.5	4	V
V_{T-}	negative-going threshold		1	1.5	–	V
V_H	hysteresis		0.4	1	–	V
OSCILLATOR INPUTS; OSCI AND FSI						
V_{IH}	input voltage HIGH		$0.7V_{DD}$	-	–	V
V_{IL}	input voltage LOW		–	–	$0.3V_{DD}$	V
Outputs						
PUSH-PULL OUTPUTS; CB, CS, BK, ID, HD, VD, CLP AND CLO						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
OSCILLATOR OUTPUTS; OSCO AND FSO						
V_{OH}	output voltage HIGH	$-I_O$ = 0.75 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 0.75 mA; V_{DD} = 5 V	–	–	0.5	V
3-STATE OUTPUTS; WMP AND PH						
V_{OH}	output voltage HIGH	$-I_O$ = 2 mA; V_{DD} = 5 V	4.5	–	–	V
V_{OL}	output voltage LOW	I_O = 2 mA; V_{DD} = 5 V	–	–	0.5	V
$\pm I_{OZ}$	OFF-state current	T_{amb} = 25 °C	–	–	50	nA

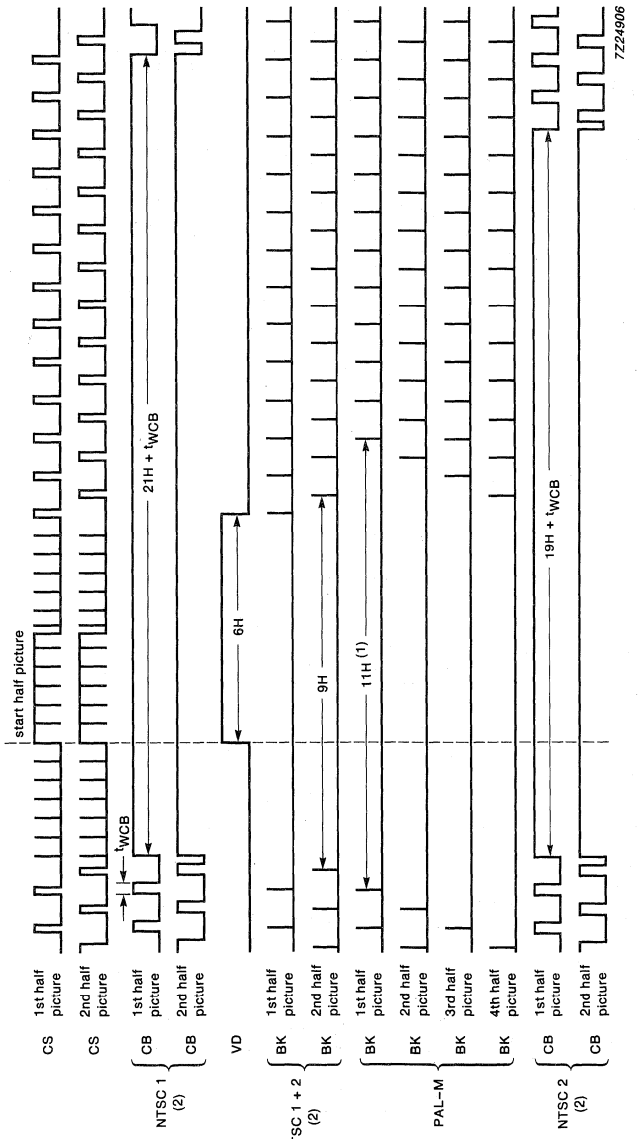
OUTPUT WAVEFORMS

The output waveforms for the different modes of operation are illustrated by Figs 5 and 6.



(1) H = 1 horizontal scan.

Fig.5 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the first half picture of PAL/CCIR and are not interlaced.



(1) H = 1 horizontal scan.
(2) NTSC mode reset; the fourth half picture is identical to the second half picture for NTSC.

Fig.6 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the first half picture of NTSC and are not interlaced.

WAVEFORM TIMING

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is illustrated in the table below as the number (N) of oscillations at OSCI. The timings are derived from N x t_{OSCI} ± 100 ns.
One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$.
Where t_{OSCI} = 200 ns for PAL/SECAM and 198.6 ns for NTSC/PAL-M

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Composite sync (CS)							
t_{WSC1}	horizontal sync pulse width	4.8	4.77	4.77	4.8	µs	24
t_{WSC2}	equalizing pulse width	2.4	2.38	2.38	2.4	µs	12
t_{WSC3}	serration pulse width	4.8	4.77	4.77	4.8	µs	24
-	duration of pre-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of post-equalizing pulses	2.5	3	3	2.5	H	-
-	duration of serration pulses	2.5	3	3.5	2.5	H	-
Composite blanking (CB)							
HORIZONTAL BLANKING PULSE WIDTH							
t_{WCB}	PAL/SECAM/PAL-M	12	–	11.12	12	µs	60
t_{WCB}	NTSC1	–	11.12	–	–	µs	56
t_{WCB}	NTSC2	–	10.53 *	–	–	µs	53
FRONT PORCH							
t_{PCBCS}	front porch	1.6	1.59	1.59	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	PAL/SECAM/PAL-M	25H + t_{WCB}	–	21H + t_{WCB}	25H + t_{WCB}	–	-
-	NTSC1	–	21H + t_{WCB}	–	–	–	-
-	NTSC2	–	19H + t_{WCB}	–	–	–	-
Burst key (BK) (not SECAM)							
t_{WBK}	burst key pulse width	2.4	2.38	2.38	–	µs	12
t_{PCSBK}	CS to burst key delay	5.6	5.56	5.76	–	µs	28
-	burst suppression	9	9	11	–	H	-

* Horizontal blanking pulse width for NTSC2 can be 11.12 µs maximum

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
Burst key (BK) (not SECAM) (continued) POSITION OF BURST SUPPRESSION							
-	first half picture	H623 to H6	H523 to H6	H523 to H8	–	–	-
-	second half picture	H310 to H318	H261 to H269	H260 to H270	–	–	-
-	third half picture	H622 to H5	H523 to H6	H522 to H7	–	–	-
-	fourth half picture	H311 to H319	H261 to H269	H259 to H269	–	–	-
Burst key (BK) (SECAM)							
t_{WBK}	chroma pulse width	–	–	–	7.2	µs	36
t_{PBKCS}	CS to chroma delay	–	–	–	1.6	µs	8
DURATION OF VERTICAL BLANKING							
-	SECAM1	–	–	–	note 1	–	-
-	SECAM2	–	–	–	note 2	–	-
Clamp pulse (CLP)							
t_{WCLP}	clamp pulse width	2.4	2.38	2.38	2.4	µs	12
t_{PCSCLP}	CS to CLP delay	1.6	1.59	1.59	1.6	µs	8
Horizontal drive (HD)							
t_{WHD}	pulse width	7.2	7.15	7.15	7.2	µs	36
t_{PHDCS}	CS to HD delay	0.8	0.79	0.79	0.8	µs	4
-	repetition period	64	63.56	63.56	64	µs	-
Vertical drive (VD)							
-	VD duration	10	6	6	10	H	-
t_{PVDCS}	CS to VD delay	1.6	1.59	1.59	1.6	µs	8
White measurement pulse (WMP)							
-	pulse width	2.4	2.38	2.38	2.4	µs	12
-	CS to WMP delay	34.4	34.16	34.16	34.4	µs	172
-	duration of WMP	10	9	9	10	H	-

WAVEFORM TIMING (CONTINUED)

SYMBOL	PARAMETER	PAL	NTSC	PAL-M	SECAM	UNIT	N
White measurement pulse (WMP) (continued)							
POSITION OF WMP							
-	first half picture	H163 to H173	H134 to H143	H134 to H143	H163 to H173	–	-
-	second half picture	H475 to H485	H396 to H405	H396 to H405	H475 to H485	–	-
Identification (ID)							
t_{WID}	pulse width	12	11.12	11.12	12	µs	60
t_{PIDCS}	CS to ID delay	1.6	1.59	1.59	1.6	µs	8
POSITION OF ID							
-	first half picture	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	-
-	second half picture	H320 to H328	H271 to H285	H271 to H285	H320 to H328	–	-

Notes to the characteristics

1. SECAM1, first half picture: 25H + t_{WBK} except H320 to H328. Second half picture: 24.5H + t_{WBK} except H7 to H15.

2. SECAM2, first half picture: 25H + t_{WBK}. Second half picture: 24.5H + t_{WBK}.

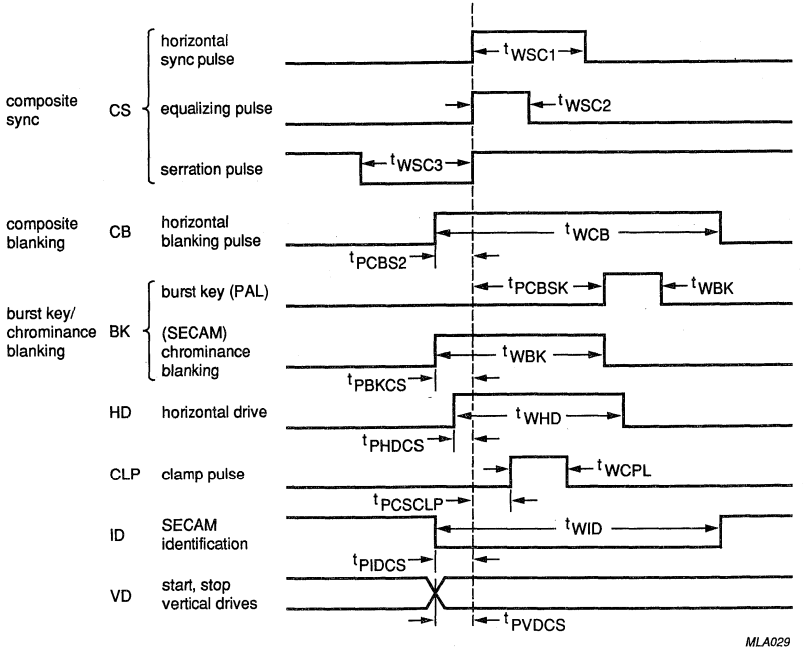


Fig.7 Waveform timing.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

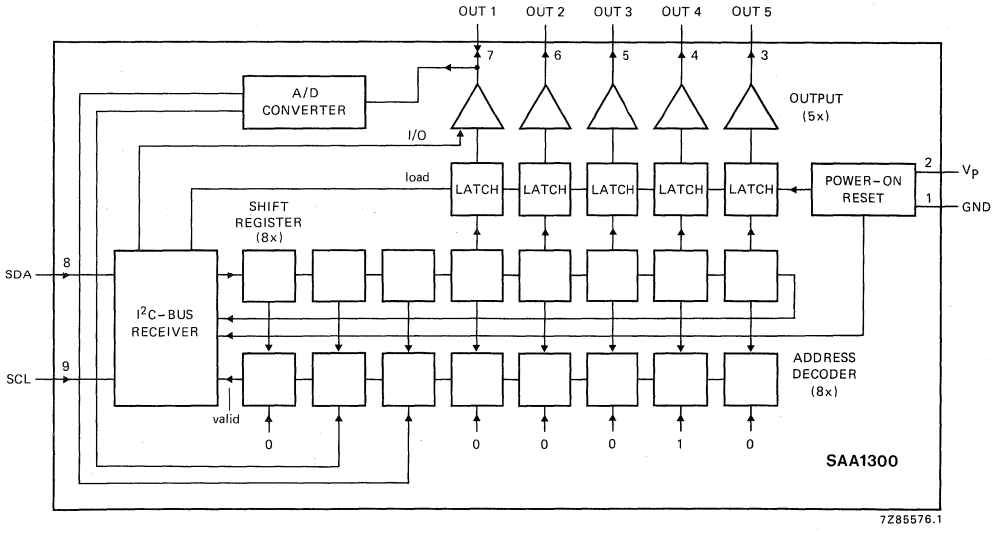


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

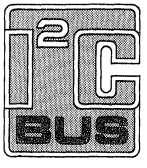
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

Data sheet	
status	Preliminary specification
date of issue	January 1991

SAA1310

Control interface for VHS video recorders

FEATURES

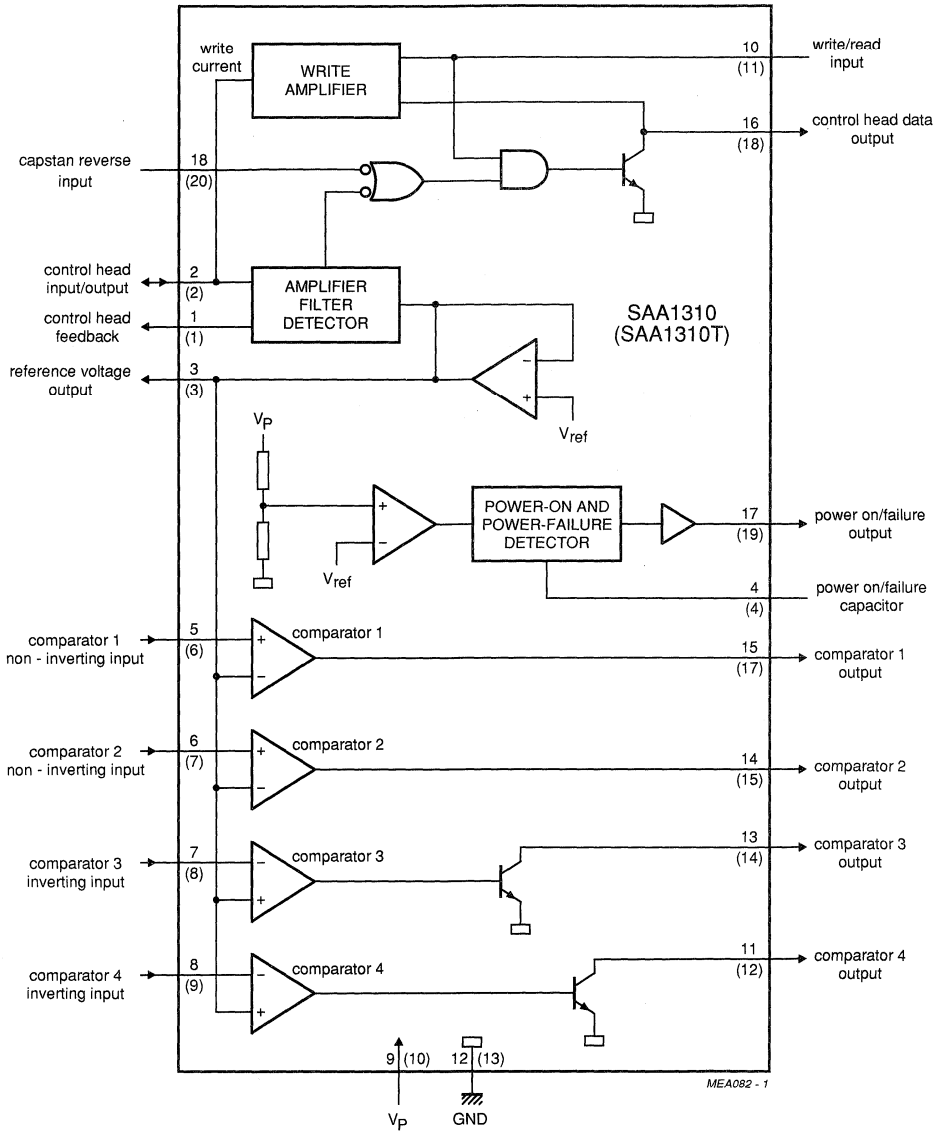
- Full support of VISS and VASS mode (VHS Index/Address Search System
- Read, write and overwrite of Tape Control/head signal (CTL)
- Power-ON and power-failure indicator
- 4 general purpose comparators for interface between sensors and microprocessor
- 2 comparators have a 100 mA output driver
- PAL and NTSC compatible

GENERAL DESCRIPTION

The SAA1310 provides an interface between the tape control head in the VHS deck-electronics.
The circuit also includes an interface between sensors in the deck mechanics and the microprocessor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1310	18	DIL	plastic	SOT102
SAA1310T	20	SO	plastic	SOT163



Pin numbers in parenthesis refer to the SAA1310T.

Fig.1 Block diagram.

PIN CONFIGURATION

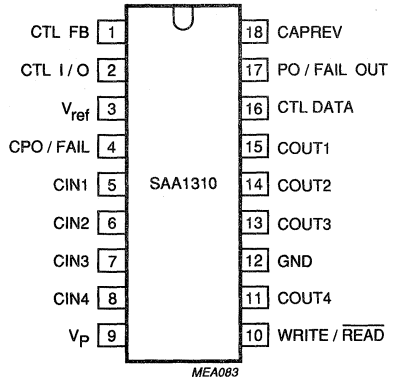


Fig.2 (a) Pin configuration for SAA1310.

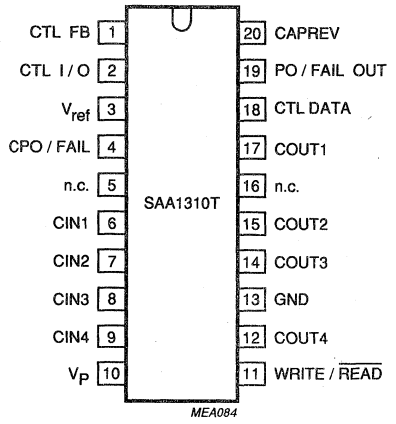


Fig.2 (b) Pin configuration for SAA1310T.

PINNING (pins in parenthesis refer to SAA1310T)

SYMBOL	PIN	DESCRIPTION
CTL FB	1 (1)	control head feedback
CTL I/O	2 (2)	control head input/output
V_{ref}	3 (3)	reference voltage output
CPO/FAIL	4 (4)	power on/failure capacitor
CIN1	5 (6)	comparator 1 input
CIN2	6 (7)	comparator 2 input
CIN3	7 (8)	comparator 3 input
CIN4	8 (9)	comparator 4 input
V_P	9 (10)	supply voltage
WRITE/$\overline{READ}$	10 (11)	write/read input
COUT4	11 (12)	comparator 4 output
GND	12 (13)	ground
COUT3	13 (14)	comparator 3 output
COUT2	14 (15)	comparator 2 output
COUT1	15 (17)	comparator 1 output
CTL DATA	16 (18)	control head data output
PO/FAIL OUT	17 (19)	power on/failure output
CAPREV	18 (20)	capstan reverse input

LIMITING VALUES (pin numbers in parenthesis refer to SAA1310T)

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		0	6.0	V
V_I/V_O	voltage on all pins	except pins 11 (12) and 13 (14)	0	V_P	V
V_O	output voltage on pins 11 (12) and 13 (14)		0	18	V
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	ambient temperature range		0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
R_{th}	thermal resistance (SAA1310)	75	-	K/W
R_{th}	thermal resistance (SAA1310T)	90	-	K/W

CHARACTERISTICS (pin numbers in parenthesis refer to SAA1310T)

V_P = 5 V; T_{amb} = 25 °C; all voltage referenced to pin 12 (13); according to the test set-up (see Fig.4); unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
P_d	power dissipation	note 1	-	85	-	mW
Supply pin 9 (10)						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current	read mode	10	15	20	mA
		write mode; duty factor = 50%	13	18	24	mA
CTL I/O pin 2 (2)						
READ MODE PIN 10 (11) < 0.5 V						
V_I	input voltage (peak-to-peak value)	f = 500 Hz	0.35	-	-	mV
		f = 30 kHz; non-linear operation	-	-	200	mV
B	bandwidth low-pass filter		-	3	-	kHz
I_b	input bias current	read mode	-	0.1	-	µA
WRITE MODE PIN 10 (11) > 3.5 V						
V_O	output voltage LOW	$I_{CTL\ I/O}$ = 3 mA; pin CTL DATA = HIGH	-	-	0.4	V
V_O	output voltage HIGH	$I_{CTL\ I/O}$ = −3 mA; pin CTL DATA = LOW	4.6	-	-	V
WRITE/$\overline{\text{READ}}$ pin 10 (11)						
V_I	input voltage	read mode	-	-	0.5	V
		write mode; analog	1.6	-	3.3	V
I_I	input current	read mode	-	-1.5	-	µA
		write mode	-	0.1	-	µA
V_{ref} pin 3 (3); note 2						
V_O	output voltage		2.4	2.5	2.6	V
I_{tot}	total current	including write current	−4	-	+4	mA
R_O	output resistance		-	0.4	0.6	Ω
CAPREV pin 18 (20)						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	V_{CAPREV} = 5 V	-	-	10	µA
I_{IH}	input current LOW	V_{CAPREV} = 0 V	−10	-	-	µA
CTL DATA pin 16 (18)						
WRITE MODE						
V_{IH}	input voltage HIGH		2.0	-	-	V
V_{IL}	input voltage LOW		-	-	0.8	V
I_{IH}	input current HIGH	$V_{CTL\ DATA}$ = 5 V	-	-	10	µA
I_{IL}	input current LOW	$V_{CTL\ DATA}$ = 0 V	−10	-	-	µA
READ MODE						
V_{OL}	output voltage LOW	I_{OL} = 0.5 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −50 µA	2.4	-	-	V

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
CPO/FAIL and PO/FAIL OUT pin 4 (4) and 17 (19); see Fig.3						
V_O	operating voltage range	at decreasing V_P	1.5	-	5.5	V
V_{OL}	output voltage LOW	I_{OL} = 1 mA	-	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	V_P−0.9	-	-	V
t_d	delay time	C_{CAPREV} = 68 nF	-	50	-	ms
V_{TL1}	threshold level 1		4.5	-	4.8	V
V_{TL2}	threshold level 2		-	3.5	-	V
I_O	source current pin 4		-	−3	-	µA
I_O	sink current pin 4		-	300	-	µA
$V_{O(min.)}$	minimum output voltage		-	20	-	mV
$V_{O(max.)}$	maximum output voltage		-	2.1	-	V
High output current type comparators						
CIN3 and CIN4 pins 7 (8) and 8 (9)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_{IL}	input current LOW	CIN3 = CIN4 = 0 V	−1	-	-	µA
I_{IH}	input current HIGH	CIN3 = CIN4 = V_P	-	-	+1	µA
COUT3 and COUT4 pins 13 (14) and 11 (12)						
V_{OL}	output voltage LOW	I_{OL} = 100 mA I_{OL} = 2 mA	- -	- -	1.0 0.4	V V
$\pm I_{OL}$	leakage current	output voltage HIGH; COUT3 = COUT4 = 17 V	-	-	1	µA
t_{tr}	transient time	note 3	-	0.5	-	µs
T_j	thermal protection		-	130	-	°C
Low output current type comparators						
CIN1 AND CIN2 pins 5 (6) and 6 (7)						
V_{hys}	input hysteresis		-	10	-	mV
V_{IL}	input voltage LOW		-	-	V_{ref} −10 mV	V
V_{IH}	input voltage HIGH		V_{ref} +10 mV	-	-	V
I_I	input current	CIN1 = CIN2 = 0 V CIN1 = CIN2 = V_P	−1 -	- -	- +1	µA µA
COUT1 AND COUT2 pins 15 (17) and 14 (15)						
V_{OL}	output voltage HIGH	I_{OH} = −100 µA	4.5	-	-	V
V_{OH}	output voltage LOW	I_{OL} = 2 mA	-	-	1	V
t_{tr}	transient time	note 4	-	0.5	-	µs

Notes to the characteristics

1. Without the sink current of the comparators; in write mode.

2. Minimum value of capacitor connected to this pin is 4.7 µF.

3. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 250 Ω resistor.

4. V_i = 100 mV p-p. Inputs connected to V_{ref} via a 10 kΩ resistor; outputs connected to V_P via a 2.5 kΩ resistor.

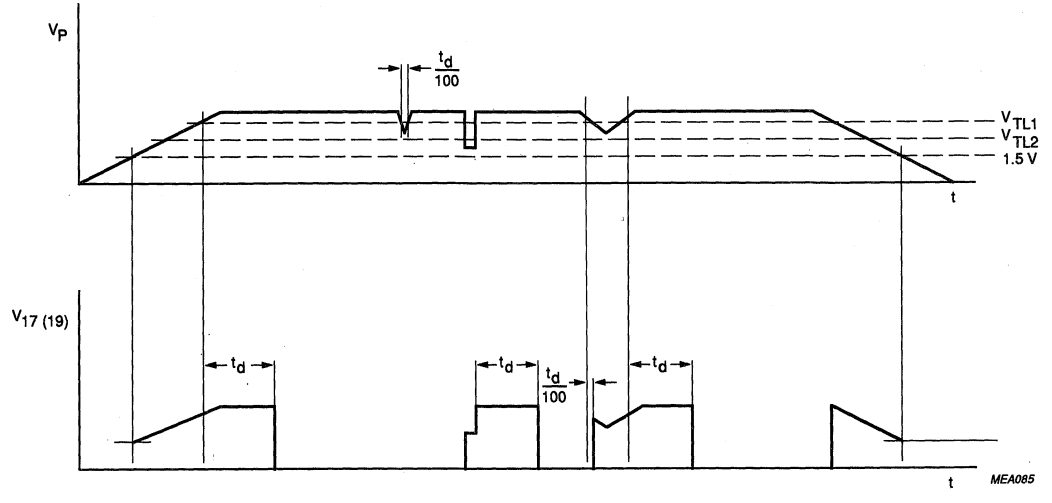
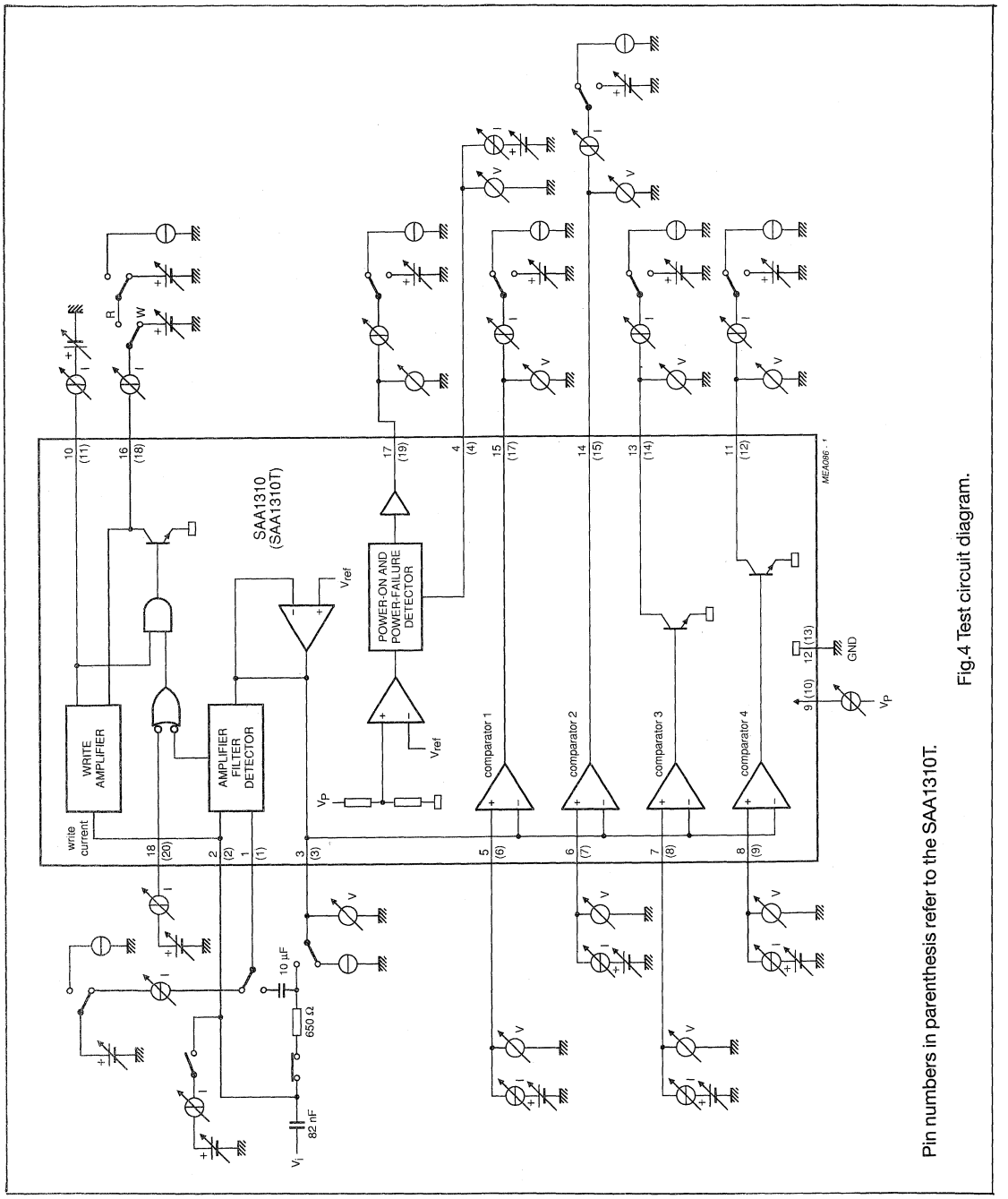


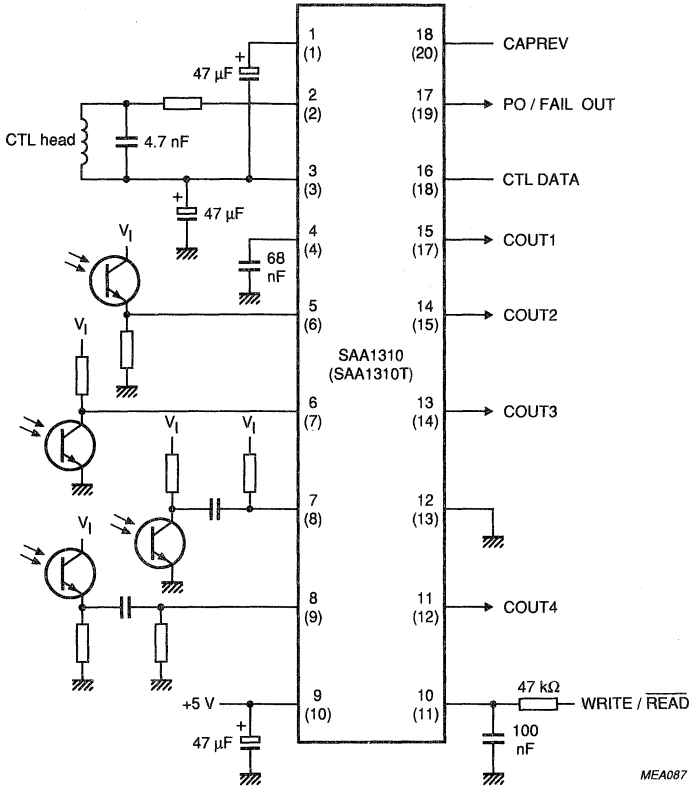
Fig.3 Power-ON and power-failure detector.

APPLICATION INFORMATION



Pin numbers in parenthesis refer to the SAA1310T.

Fig.4 Test circuit diagram.



Pin numbers in parenthesis refer to the SAA1310T.

Fig.5 Application diagram.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT146).
SAA3004T: 20-lead mini-pack; plastic (SO20; SOT163A).

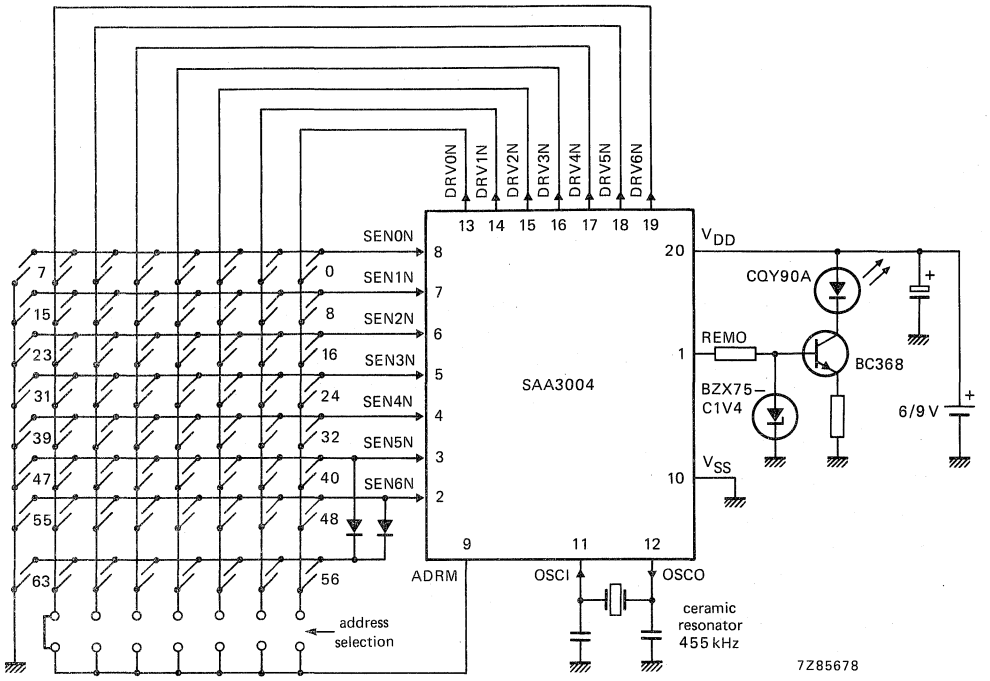


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

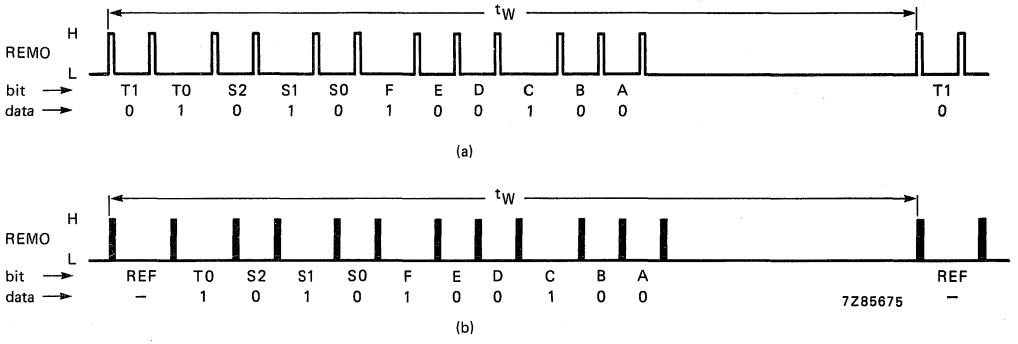
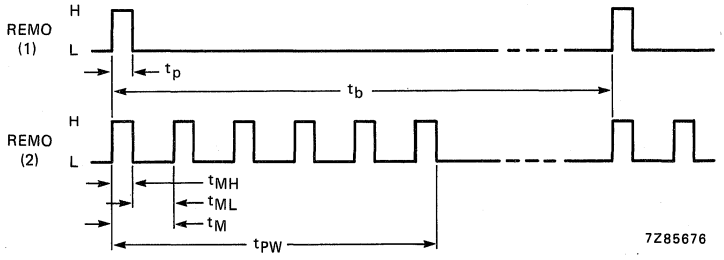


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

DEVELOPMENT DATA

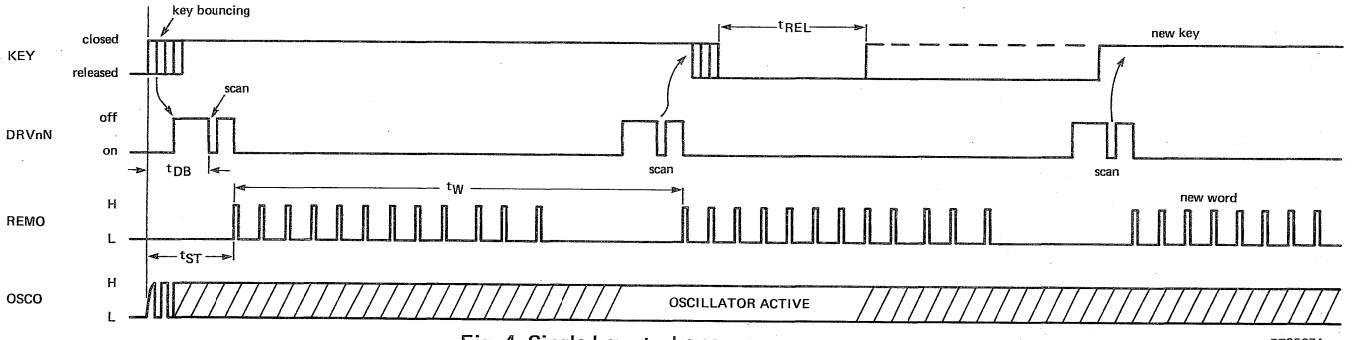


Fig. 4 Single key-stroke sequence.
Debounce time: t_{DB} = 4 to 9 x T_o.
Start time: t_{ST} = 5 to 10 x T_o.
Minimum release time: t_{REL} = T_o.
Word distance: t_W.

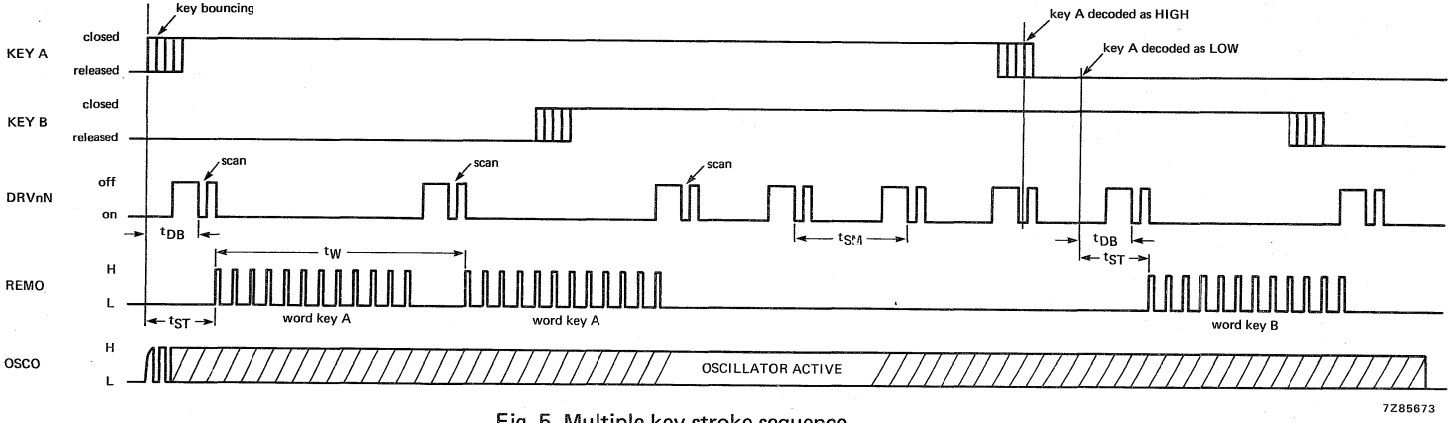


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: t_{SM} = 6 to 10 x T_o.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p μs	t_M μs	t_{ML} μs	t_{MH} μs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	o						
	2	0	0	1	X	o					
	3	0	1	0	X	X	o				
	4	0	1	1	X	X	X	o			
	5	1	0	0	X	X	X	X	o		
	6	1	0	1	X	X	X	X	X	o	
MODULATED	0	1	1	1							o
	1	0	0	0	o						o
	2	0	0	1	X	o					o
	3	0	1	0	X	X	o				o
	4	0	1	1	X	X	X	o			o
	5	1	0	0	X	X	X	X	o		o
	6	1	0	1	X	X	X	X	X	o	o

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1	**			8 to 15
*	SEN2N	0	1	0	**			16 to 23
*	SEN3N	0	1	1	**			24 to 31
*	SEN4N	1	0	0	**			32 to 39
*	SEN5N	1	0	1	**			40 to 47
*	SEN6N	1	1	0	**			48 to 55
*	SEN5N and SEN6N	1	1	1	**			56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

DEVELOPMENT DATA

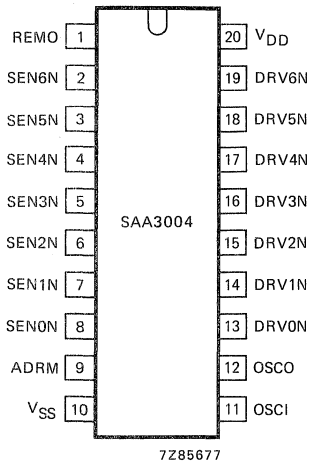


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	μA μA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	μA μA
Input leakage current V_I = V_{DD}	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	μA μA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	μA μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

INFRARED REMOTE CONTROL TRANSMITTER (RECS 80 LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3008 transmitter IC is designed for infrared remote control systems. It has a capacity for 1280 commands arranged in 20 sub-system address groups of 64 commands each. The subsystem address may be selected by press-button, slider switches or be hard-wired.

Commands are transmitted in patterns which are pulse distance coded. Modulated pulse transmissions allow a narrow-band receiver to be used for improved noise rejection. The modulation frequency of the SAA3008 is 38 kHz which is 1/12 of the oscillator frequency of 455 kHz (typical).

Features

- Modulated transmission
- Ceramic resonator controlled frequency
- Data-word-start with reference time of unique start pattern
- Supply voltage range 2 V to 6.5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups
- Up to 64 commands per subsystem address

  } up to 1280 commands

- Requires few additional components

PACKAGE OUTLINES

SAA3008P: 20-lead DIL; plastic (SOT146).
SAA3008T: 20-lead mini-pack; plastic (SO20; SOT163A).

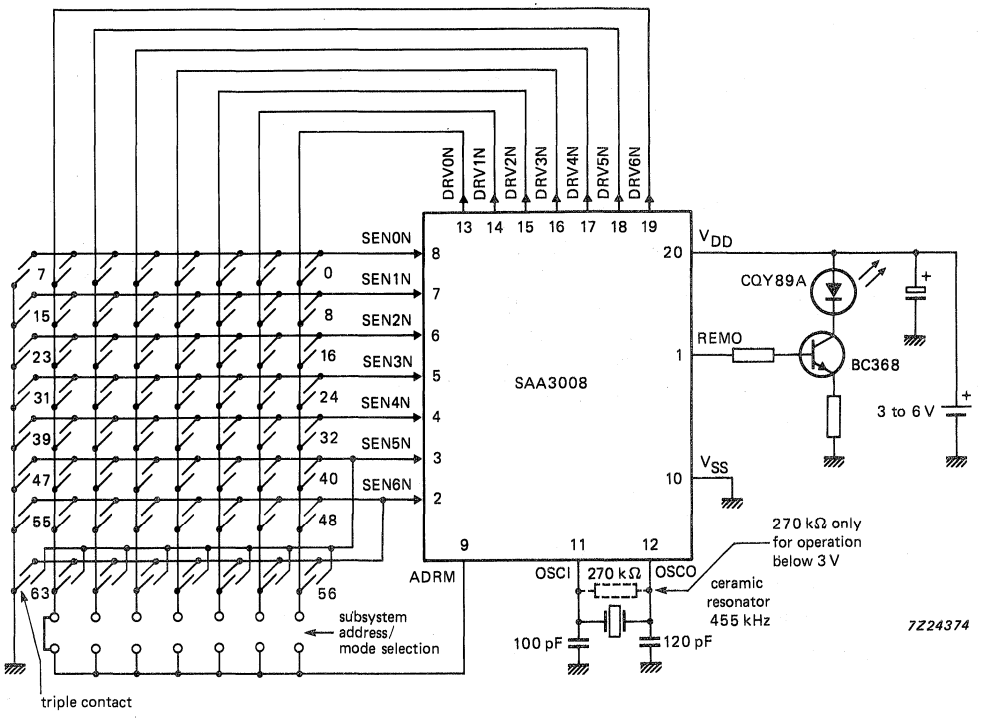


Fig.1 SAA3008 application example.

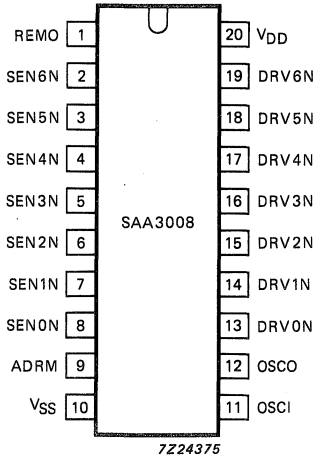


Fig.2 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	sense inputs from key matrix
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address/mode control input
10	V_{SS}	ground (0 V)
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	drive outputs to key matrix
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Key matrix (DRV0N - DRV6N and SEN0N - SEN6N)

The transmitter keyboard is arranged as a scanned matrix with seven driver outputs (DRV0N to DRV6N) and seven sensing inputs (SEN0N to SEN6N) as shown in Fig.1. The driver outputs are open-drain n-channel transistors which are conductive in the stand-by mode. The sensing inputs enable the generation of 56 command codes. With two external diodes connected (or triple contact), as in Fig.1, all 64 commands are addressable. The sense lines have p-channel pull-up transistors, so that they are HIGH until pulled LOW by connecting them to an output via a key depression to initiate a code transmission.
The maximum allowable value of contact series resistance for keyboard switches in the ON-state is 7 kΩ.

Address/mode input (ADRM)

Subsystem addresses are defined by connecting one or two of the key matrix driver lines (DRV0N to DRV6N) to the ADRM input. This allows up to 20 subsystem addresses to be generated for the REMO output (bits S3, S2, S1 and S0) as shown in Table 1 and Fig.3.

The transmission mode is defined by the DRV6N to ADRM connection as follows:

- Mode 1 DRV6N not connected to ADRM
- Mode 2 DRV6N connected to ADRM

In Mode 1 the reference time REF equals 3To, this may be used as a reference time for the decoding sequence. In Mode 2 an additional modulated pulse has been inserted into the middle of the reference time, therefore, these pulses are now separated by 1.5To. This unique start pattern START uses the detection of a beginning word (see Fig.3).
When more than one connection is made to ADRM then all connections should be decoupled using diodes.

The ADRM input has switched pull-up and pull-down loads. In the standby mode only pull-down load is active and ADRM input is held LOW (this condition is independent of the ADRM circuit configuration and minimizes power loss in the standby mode). When a key is pressed the transmitter becomes active (pull-down is switched OFF, pull-up is switched ON) and the driver line signals are sensed for the subsystem address coding.

The subsystem address is sensed only within the first scan cycle, whereas the command code is sensed in every scan. The transmitted subsystem address remains unchanged if the subsystem address selection is changed while the command key is pressed. A change of the subsystem address does not start a transmission.

In a multiple keystroke sequence (Fig.6) the second word B might be transmitted with subsystem address 18 or 19 instead of the preselected subsystem address (Table 1). This is only relevant for systems decoding subsystem address 18 or 19.

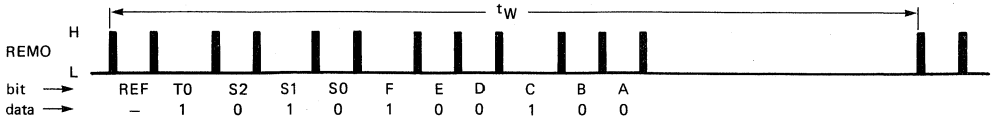
Remote control signal output (REMO)

The REMO output driver stage incorporates a bipolar emitter-follower which allows a high output current in the output active (HIGH) state (Fig.7).
The information is defined by the distance 't_b' between the leading edges of the modulated pulses (Fig.4). The distance t_b is a multiple of the basic unit T_O (Table 3) which equals 1152 periods of the oscillator frequency f_{osc} (Table 3). The pulses are modulated with 6 periods of 1/12 of the oscillator frequency (38 kHz).
The format of the output data is illustrated in Figs 3 and 4.
A data word starts with the reference time and toggle bit T0 and is followed by the definition bits for the subsystem address S3, S2, S1 and S0 (bit S3 is transmitted only for subsystem addresses 8 to 20).
The selected command key is defined by bits F, E, D, C, B and A as shown in Table 2.

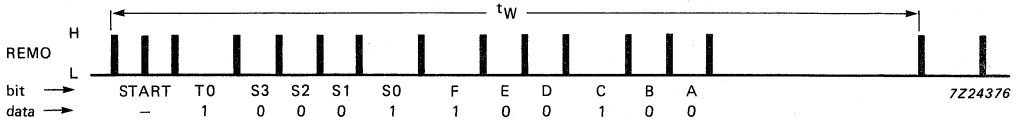
DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The toggle bit T0 acts as an indication for the decoder whether the next instruction should be considered as a new command or not. The codes for the subsystem address and the selected key are given in Table 3.



(a) Transmission with reference time and subsystem addresses 1 to 7.



(b) Transmission with start-pattern and subsystem addresses 8 to 20.

Where:

Reference time	
start pattern T0	toggle bit
S3, S2, S1, S0	subsystem address
A to F	command bits
t_W	word length
binary values	determined by pulse spacing

Fig.3 Data format of remote control signal (REMO).

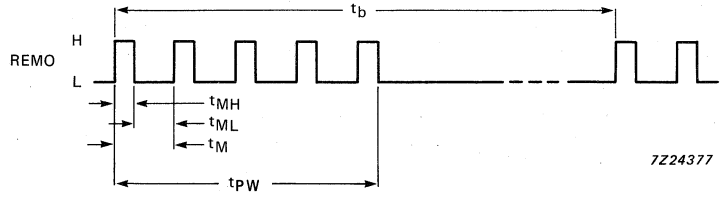


Fig.4 Waveform for one pulse period at REMO output; for timing values see Table 3.

Oscillator (OSCI, OSCO)

The external components for the oscillator circuit are connected to OSCI and OSCO. The oscillator operates with a ceramic resonator in the frequency range 350 kHz to 500 kHz, as defined by the resonator. When operating at a supply voltage of below 3 V a 270 kHz resistor should be connected in parallel with the resonator.

DEVELOPMENT DATA

Table 1 Definition of subsystem addresses

address number	driver line(s) connected to ADRM	subsystem address S3	S2	S1	S0
1	no connection	–	1	1	1
2	DRV0N	–	0	0	0
3	DRV1N	–	0	0	1
4	DRV2N	–	0	1	0
5	DRV3N	–	0	1	1
6	DRV4N	–	1	0	0
7	DRV5N	–	1	0	1
8	DRV0N and DRV2N	0	0	0	0
9	DRV0N and DRV3N	1	0	0	0
10	DRV0N and DRV4N	0	1	0	0
11	DRV0N and DRV5N	1	1	0	0
12	DRV1N and DRV2N	0	0	0	1
13	DRV1N and DRV3N	1	0	0	1
14	DRV1N and DRV4N	0	1	0	1
15	DRV1N and DRV5N	1	1	0	1
16	DRV2N and DRV3N	1	0	1	0
17	DRV2N and DRV4N	0	1	1	0
18	DRV2N and DRV5N	1	1	1	0
19	DRV3N and DRV4N	0	1	1	1
20	DRV3N and DRV5N	1	1	1	1

Table 2 Definition of command codes

key pressed	drive-to-sense connection made	command code generated F	EE	D	C	B	A
0	DRV0N to SEN0N	0	0	0	0	0	0
1	DRV1N to SEN0N	0	0	0	0	0	1
2	DRV2N to SEN0N	0	0	0	0	1	0
3	DRV3N to SEN0N	0	0	0	0	1	1
4	DRV4N to SEN0N	0	0	0	1	0	0
5	DRV5N to SEN0N	0	0	0	1	0	1
6	DRV6N to SEN0N	0	0	0	1	1	0
7	DRV7N to SEN0N	0	0	0	1	1	1
8	DRV0N to SEN1N	0	0	1	0	0	0
9	DRV1N to SEN1N	0	0	1	0	0	1
10	DRV2N to SEN1N	0	0	1	0	1	0
11	DRV3N to SEN1N	0	0	1	0	1	1
12	DRV4N to SEN1N	0	0	1	1	0	0
13	DRV5N to SEN1N	0	0	1	1	0	1
14	DRV6N to SEN1N	0	0	1	1	1	0
15	DRV7N to SEN1N	0	0	1	1	1	1
16	DRV0N to SEN2N	0	1	0	0	0	0
17	DRV1N to SEN2N	0	1	0	0	0	1
18	DRV2N to SEN2N	0	1	0	0	1	0
19	DRV3N to SEN2N	0	1	0	0	1	1
20	DRV4N to SEN2N	0	1	0	1	0	0

Table 2 Definition of command codes (continued)

key pressed	drive-to-sense connection made	command code generated F	E	D	C	B	A
21	DRV5N to SEN2N	0	1	0	1	0	1
22	DRV6N to SEN2N	0	1	0	1	1	0
23	DRV7N to SEN2N	0	1	0	1	1	1
24	DRV0N to SEN3N	0	1	1	0	0	0
25	DRV1N to SEN3N	0	1	1	0	0	1
26	DRV2N to SEN3N	0	1	1	0	1	0
27	DRV3N to SEN3N	0	1	1	0	1	1
28	DRV4N to SEN3N	0	1	1	1	0	0
29	DRV5N to SEN3N	0	1	1	1	0	1
30	DRV6N to SEN3N	0	1	1	1	1	0
31	DRV7N to SEN3N	0	1	1	1	1	1
32	DRV0N to SEN4N	1	0	0	0	0	0
33	DRV1N to SEN4N	1	0	0	0	0	1
34	DRV2N to SEN4N	1	0	0	0	1	0
35	DRV3N to SEN4N	1	0	0	0	1	1
36	DRV4N to SEN4N	1	0	0	1	0	0
37	DRV5N to SEN4N	1	0	0	1	0	1
38	DRV6N to SEN4N	1	0	0	1	1	0
39	DRV7N to SEN4N	1	0	0	1	1	1
40	DRV0N to SEN5N	1	0	1	0	0	0
41	DRV1N to SEN5N	1	0	1	0	0	1
42	DRV2N to SEN5N	1	0	1	0	1	0
43	DRV3N to SEN5N	1	0	1	0	1	1
44	DRV4N to SEN5N	1	0	1	1	0	0
45	DRV5N to SEN5N	1	0	1	1	0	1
46	DRV6N to SEN5N	1	0	1	1	1	0
47	DRV7N to SEN5N	1	0	1	1	1	1
48	DRV0N to SEN6N	1	1	0	0	0	0
49	DRV1N to SEN6N	1	1	0	0	0	1
50	DRV2N to SEN6N	1	1	0	0	1	0
51	DRV3N to SEN6N	1	1	0	0	1	1
52	DRV4N to SEN6N	1	1	0	1	0	0
53	DRV5N to SEN6N	1	1	0	1	0	1
54	DRV6N to SEN6N	1	1	0	1	1	0
55	DRV7N to SEN6N	1	1	0	1	1	1
56	DRV0N to SEN5N and SEN6N	1	1	1	0	0	0
57	DRV1N to SEN5N and SEN6N	1	1	1	0	0	1
58	DRV2N to SEN5N and SEN6N	1	1	1	0	1	0
59	DRV3N to SEN5N and SEN6N	1	1	1	0	1	1
60	DRV4N to SEN5N and SEN6N	1	1	1	1	0	0
61	DRV5N to SEN5N and SEN6N	1	1	1	1	0	1
62	DRV6N to SEN5N and SEN6N	1	1	1	1	1	0
63	DRV7N to SEN5N and SEN6N	1	1	1	1	1	1

Table 3 Pulse timing

parameter	symbol	duration	duration at f_{osc} = 455 kHz; t_{osc} = 2.2 μs
Modulation period	t_M	$12t_{osc}$	26.4 μs
Modulation LOW time	t_{ML}	$8t_{osc}$	17.6 μs
Modulation HIGH time	t_{MH}	$4t_{osc}$	8.8 μs
Modulation pulse width	t_{PW}	$5t_M + t_{MH}$	140.8 μs
Basic unit of pulse spacing	t_o	$1152t_{osc}$	2.53 ms
Word length for subsystem addresses			
0 to 7	t_W	$55296t_{osc}$	121.44 ms
8 to 20	t_W	$59904t_{osc}$	132.56 ms
Pulse separation for			
logic 0	t_b	$2t_o$	5.06 ms
logic 1	t_b	$3t_o$	7.59 ms
reference time	t_b	$3t_o$	7.59 ms
toggle bit	t_b	$2t_o$	5.06 ms
		$3t_o$	7.59 ms
Start pattern	t_b	$2 \times 1.5t_o$	2 x 3.79 ms

DEVELOPMENT DATA

OPERATION

Keyboard

In the standby mode all drivers DRV0N-DRV6N are ON but are non-conducting due to their open drain configuration. When a key is pressed, a completed drain connection pulls down one or more of the sense lines to ground. Referring to Fig.5, the power-up sequence for the IC commences as a key is pressed. The oscillator becomes active and then, following the debounce time (t_{DB}), the output drivers become active successively.

Within the first scan cycle the transmission mode, subsystem address and the selected command code are sensed and loaded into an internal data latch. In a multiple keystroke sequence (Fig.6) the command code is always altered according to the sensed key.

Multiple keystroke protection

The keyborad is protected against multiple keystrokes. If more than one key is pressed the circuit will not generate a new REMO sequence (Fig.6).
In a multiple keystroke sequence the scan repetition rate is increased to detect the release of the key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching directly to ground (codes 7, 15, 23, 31, 39, 47, 55, 63) are not completely covered by multiple keystroke protection. If one sense input is switched to ground, other keys on that sense line are ignored.
- The sense lines SEN5N and SEN6N are not protected against multiple keystrokes on the same driver line because this has been used to define codes 56 to 63.

OPERATION (continued)

Output sequence

The output operation starts when the code of the selected key has been loaded into the internal command register. A burst of pulses, including the latched address and command codes, is generated at the output REMO for as long as the key is pressed. The format of the output pulse train is as shown in Figs 3 and 4. The operation is terminated by releasing the key, or by pressing more than one key at the same time. Once a sequence has been started, the transmitted words will always be completed after the key has been released.
The toggle bit T0 is incremented if the key is released for a minimum time t_{REL} (Fig.5). In a multiple keystroke sequence the toggle bit remains unchanged.

DEVELOPMENT DATA

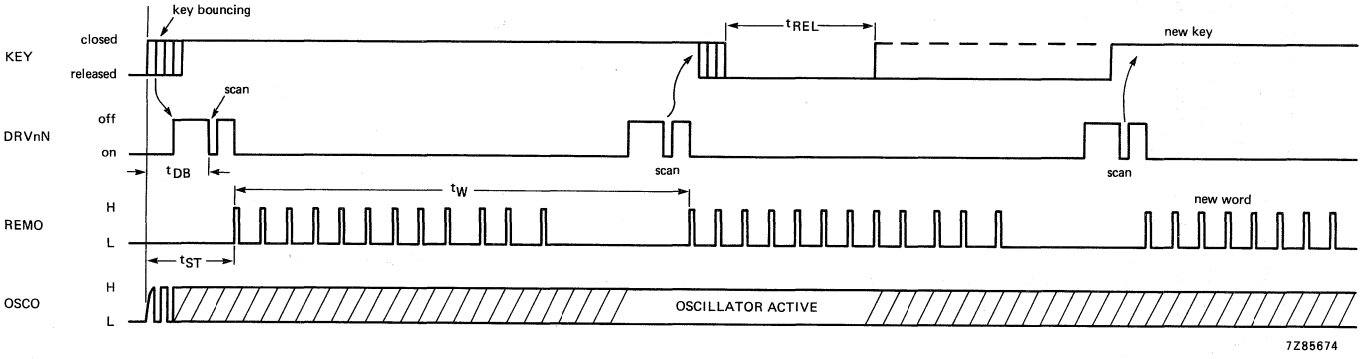


Fig.5 Single keystroke sequence; t_{DB} = debounce time = $4T_o$ to $9T_o$; t_{ST} = start time = $5T_o$ to $10T_o$; t_{REL} = minimum release time = T_o; t_W = word length.

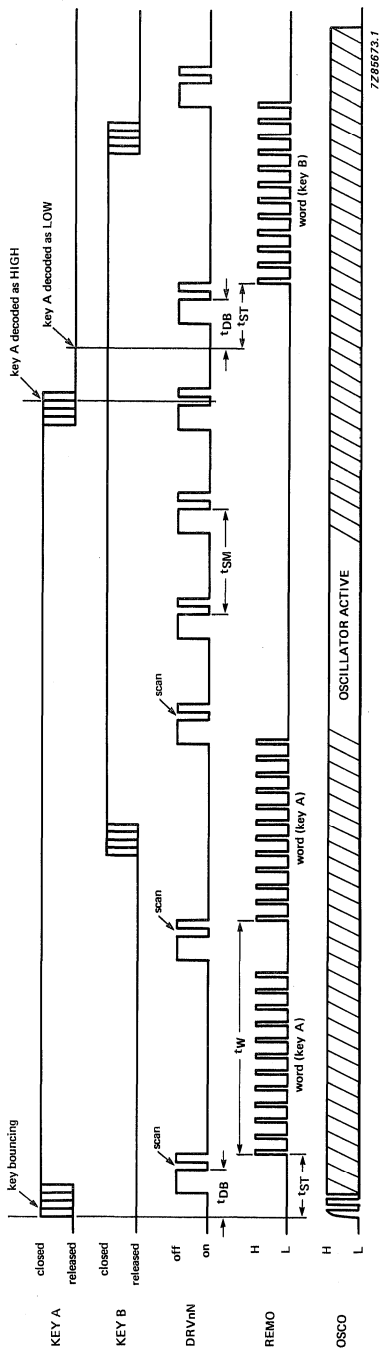


Fig.6 Scan rate multiple keystroke sequence: t_{SM} = scan rate (multiple keystroke) = $6T_O$ to $10T_O$; t_{DB}, t_{ST}, and t_W are as per Fig.5.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.3	+7	V
Input voltage range		V_I	−0.3	V_{DD} + 0.3	V
Output voltage range		V_O	−0.3	V_{DD} + 0.3	V
Total power dissipation					
DIL package (SOT146)		P_{tot}	–	300	mW
mini-pack (SO20; SOT163A)		P_{tot}	–	200	mW
Power dissipation					
matrix outputs DRV0N to DRV6N		P_O	–	50	mW
remote data output REMO		P_O	–	200	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−20	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	6.5	V
Supply current active	f_{osc} = 455 kHz;					
	V_{DD} = 3 V	I_{DD}	–	0.25	–	mA
	V_{DD} = 4.5 V	I_{DD}	–	0.5	–	mA
	V_{DD} = 6 V	I_{DD}	–	1	–	mA
Standby mode	T_{amb} = 25 °C;					
	V_{DD} = 6 V	I_{DD}	–	–	4	μA
Oscillator frequency						
(ceramic resonator)	V_{DD} = 2 to 6.5 V	f_{osc}	350	–	500	kHz
Inputs SEN0N to SEN6N						
Input voltage LOW	V_{DD} = 2 to 6.5 V	V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH	V_{DD} = 2 to 6.5 V	V_{IH}	0.7 V_{DD}	–	–	V
Input current						
(p-channel pull-up)	V_{IL} = 0 V					
	V_{DD} = 2 V	I_I	−10	–	−100	μA
	V_{DD} = 6.5 V	I_I	−100	–	−600	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs DRV0N to DRV6N (open drain 1)						
Output voltage ON	I_O = 0.25 mA; V_{DD} = 2 V	V_{OL}	–	–	0.3	V
	I_O = 2.5 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.6	V
Output current OFF	V_{DD} = 6.5 V	I_O	–	–	10	μA
Input ADRM						
Input voltage LOW		V_{IL}	–	–	0.4 V_{DD}	V
Input voltage HIGH		V_{IH}	0.85 V_{DD}	–	–	V
Input current (switched p and n channel pull-up and pull-down)						
pull-up active	V_I = 0 V					
	V_{DD} = 2 V	I_{IL}	−10	–	−100	μA
	V_{DD} = 6.5 V	I_{IL}	−100	–	−600	μA
pull-down active	V_I = V_{DD}					
	V_{DD} = 2 V	I_{IH}	10	–	100	μA
	V_{DD} = 6.5 V	I_{IH}	100	–	600	μA
Output REMO						
Output voltage HIGH	I_{OH} = −40 mA; T_{amb} = 25 °C					
	V_{DD} = 2 V	V_{OH}	0.8	–	–	V
	V_{DD} = 6.5 V	V_{OH}	5.0	–	–	V
	I_{OH} = 0.5 mA; V_{DD} = 2 V	V_{OH}	0.8 V_{DD}	–	–	V
Output voltage LOW	I_{OL} = 0.5 mA; V_{DD} = 2 V	V_{OL}	–	–	0.4	V
	I_{OL} = 2.0 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.4	V
Input OSCI						
Input current HIGH	V_{DD} = 6.5 V	I_{IH}	3.0	–	7.0	μA
Output OSCO						
Output voltage HIGH	I_{OH} = 100 μA; V_{DD} = 6.5 V	V_{OH}	V_{DD}−0.8	–	–	V
Output voltage LOW	I_{OL} = 100 μA; V_{DD} = 6.5 V	V_{OL}	–	–	0.7	V

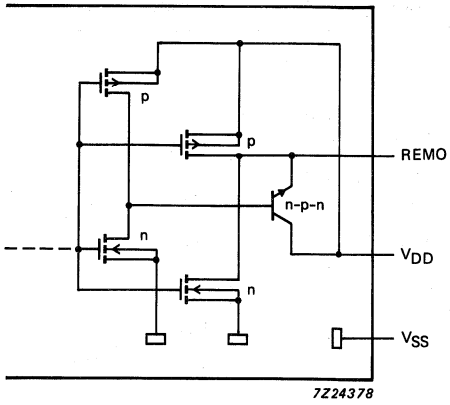


Fig.7 REMO output stage.

INFRARED REMOTE CONTROL DECODERS

GENERAL DESCRIPTION

The main function of the SAA3009 and SAA3049 ICs is to check and convert the received coded data (RECS80/RC5) into latched binary outputs. The device address can be hard-wired for a particular address allowing several devices in one location. Alternatively, received data with any address can be accepted, the received data and address are then outputs.

Features

- Decodes 64 remote control commands with a maximum of 32 subaddresses
- Accepts RECS80 codes with pulse position modulation (SAA3004, SAA3007, SAA3008) or RC5 codes with biphase transmission (SAA3006, SAA3010)
- Available at SAA3009 with 8 high current (10 mA) open-drain outputs and internal pull-ups for direct LED drive via resistors or as SAA3049 for low supply current applications
- Adding circuitry for binary decoding allows a maximum of 2048 commands to be used, for example 1-of-16 decoder (HEF4515)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009	note 1	V_{CC}	4.5	5.0	5.5	V
SAA3049	note 2	V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009	note 1	I_{CC}	–	–	70	mA
SAA3049	note 2	I_{CC}	–	1.0	2.0	mA
Oscillator frequency		f_{osc}	–	4	–	MHz
Output sink current LOW (pins 1 to 8)						
SAA3009	note 3	I_{OL}	–	–	10	mA
SAA3049	note 4	I_{OL}	1.6	3.0	–	mA

Notes to the QUICK REFERENCE DATA

1. T_{amb} = 0 to + 70 °C.
2. T_{amb} = –40 to + 85 °C.
3. Open-drain with 20 to 50 kΩ internal pull-up resistor.
4. Open-drain without internal pull-up resistor at V_{CC} = 5 V ± 10%; V_O = 0.4 V.

PACKAGE OUTLINES

SAA3009P; SAA3049P: 20 lead DIL; plastic (SOT146).
SAA3049T: 20 lead mini-pack; plastic (SO20; SOT163A).

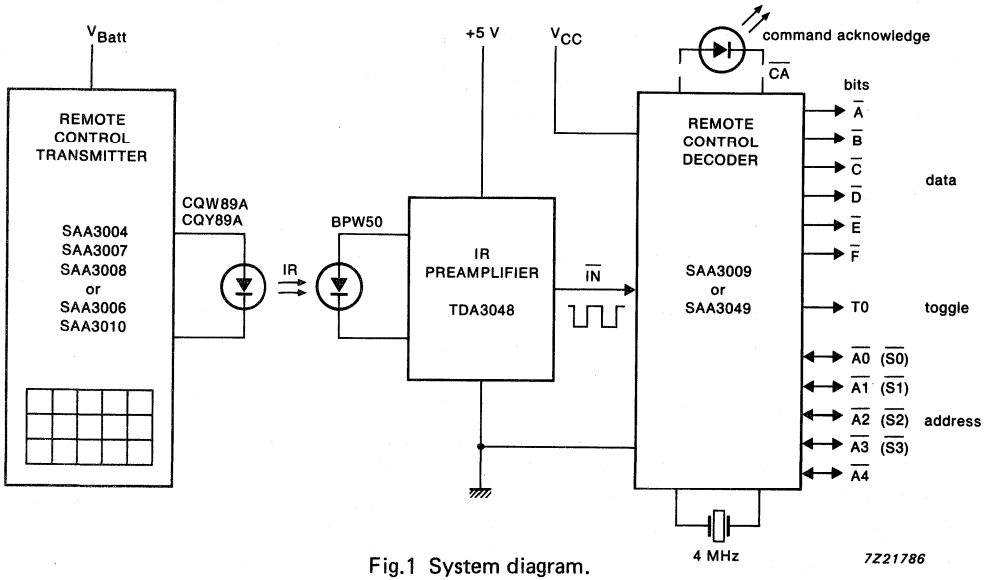


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004 V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)

SAA3007 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3008 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3006 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

SAA3010 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	$V_{CC}+0.8$	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	–	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	–	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation				
SAA3009	P_{tot}	–	1	W
SAA3049	P_{tot}	–	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+70	°C
SAA3049	T_{amb}	−40	+85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+150	°C
SAA3049	T_{stg}	−65	+150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = –40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	–0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	–0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	$I_{OH} = -50\ \mu A$	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 10$ mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 5$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	$V_{CC} = 5$ V ± 10%; $V_{OL} = 0.4$ V	I_{OL}	1.6	3.0	–	mA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 or SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

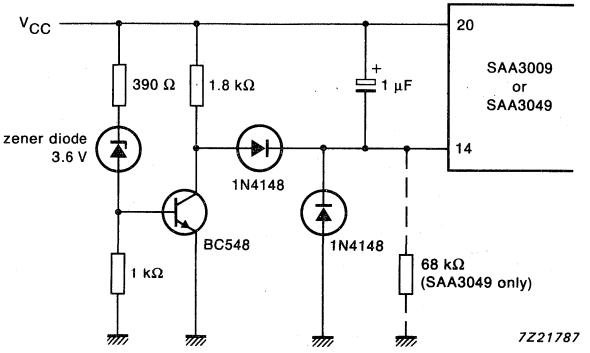


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

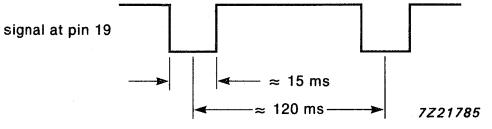
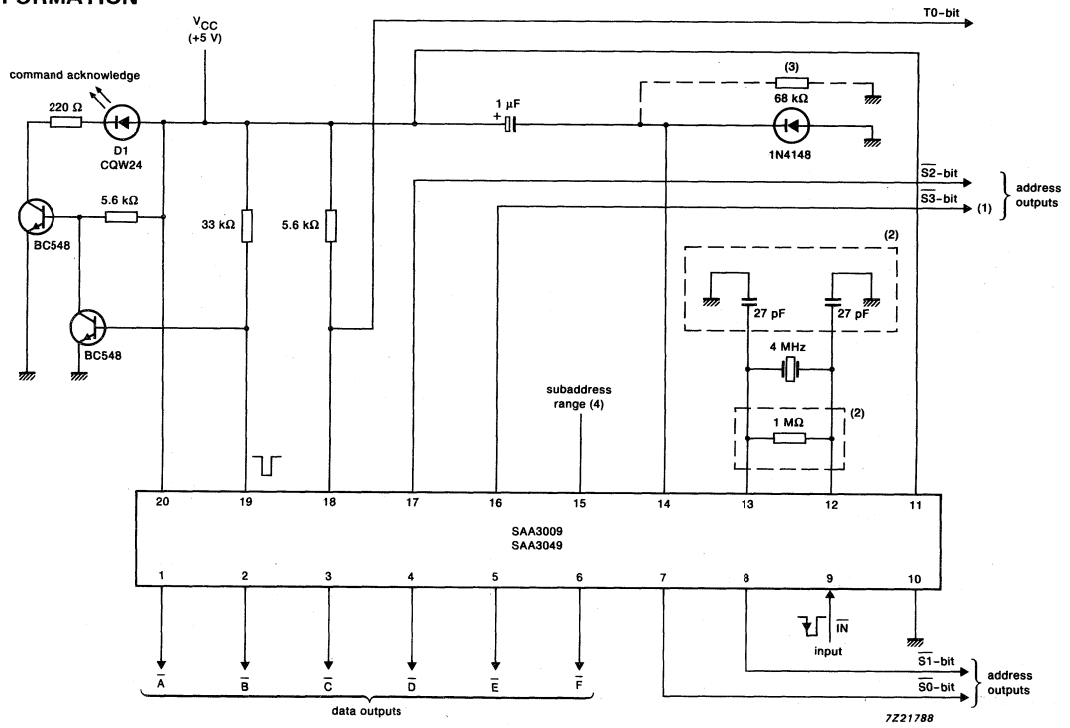


Fig.3 Output diagram of command acknowledge.

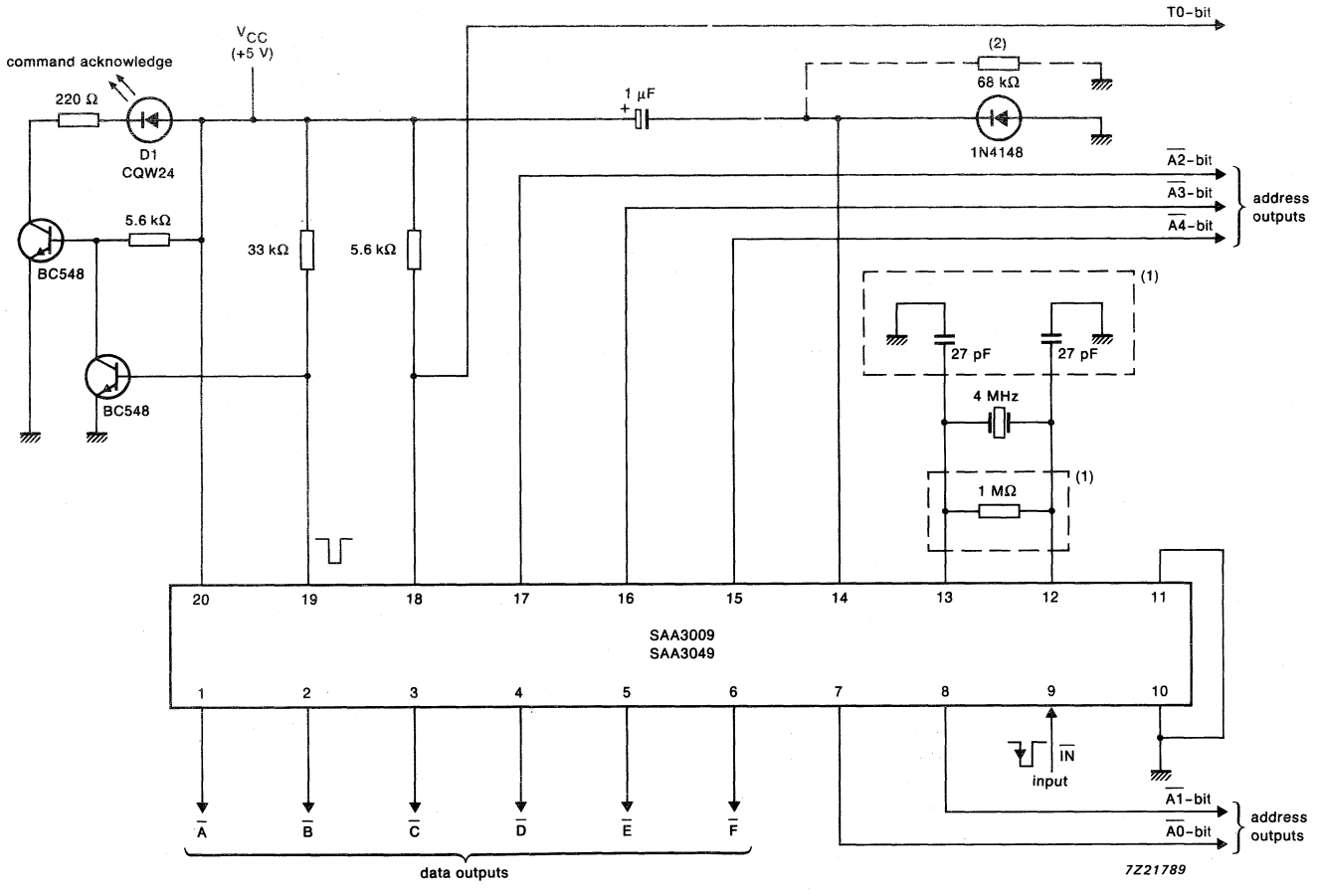
APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

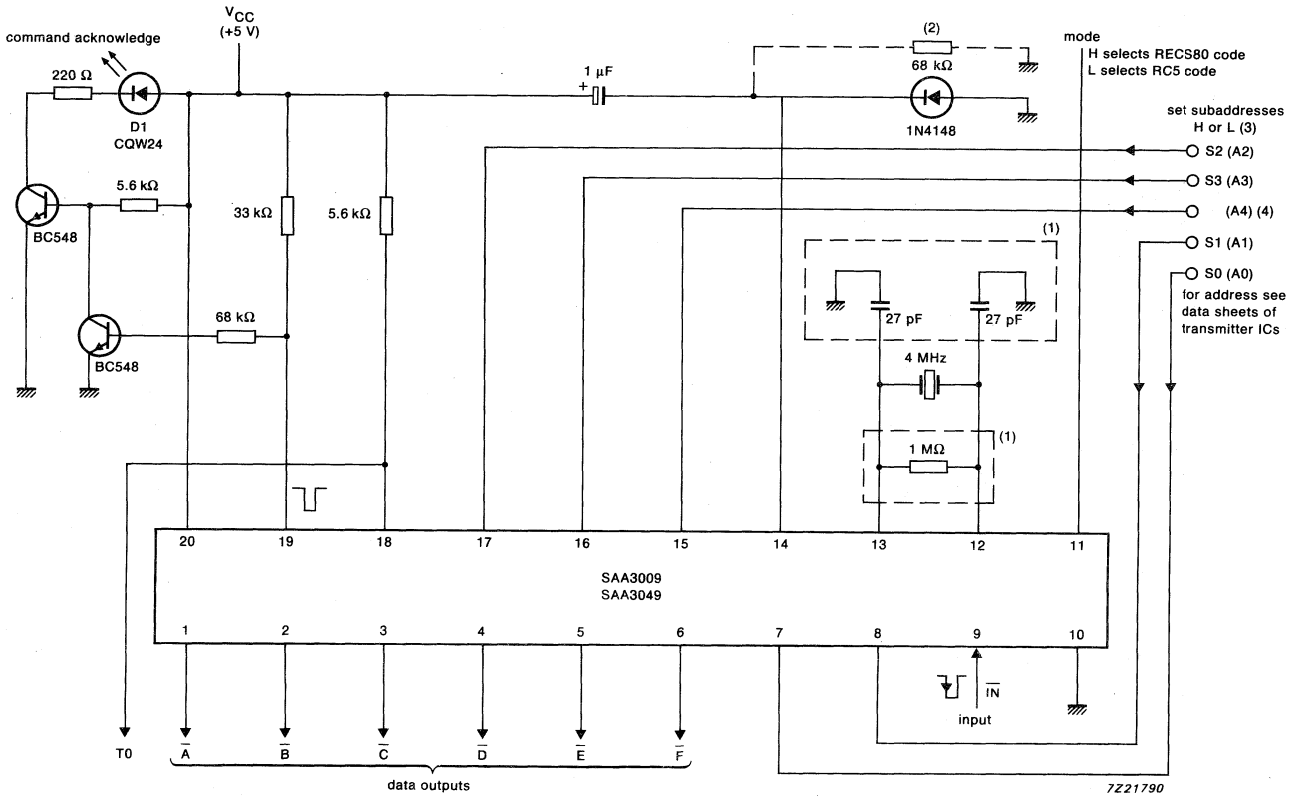
Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

APPLICATION INFORMATION (continued)



(1) only for SAA3009.
(2) only for SAA3049.

Fig.5 Remote control decoder with latched 12-bit parallel outputs (11 bits inverted) for use with transmitter types SAA3006 or SAA3010; pin 11 is LOW for RC5 code.



(1) only for SAA3009.
(2) only for SAA3049.
(3) address inputs:
when LOW address input pin is connected to ground
when HIGH address input pin is open (SAA3009)
when HIGH address input pin is connected via pull-up resistor to V_{CC} (SAA3049)
(4) subaddress range RECS80 code:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.6 Remote control decoder for up to 20 subaddresses with 6 + 1-bit parallel outputs (RECS80 code). Decoder is set for required subaddress by holding address pins HIGH or LOW. Pin 11 is HIGH for use with transmitter types SAA3004, SAA3007 or SAA3008 (RECS80 code). Pin 11 is LOW for use with transmitter types SAA3006 or SAA3010 (RC5 code). Remote control decoder for up to 32 subaddresses with 6 + 1-bit parallel outputs (RC5 code).

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

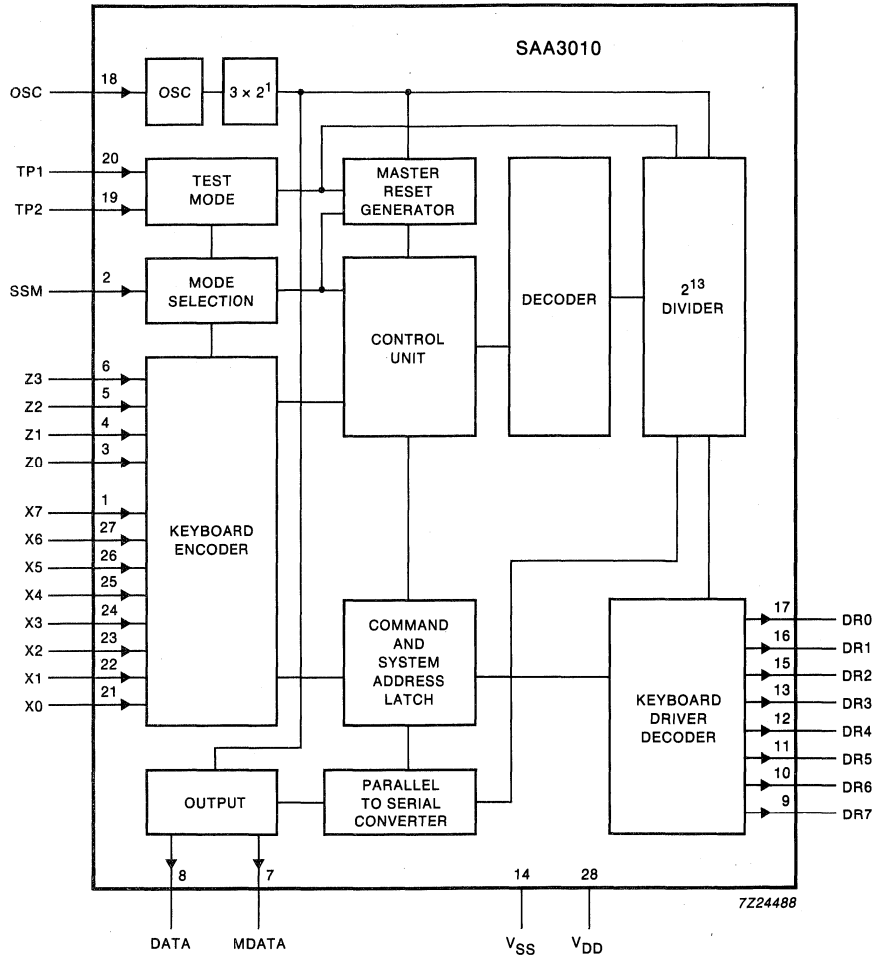


Fig.1 Block diagram.

PINNING

pin	mnemonic	function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	V_{SS}	ground (0 V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	V_{DD} (I)	voltage supply

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

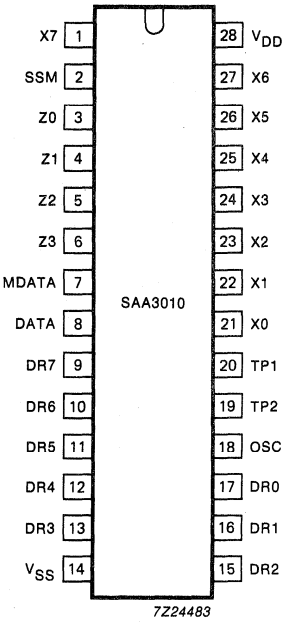


Fig.2 Pinning diagram.

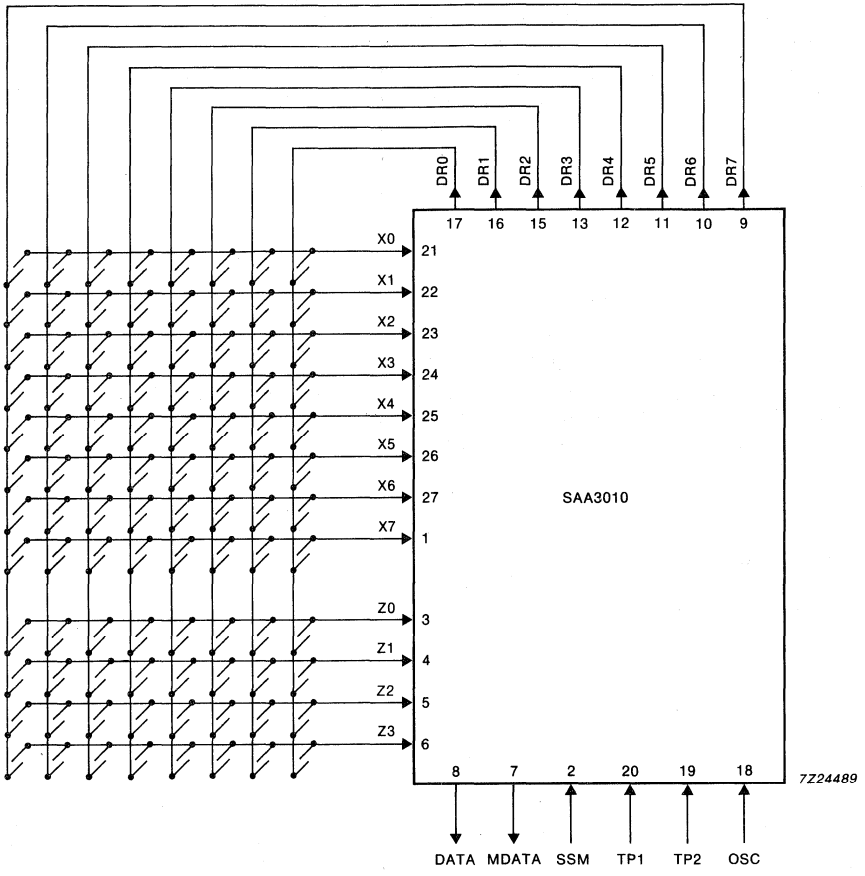


Fig.3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).

When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.

The maximum value of the contact series resistance of the switched keyboard is 7 kΩ.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.4 and Tables 1 and 2. The code is transmitted using a biphase technique as illustrated by Fig.5. The code consists of four parts:

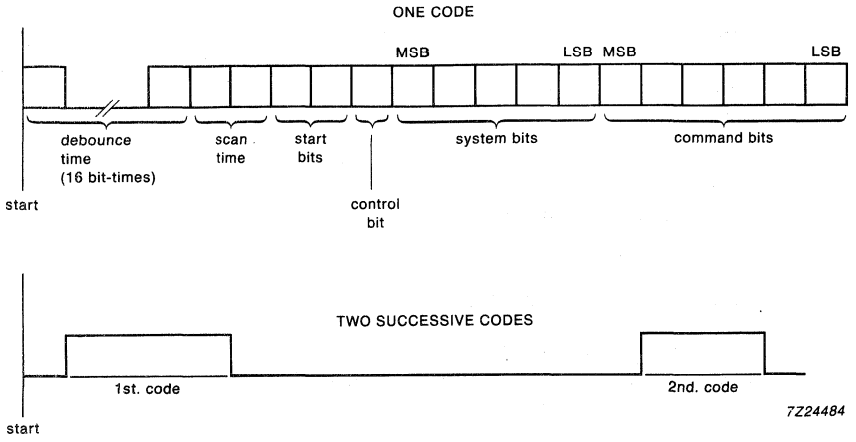
- Start part – 1.5 bits (2 x logic 1)
- Control part – 1 bit
- System part – 5 bits
- Command part – 6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50% duty factor.

In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).

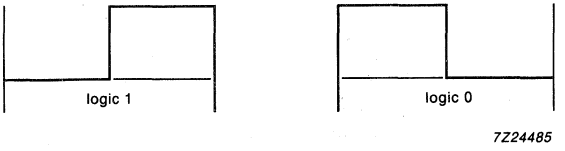
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

FUNCTIONAL DESCRIPTION (continued)



Where: debounce time + scan time = 18 bit-times
repetition time = 4 x 16 bit-times

Fig.4 Data output format.



Where: 1 bit-time = 3.2^8 x T_{OSC} = 1.778 ms (typ.)

Fig.5 Biphase transmission technique.

Table 1 Command matrix (X-DR)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
0	●	●	0 0 0 0 0 0
1	●	●	0 0 0 0 0 1
2	●	●	0 0 0 0 1 0
3	●	●	0 0 0 0 1 1
4	●	●	0 0 0 1 0 0
5	●	●	0 0 0 1 0 1
6	●	●	0 0 0 1 1 0
7	●	●	0 0 0 1 1 1
8	●	●	0 0 1 0 0 0
9	●	●	0 0 1 0 0 1
10	●	●	0 0 1 0 1 0
11	●	●	0 0 1 0 1 1
12	●	●	0 0 1 1 0 0
13	●	●	0 0 1 1 0 1
14	●	●	0 0 1 1 1 0
15	●	●	0 0 1 1 1 1
16	●	●	0 1 0 0 0 0
17	●	●	0 1 0 0 0 1
18	●	●	0 1 0 0 1 0
19	●	●	0 1 0 0 1 1
20	●	●	0 1 0 1 0 0
21	●	●	0 1 0 1 0 1
22	●	●	0 1 0 1 1 0
23	●	●	0 1 0 1 1 1
24	●	●	0 1 1 0 0 0
25	●	●	0 1 1 0 0 1
26	●	●	0 1 1 0 1 0
27	●	●	0 1 1 0 1 1
28	●	●	0 1 1 1 0 0
29	●	●	0 1 1 1 0 1
30	●	●	0 1 1 1 1 0
31	●	●	0 1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Table 1 Command matrix (X-DR) (continued)

code no.	X-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	command bits 5 4 3 2 1 0
32	●	●	1 0 0 0 0 0
33	●	●	1 0 0 0 0 1
34	●	●	1 0 0 0 1 0
35	●	●	1 0 0 0 1 1
36	●	●	1 0 0 1 0 0
37	●	●	1 0 0 1 0 1
38	●	●	1 0 0 1 1 0
39	●	●	1 0 0 1 1 1
40	●	●	1 0 1 0 0 0
41	●	●	1 0 1 0 0 1
42	●	●	1 0 1 0 1 0
43	●	●	1 0 1 0 1 1
44	●	●	1 0 1 1 0 0
45	●	●	1 0 1 1 0 1
46	●	●	1 0 1 1 1 0
47	●	●	1 0 1 1 1 1
48	●	●	1 1 0 0 0 0
49	●	●	1 1 0 0 0 1
50	●	●	1 1 0 0 1 0
51	●	●	1 1 0 0 1 1
52	●	●	1 1 0 1 0 0
53	●	●	1 1 0 1 0 1
54	●	●	1 1 0 1 1 0
55	●	●	1 1 0 1 1 1
56	●	●	1 1 1 0 0 0
57	●	●	1 1 1 0 0 1
58	●	●	1 1 1 0 1 0
59	●	●	1 1 1 0 1 1
60	●	●	1 1 1 1 0 0
61	●	●	1 1 1 1 0 1
62	●	●	1 1 1 1 1 0
63	●	●	1 1 1 1 1 1

Table 2 System matrix (Z-DR)

syst. no.	Z-lines 0 1 2 3 4 5 6 7	DR-lines 0 1 2 3 4 5 6 7	system bits 4 3 2 1 0
0	●	●	0 0 0 0 0
1	●	●	0 0 0 0 1
2	●	●	0 0 0 1 0
3	●	●	0 0 0 1 1
4	●	●	0 0 1 0 0
5	●	●	0 0 1 0 1
6	●	●	0 0 1 1 0
7	●	●	0 0 1 1 1
8	●	●	0 1 0 0 0
9	●	●	0 1 0 0 1
10	●	●	0 1 0 1 0
11	●	●	0 1 0 1 1
12	●	●	0 1 1 0 0
13	●	●	0 1 1 0 1
14	●	●	0 1 1 1 0
15	●	●	0 1 1 1 1
16	●	●	1 0 0 0 0
17	●	●	1 0 0 0 1
18	●	●	1 0 0 1 0
19	●	●	1 0 0 1 1
20	●	●	1 0 1 0 0
21	●	●	1 0 1 0 1
22	●	●	1 0 1 1 0
23	●	●	1 0 1 1 1
24	●	●	1 1 0 0 0
25	●	●	1 1 0 0 1
26	●	●	1 1 0 1 0
27	●	●	1 1 0 1 1
28	●	●	1 1 1 0 0
29	●	●	1 1 1 0 1
30	●	●	1 1 1 1 0
31	●	●	1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with "take over" of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

- debounce time
- between two codes.

When a key is released during matrix scanning, a reset will occur if:

- a key is released while one of the driver outputs is in the low ohmic state (logic 0)
- a key is released before that key has been detected
- there is no wired connection in the Z-DR matrix when SSM is HIGH.

Oscillator

The OSC is the input/output for a 1-pin oscillator. The oscillator is formed by a ceramic resonator, TOKO CRK429, order code, 2422 540 98069 or equivalent. A resistor of 6.8 kΩ must be placed in series with the resonator. The resistor and resonator are grounded at one side.

Test

Initialization of the circuit is performed when TP1, TP2 and OSC are HIGH. All internal nodes are defined except for the LATCH. The latch is defined when a scan cycle is started by pulling down an X- or Z-input while the oscillator is running.

If the debounce cycle has been completed, the scan cycle can be completed 3×2^3 faster, by setting TP1 HIGH.

If the scan cycle has been completed, the contents of the latch can be read 3×2^7 faster by setting TP2 HIGH.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	8.5	V
Input voltage range *	V_I	−0.5	V_{DD}+0.5	V
Output voltage range *	V_O	−0.5	V_{DD}+0.5	V
Input current	I_I	−	±10	mA
Output current	I_O	−	±10	mA
Maximum power dissipation				
OSC output	P_O	−	50	mW
other outputs	P_O	−	100	mW
Total power dissipation	P_{tot}	−	200	mW
Operating ambient temperature range	T_{amb}	−25	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

* V_{DD}+0.5 V must not exceed 9.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

T_{amb} = −25 °C to + 70 °C; V_{DD} = 2.0 to 7.0 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	7.0	V
Quiescent supply current	note 1 T_{amb} = 25 °C; I_O = 0 mA at all outputs. X0 to X7 and Z0 to Z3 at V_{DD} TP1, TP2, OSC at V_{SS} SSM at V_{SS} or V_{DD}	I_{DD}	–	–	10	μA
INPUTS						
Keyboard inputs X and Z with p-channel pull-up transistor						
Input current at each input	V_I = 0 V; TP1 = TP2 = SSM = LOW	$-I_I$	10	–	600	μA
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	note 2	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7 V; TP1 = TP2 = HIGH	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	1	μA
OSC						
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	2	μA
Input current	T_{amb} = 25 °C; V_I = V_{DD}	I_{OSC}	4.5	–	30	μA
SSM, TP1, TP2						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7.0 V	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V	$-I_{LI}$	–	–	1	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
DATA, MDATA						
Output voltage HIGH	$I_{OH} = -0.4$ mA	V_{OH}	$V_{DD}-0.3$	–	–	V
Output voltage LOW	$I_{OL} = 0.6$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA
	$V_O = 0$ V	$-I_{LO}$	–	–	20	μA
	$V_O = 0$ V; $T_{amb} = 25$ °C	$-I_{LO}$	–	–	2	μA
DR0 to DR7						
Output voltage LOW	$I_{OL} = 0.3$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA

Notes to the DC characteristics

1. Quiescent supply current measurement must be preceded by the initialization procedure described in the **TEST** section.
2. This DC test condition protects the AC performance of the output. The DC current requirements in the actual application are lower.

AC CHARACTERISTICS

T_{amb} = −25 to + 85 °C; V_{DD} = 2.0 to 7.0 V unless otherwise stated

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency	C_L = 160 pF; Figs 6 and 7					
operational		f_{OSC}	−	−	450	kHz
free-running		f_{OSC}	10	−	120	kHz

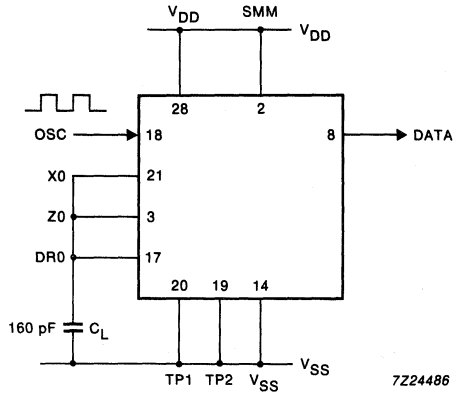


Fig.6 Test set-up for maximum f_{OSC} measurement.

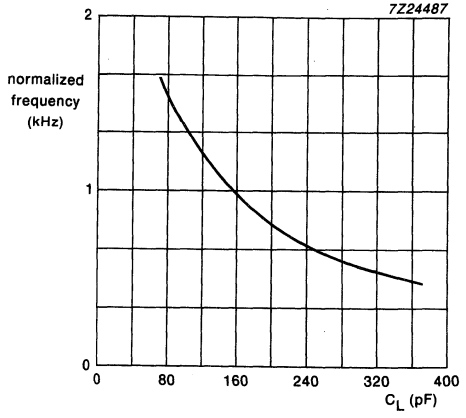


Fig.7 Typical normalized frequency as a function of keyboard load capacitance.

INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Very low current consumption
- For infrared transmission link
- Transmission by biphase technique
- Short transmission times; speed-up of system reaction time
- LC oscillator; no crystal required
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 12,6	V
Input voltage range	V_I	$-0,5$ to $(V_{DD}+0,5)$	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	$-0,5$ to $(V_{DD}+0,5)$	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	-25 to $+85$	°C

* V_{DD} + 0,5 V not to exceed 15 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

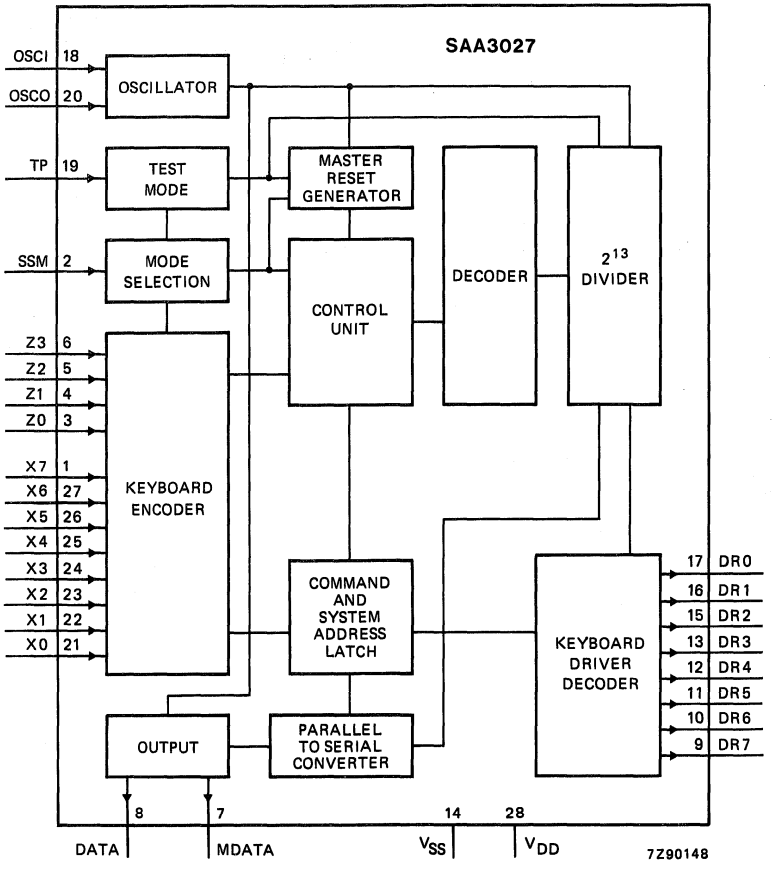


Fig. 1 Block diagram.

DEVELOPMENT DATA

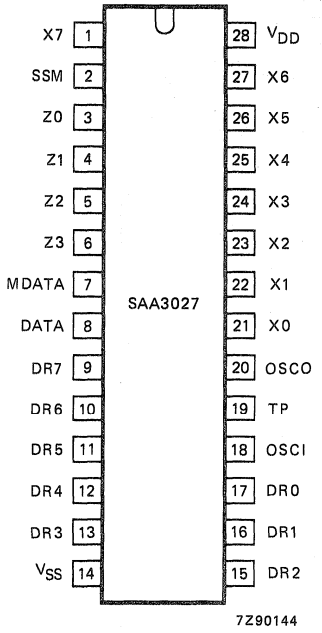
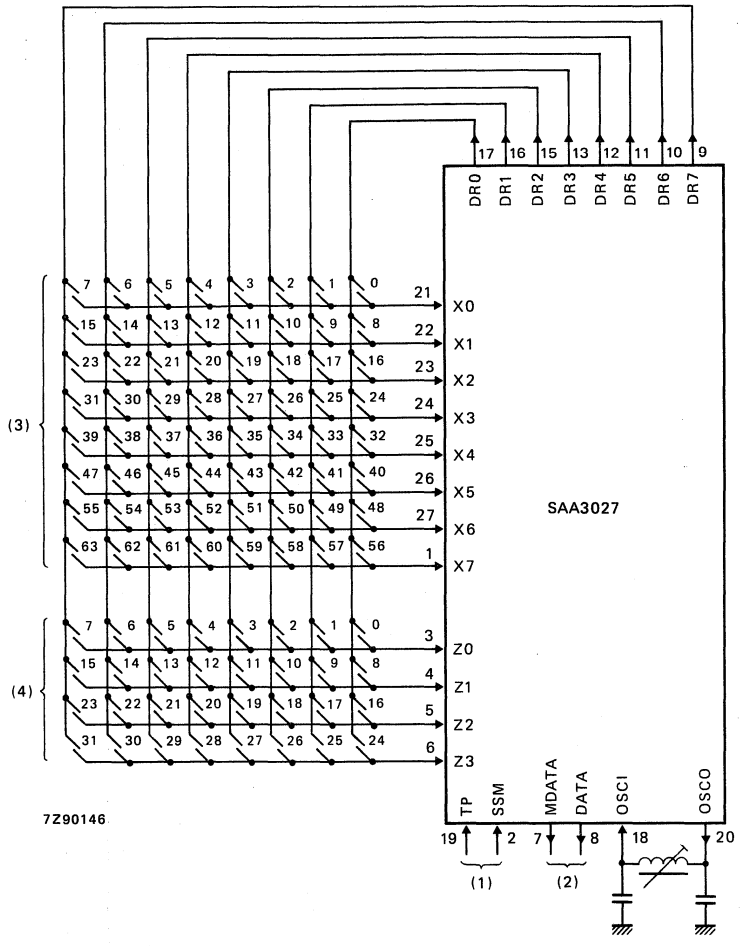


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
19	TP	test pin
18	OSC1	oscillator input
20	OSC0	oscillator output
17	DR0	scan driver outputs with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	



(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DECRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

DEVELOPMENT DATA

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output respectively of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72 kHz (typical).

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10 kΩ.

Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.

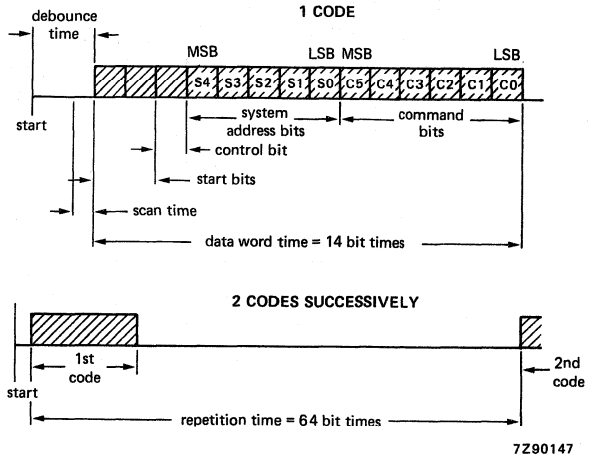


Fig. 4 DATA output format (RC-5).

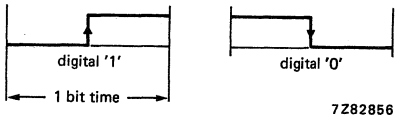


Fig. 5 Biphase transmission code; 1 bit time = $2^7 \times T_{OSC}$ = 1,778 ms (typical), where T_{OSC} is the oscillator period time.

Table 1 Command matrix X-DR

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

DEVELOPMENT DATA

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 2 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to +15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Power dissipation output OSCO	P_O	max. 50	mW
Power dissipation per output (all other outputs)	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to +85	°C
Storage temperature range	T_{stg}	−55 to +150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,75	–	12,6	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	12,6	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	4,75 to 12,6	$-I_I$	10	–	300	μA
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
SSM, TP and OSCI inputs						
Input voltage HIGH	4,75 to 12,6	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C;						
V_I = 12,6 V	12,6	I_{IR}	–	–	1	μA
V_I = 0 V	12,6	$-I_{IR}$	–	–	1	μA
Outputs						
DATA, MDATA outputs						
Output voltage HIGH at $-I_{OH}$ = 0,8 mA	4,75 to 12,6	V_{OH}	V_{DD} − 0,6	–	–	V
Output voltage LOW at I_{OL} = 0,8 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at:						
V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 12,6 V	12,6	I_{OR}	–	–	1	μA
V_O = 0 V	12,6	$-I_{OR}$	–	–	2	μA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
DR0 to DR7 outputs						
Output voltage LOW; at I_{OL} = 0,35 mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 12,6 V	12,6	I_{OR}	–	–	10	μA
at V_O = 12,6 V; T_{amb} = 25 °C	12,6	I_{OR}	–	–	1	μA
OSCO output						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA; OSCI = V_{SS}	4,75 to 12,6	V_{OH}	$V_{DD}-0,6$	–	–	V
Output voltage LOW at $-I_{OL}$ = 0,45 mA; OSCI = V_{DD}	4,75 to 12,6	V_{OL}	–	–	0,5	V
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	4,75	f_{OSCI}	75	72	–	kHz
	6	f_{OSCI}	120	72	–	kHz
	12,6	f_{OSCI}	300	72	–	kHz

DEVELOPMENT DATA

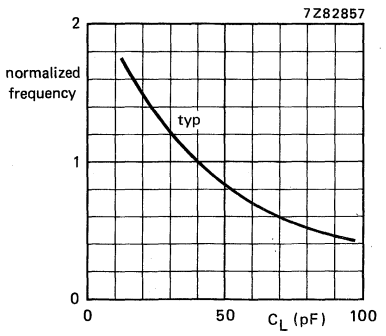


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

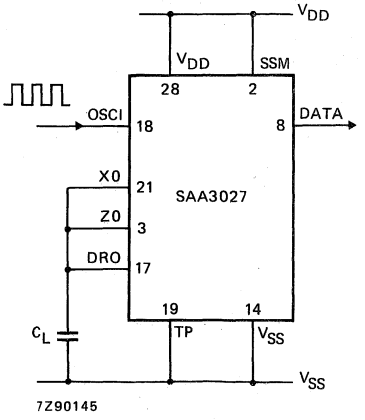


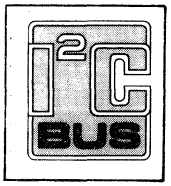
Fig. 7 Test circuit for measurement of maximum oscillator frequency.

Philips Components

Data sheet	
status	Product specification
date of issue	September 1990

SAA3028

Infrared remote control transcoder (RC-5)



FEATURES

- Converts RC-5 biphase coded signals into binary equivalents
- Two data inputs
- Rejects all codes not in RC-5 format
- I²C output interface capability
- Power-off facility
- Power-on-reset for defined start-up

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available for RC-5 coded signals. The input used is that at which an active code is first detected. Coded signals not in RC-5 format are rejected. Data input and output is by serial transfer, the output interface being compatible for I²C-bus operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		4.5	5.5	V
I_{DD}	supply current (quiescent)	V_{DD} = 5.5 V; T_{amb} = 25 °C	-	200	µA
T_{amb}	operating temperature range		−25	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3028P	16	16	plastic	SOT38D
SAA3028T	16	16	mini-pack	SO16L; SOT162A

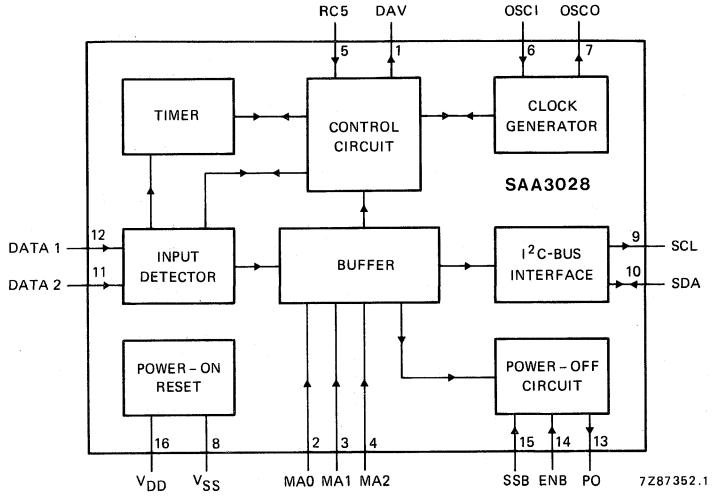


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DAV	1	data valid output with open drain n-channel transistor
MA0	2	master address input 0
MA1	3	master address input 1
MA2	4	master address input 2
RC5	5	data 2 input select
OSCI	6	oscillator input
OSCO	7	oscillator output
V_{SS}	8	negative supply (ground)
SCL	9	I²C bus serial clock line
SDA	10	I²C bus serial data line
DATA 2	11	data 2 input
DATA 1	12	data 1 input
PO	13	power-off signal output with open drain n-channel transistor
ENB	14	enable input
SSB	15	set standby input
V_{DD}	16	positive supply (+5 V)

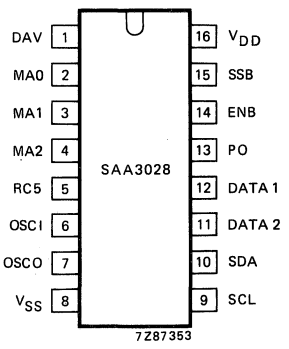


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1 Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2 This input performs according to the logic state of the select input RC-5. Only when RC-5 = HIGH, DATA 2 input will accept the RC-5 coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected. Note that in a steady state DATA 1 and DATA 2 are LOW.

Formats of RC-5 biphase coded signals are shown in Fig.3; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig.4.

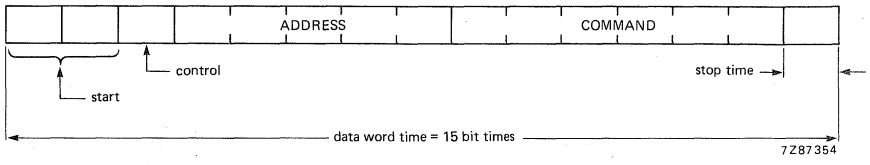


Fig.3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1.5 bit-times (nominal).

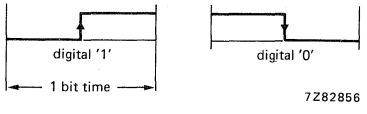


Fig.4 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1.778 ms (typical).

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I²C interface. The information now held in the buffer is shown in Table 1

Table 1 RC-5 buffer contents

CONTENTS	NUMBER OF BITS
data valid indicator	1
format indicator	1
input indicator	1
control	1
address data	5
command data	6

The information assembled in the buffer is subjected to the following controls before being made available at the I²C interface:

ENB = HIGH Enables the set standby input SSB.

SSB = LOW Causes power-off output PO to go HIGH.

PO = HIGH This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW This occurs according to the type of code being processed, as follows:
RC-5. When the binary equivalent value is transferred to the buffer.
At power-on, PO is reset to LOW.

DAV = LOW This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, the new binary values are discarded.

Output function

The data assembled in the buffer in the format shown in Fig.5 for RC-5 binary equivalent values. The data is output serially, starting from the left of the formats.

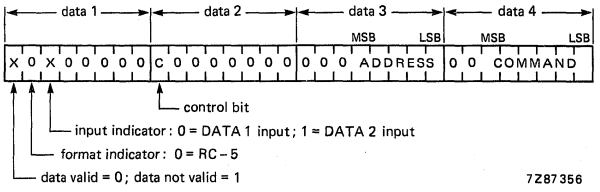


Fig.5 RC-5 binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I²C interface allows transmission on a bidirectional, two-wire I²C-bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110.

Serial output of the slave address to the I²C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig.6. The typical frequency of oscillation is 455 kHz.

(1) Catalogue number of ceramic resonator: 2422 540 98008.

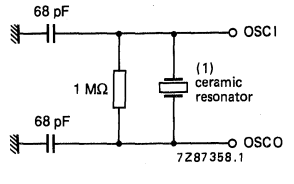


Fig.6 Oscillator circuit.

I²C-bus transmission

Formats for I²C transmission in low- and high-speed modes shown respectively in Figs.7 and 8.

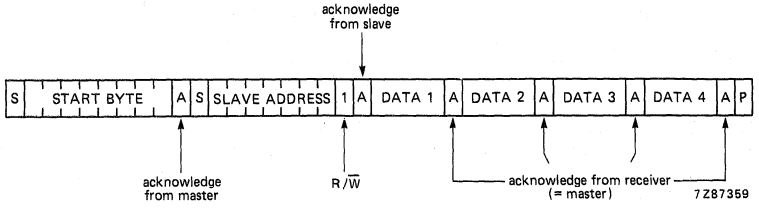


Fig.7 Format for transmission in I²C low-speed mode.

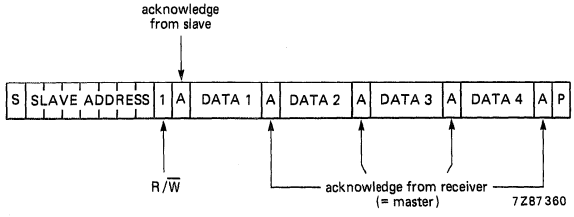


Fig.8 Format for transmission in I²C high-speed mode.

Note to figures 7 and 8

When R/$\overline{W}$ bit = 0; the slave generates an $\overline{ACK}$ (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.
When the receiver generates an $\overline{ACK}$; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).
When all data has been transmitted, the data line remains HIGH and the slave waits for P.

LIMITING VALUES

Limiting values in accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply range with respect to V_{SS}	−0.5	+15	V
V_I	input voltage range	−0.5	V_{DD}+0.5*	V
$\pm I_I$	input current	-	10	mA
V_O	output voltage range	−0.5	V_{DD}+0.5*	V
$\pm I_O$	output current	-	10	mA
P_O	power dissipation output OSCO	-	50	mW
P_O	power dissipation per output (all other outputs)	-	100	mW
P_{tot}	total power dissipation per package	-	200	mW
T_{amb}	operating ambient temperature range	−25	+85	°C
T_{stg}	storage temperature range	−55	+150	°C

HANDLING

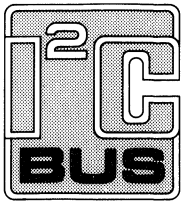
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C; at V_{DD} = 4.5 to 5.5 V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	-	5.5	V
I_{DD}	supply current; quiescent	T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	200	µA
Inputs						
MA0,MA1,MA2, DATA 1,DATA 2, RC5,SCL,ENB,SSB,OSCI						
V_{IH}	input voltage HIGH		0.7V_{DD}	-	V_{DD}	V
V_{IL}	input voltage LOW		0	-	0.3V_{DD}	V
I_{LI}	input leakage current	V_I = 5.5 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	1	µA
I_{LI}	input leakage current	V_I = 0 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	−1	µA
Outputs						
DAV,PO						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	-	-	0.4	V
I_{LO}	output leakage current	V_O = 5.5 V; T_{amb} = 25 °C; V_{DD} = 5.5 V	-	-	1	µA
OSCO						
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	V_{DD}−0.5	-	-	V
V_{OL}	output voltage LOW	I_{OL} = 0.3 mA	-	-	0.4	V
	output leakage current	T_{amb} = 25 °C		-		-
I_{LO}		V_O = 5.5 V; V_{DD} = 5.5 V		-		-
I_{LO}		V_O = 0 V; V_{DD} = 5.5 V				
SDO						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	-	-	0.4	V
I_{LO}	output leakage current	V_O = 5.5 V; T_{amb} = 25 °C; V_{DD} = 25 °C	-	-	1	µA
Oscillator						
f_{OSCI}	maximum oscillator frequency	V_{DD} = 4.75 V; see Fig.6	500	-	-	kHz

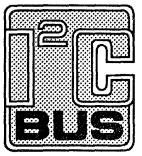


Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA4700
VPS dataline processor



FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I²C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 15 and 16)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700 is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I²C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700	18	DIL	plastic	SOT102

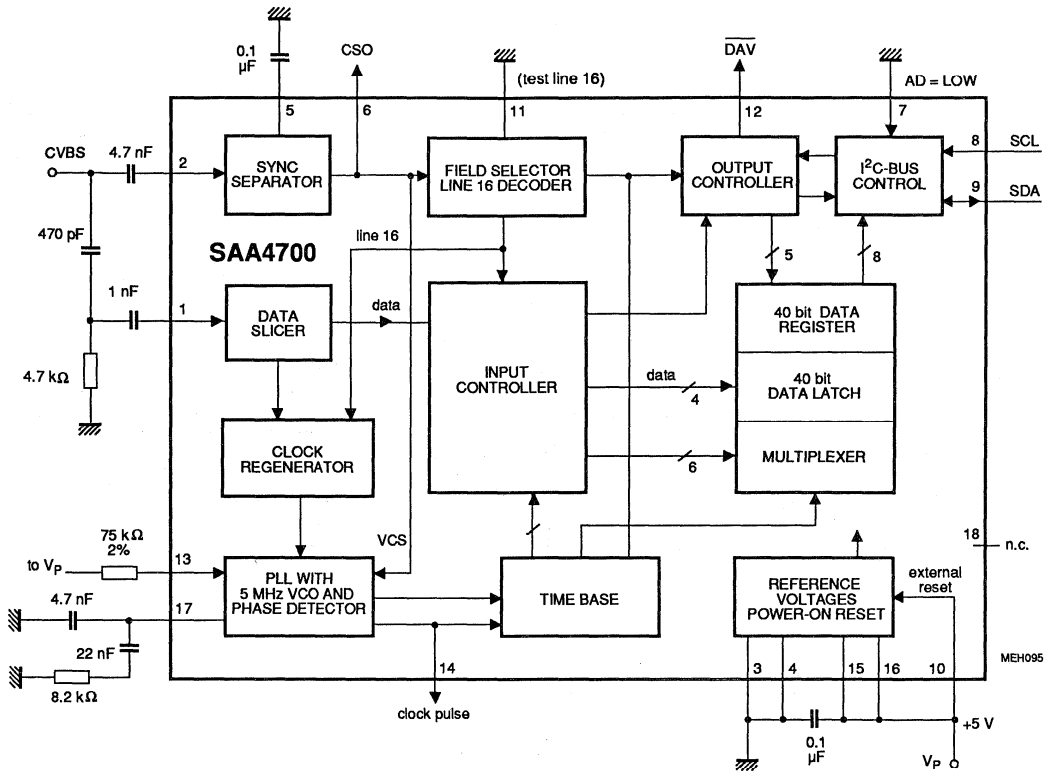


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700 extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
AD	7	address set input
SCL	8	I²C-bus clock line
SDA	9	I²C-bus data line
$\overline{RS}$	10	reset input active LOW
TP	11	test point for line 16 decoder
$\overline{DAV}$	12	data available output active LOW
R_{osc}	13	oscillator resistor for frequency adjustment
CP	14	test point clock pulse
V_{P1}	15	+5 V supply voltage (digital part)
V_{P2}	16	+5 V supply voltage (analog part)
C_{ph}	17	capacitor of phase detector
n.c.	18	not connected

PIN CONFIGURATION

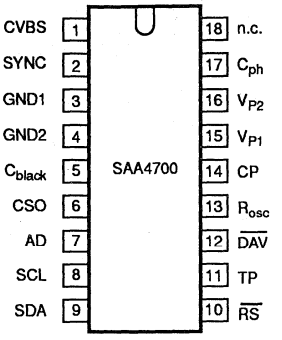


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 10 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 10 should be prepared by connecting pin 10 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 12)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 12 is set LOW after an error free dataline 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH. A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 13 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 17 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 15 and 16).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	) address assignment of signal distribution
9	)
10	messages/commands
11	)
12	) VTR control / information
13	)
14	)
15	reserve

Table 2 VTR control information of dataline 16

	VTR control information				
Word number	5	11	12	13	14
Bit number	1 8 XXXXXXXX	0 7 XXXXXXXX	8 15 XXXXXXXX	16 23 XXXXXXXX	24 31 XXXXXXXX

	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
Label binary	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
		Special system code					
System status code	1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					NC.. .NC	PC...PC
Pause code	1 X 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1					NC.. .NC	PC...PC
Interrupt code	1 X 0 0 0 0 0 1 1 1 1 1 1 0 1 1 1 1 1 1 1					NC.. .NC	PC...PC

Word 5:

Bit1	Bit2	Status
0	0	2-channel
0	1	Mono
1	0	Stereo
1	1	2-channel

Bit3	Bit4	Status
1	0	free
0	1	free

(1) address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

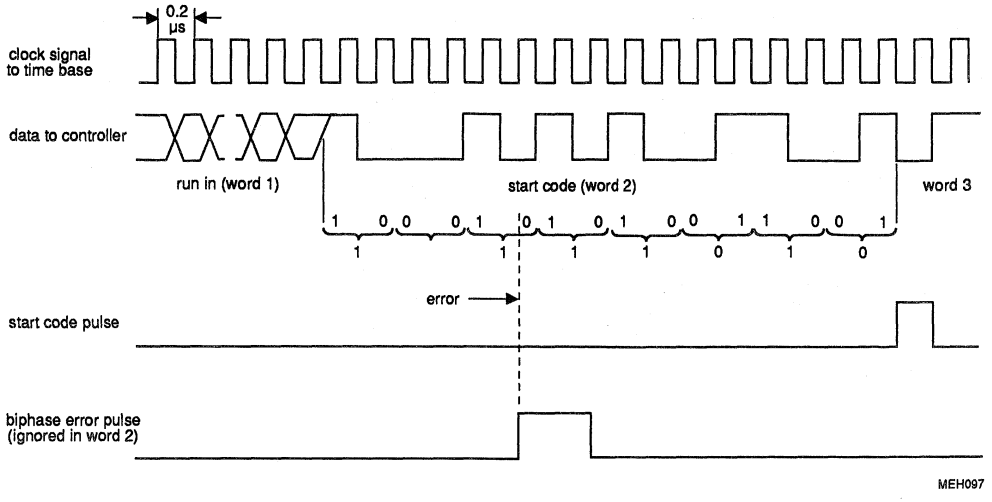


Fig.3 Timing diagram of start code detection.

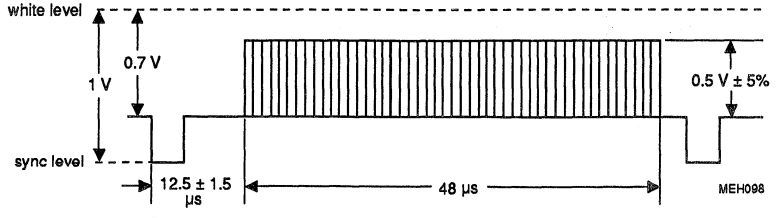


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

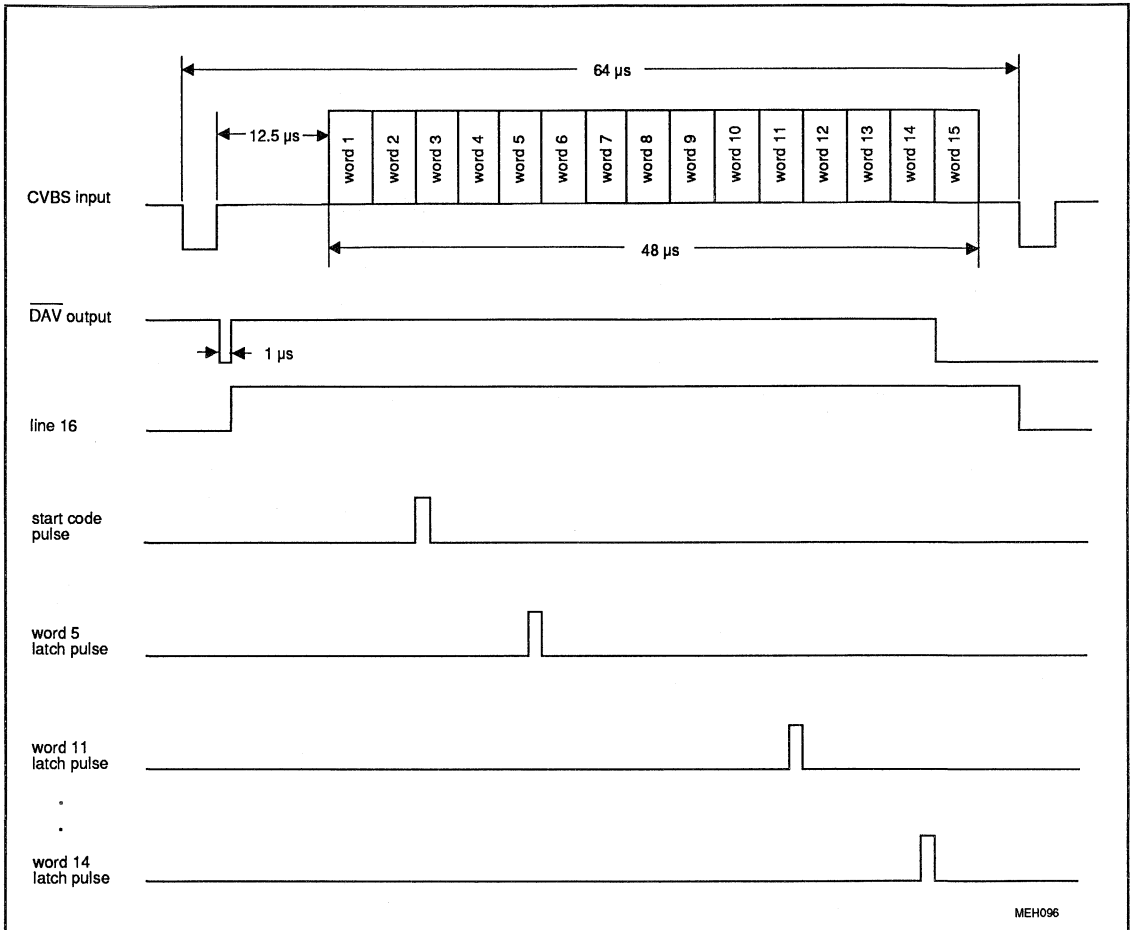


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 15 and 16 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 15)	–0.5	6.0	V
V_{P2}	supply voltage (pin 16)	–0.5	6.0	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	78	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 15 and 16)		4.5	5	5.5	V
I_P	total supply current	$I_{15} + I_{16}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	µA
I_{OH}	output current HIGH		-	-	–500	µA
t_d	sync separator delay time		-	0.3	-	µs
$\overline{\text{DAV}}$ **output** (pin 12)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	µA
I_{OH}	output current HIGH		-	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 8 and 9)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	μA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 9	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	μs
t_f	fall time		-	-	0.3	μs
$t_{p\,L}$	pulse duration LOW		4.7	-	-	μs
$t_{p\,H}$	pulse duration HIGH		4.0	-	-	μs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 7)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 10)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	μA
I_{IH}	input current HIGH		-	0.01	1	μA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

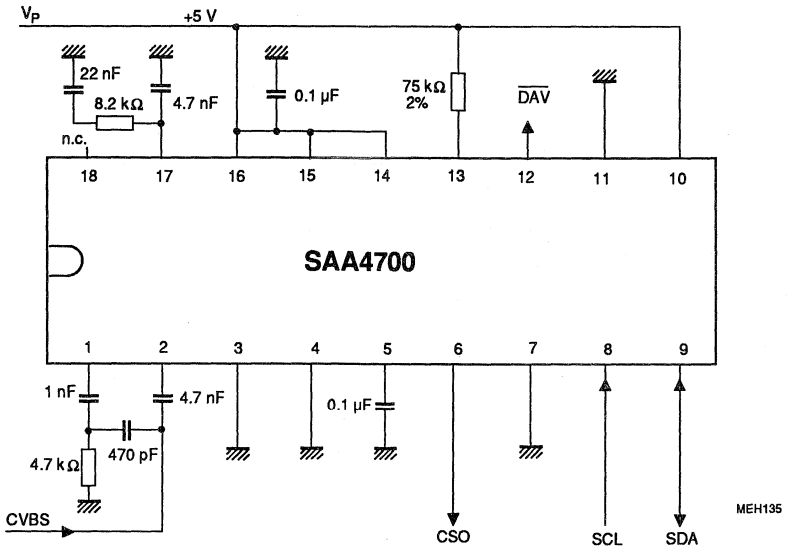


Fig.6 Application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 7 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA4700T
VPS dataline processor

FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I^2C-bus transmission

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 17 and 18)	4.5	5	5.5	V
I_P	total supply current	-	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	-	+70	°C

GENERAL DESCRIPTION

The SAA4700T is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I^2C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700T	20	mini-pack	plastic	SOT163A

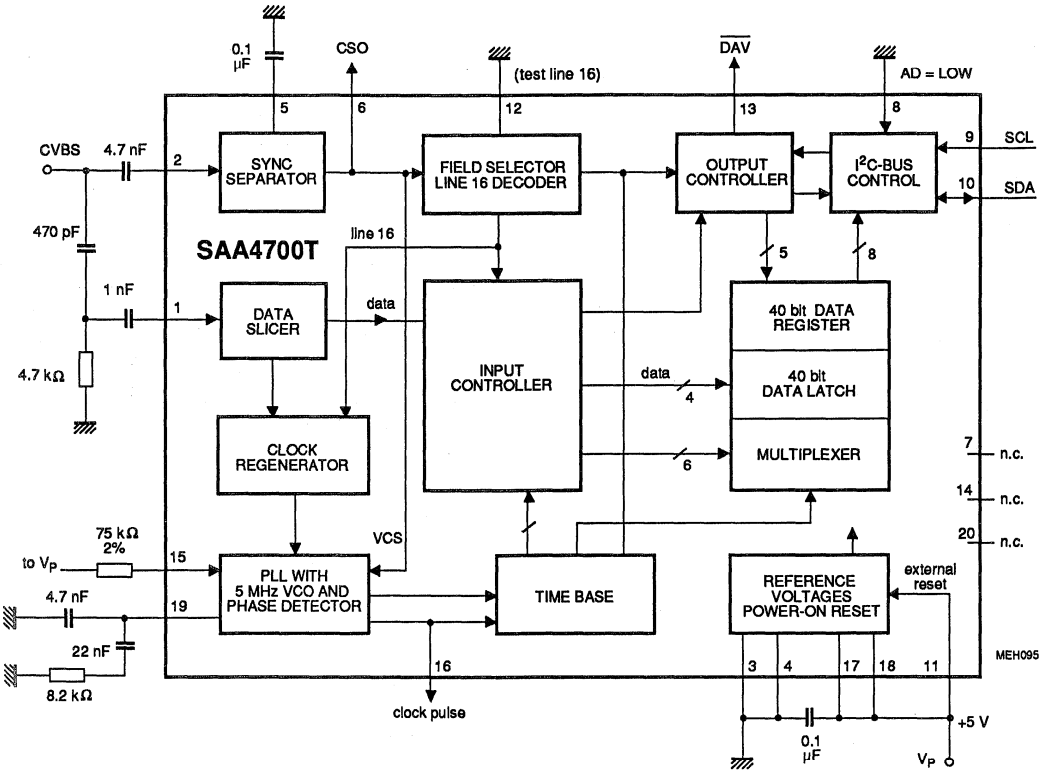


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700T extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occured, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is "FFF to F". The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
n.c.	7	not connected
AD	8	address set input
SCL	9	I²C-bus clock line
SDA	10	I²C-bus data line
$\overline{RS}$	11	reset input active LOW
TP	12	test point for line 16 decoder
$\overline{DAV}$	13	data available output active LOW
n.c.	14	not connected
R_{osc}	15	oscillator resistor for frequency adjustment
CP	16	test point clock pulse
V_{P1}	17	+5 V supply voltage (digital part)
V_{P2}	18	+5 V supply voltage (analog part)
C_{ph}	19	capacitor of phase detector
n.c.	20	not connected

PIN CONFIGURATION

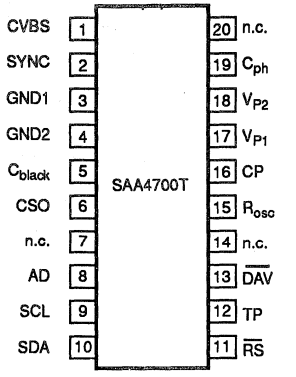


Fig.2 Pin configuration.

External reset
The circuit provides an internal power-on reset. When using this facility pin 11 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 11 should be prepared by connecting pin 11 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I²C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 13)
- I²C-bus transfer register to "FFF"

CVBS input
The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin1) via an RC high-pass filter. To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level
The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)
A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output
The data available output pin 13 is set LOW after an error free data line 16 is received. $\overline{DAV}$ returnes to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH.
A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector
The resistor connected between pin 15 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 19 acts as a low-pass filter for the phase detector.

Power supply
To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 17 and 18).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	)
9	) address assignment of signal distribution
10	messages/commands
11	)
12	)
13	) VTR control / information
14	)
15	reserve

Table 2 VTR control information of dataline 16

	VTR control information				
Word number	5	11	12	13	14
Bit number	1 8 X X X X X X X X	0 7 X X X X X X X X	8 15 X X X X X X X X	16 23 X X X X X X X X	24 31 X X X X X X X X

	AD (1)	Day	Month	Hour	Minute	Nation	Progr. source
Label binary							
		Special system code					
System status code	1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1					NC.. .NC	PC...PC
Pause code	1 X 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1					NC.. .NC	PC...PC
Interrupt code	1 X 0 0 0 0 0 1 1 1 1 1 1 0 1 1 1 1 1 1 1					NC.. .NC	PC...PC

Word 5:

Bit1	Bit2	Status
0	0	2-channel
0	1	Mono
1	0	Stereo
1	1	2-channel

Bit3	Bit4	Status
1	0	free
0	1	free

(1) address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

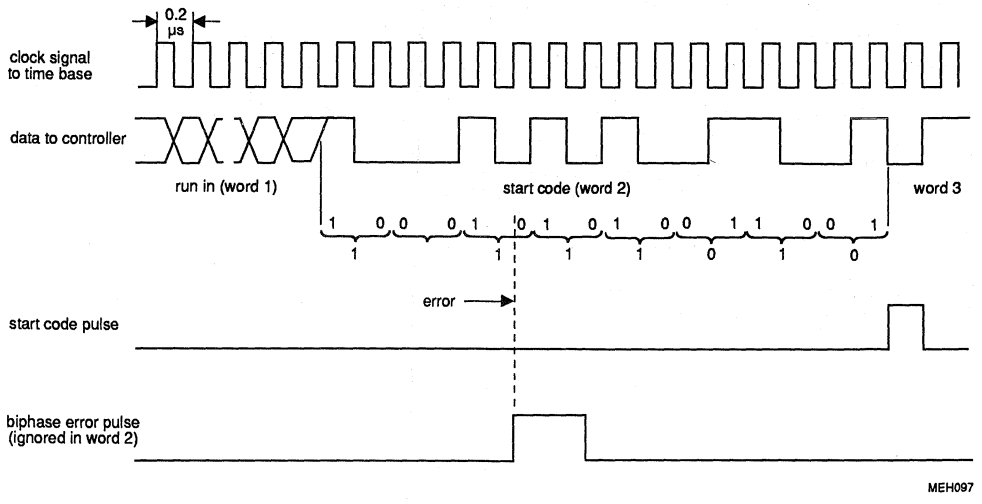


Fig.3 Timing diagram of start code detection.

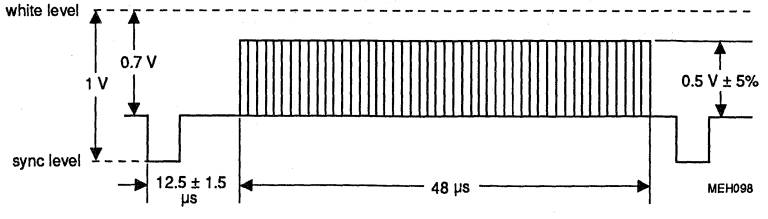


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

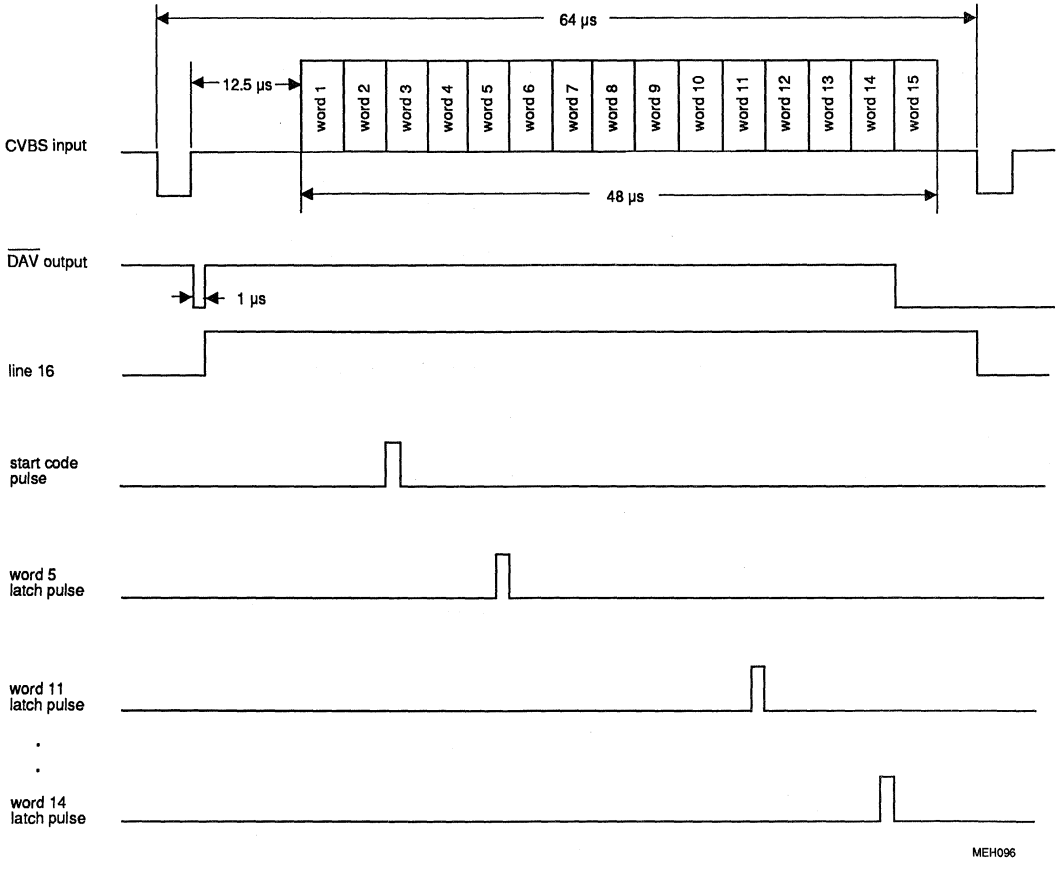


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 17 and 18 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 17)	−0.5	6.0	V
V_{P2}	supply voltage (pin 18)	−0.5	6.0	V
T_{stg}	storage temperature range	−20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	130	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 17 and 18)		4.5	5	5.5	V
I_P	total supply current	$I_{17} + I_{18}$	-	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	-	600	mV
R_S	source resistance		-	-	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	200	µA
I_{OH}	output current HIGH		-	-	−500	µA
t_d	sync separator delay time		-	0.3	-	µs
$\overline{\text{DAV}}$ **output** (pin 13)		note 2				
V_{OL}	output voltage LOW		-	-	0.4	V
V_{OH}	output voltage HIGH		2.4	-	-	V
I_{OL}	output current LOW		-	-	500	µA
I_{OH}	output current HIGH		-	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 9 and 10)						
V_{IL}	input voltage LOW		-	-	1.5	V
V_{IH}	input voltage HIGH		3	-	-	V
I_I	input current	$0.9V_P$	-	-	±10	µA
C_I	input capacitance		-	-	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 10	I_{OL} = 3 mA	-	-	0.4	V
t_r	rise time		-	-	1	µs
t_f	fall time		-	-	0.3	µs
$t_{p\,L}$	pulse duration LOW		4.7	-	-	µs
$t_{p\,H}$	pulse duration HIGH		4.0	-	-	µs
SCL	clock frequency		-	-	100	kHz
AD set input (pin 8)		note 2				
V_{IL}	input voltage LOW	address 23H	0	-	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	-	V_P	V
RESET input (pin 11)		note 2				
V_{IL}	input voltage LOW	reset active	-	-	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	-	-	V
I_{IL}	input current LOW		-	-	−10	µA
I_{IH}	input current HIGH		-	0.01	1	µA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

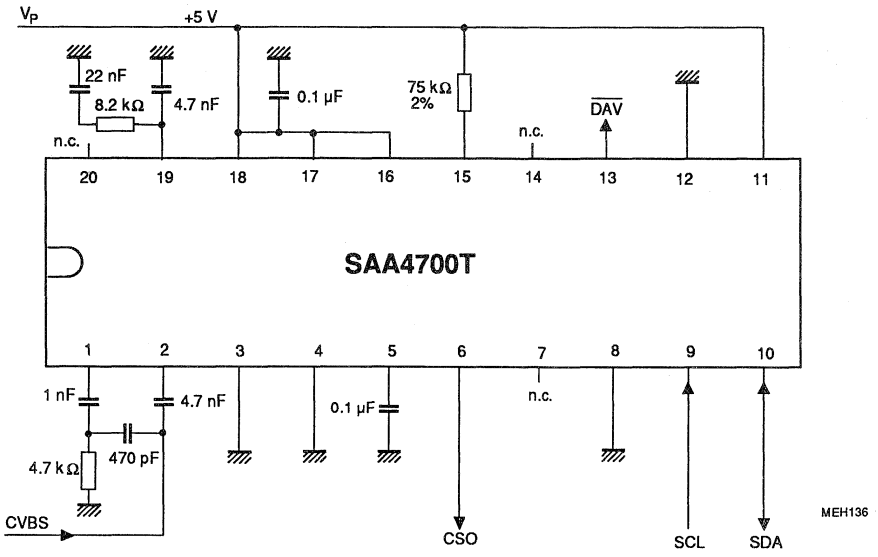


Fig.6 Application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**0010 0001 or 0010 0011** for set input AD = HIGH respectively LOW on pin 8 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectivily non-acknowledge by the microcontroller

Remarks to I²C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be "FF" continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	March 1991

SAA5191
Teletext video processor

FEATURES

- Adaptive data slicer
- Crystal-controlled data clock regeneration with a bit rate of 6.9375 MHz
- Adaptive sync separator, horizontal phase detector and 13.5 MHz VCO to provide display phase locked loop (PLL)
- TV synchronization at teletext mode

GENERAL DESCRIPTION

The SAA5191 is a bipolar integrated circuit that extracts teletext data from the video signal (CVBS), regenerates the teletext clock (TTC) and synchronizes the text display to the television signals (VCS). This device operates in conjunction with the Digital Video Teletext (back-end) Decoder (DVTB – SAA9042A) or any other compatible device.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 16)	-	12	-	V
I_P	supply current	-	70	-	mA
$V_{i\ CVBS}$	CVBS input signal on pin 27 (peak-to-peak value)				
	at pin 2 LOW	-	1	-	V
	at pin 2 open-circuit	-	2.5	-	V
V_o	output signals TTC and TTD (peak-to-peak value, pins 14, 15)	2.5	3.5	4.5	V
V_{F13}	13.5 MHz clock output signal (peak-to-peak value, pin 17)	1	2	3	V
V_{SYNC}	video sync output signal (peak-to-peak value, pin 1)	-	-	1	V
	SYNC output signal $\overline{TCS}$	200	450	650	mV
VCS	video composite sync level on output pin 25				
	LOW	-	-	0.4	V
	HIGH	2.4	-	5.5	V
T_{amb}	operating ambient temperature	0	-	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5191	28	DIL	plastic	SOT117

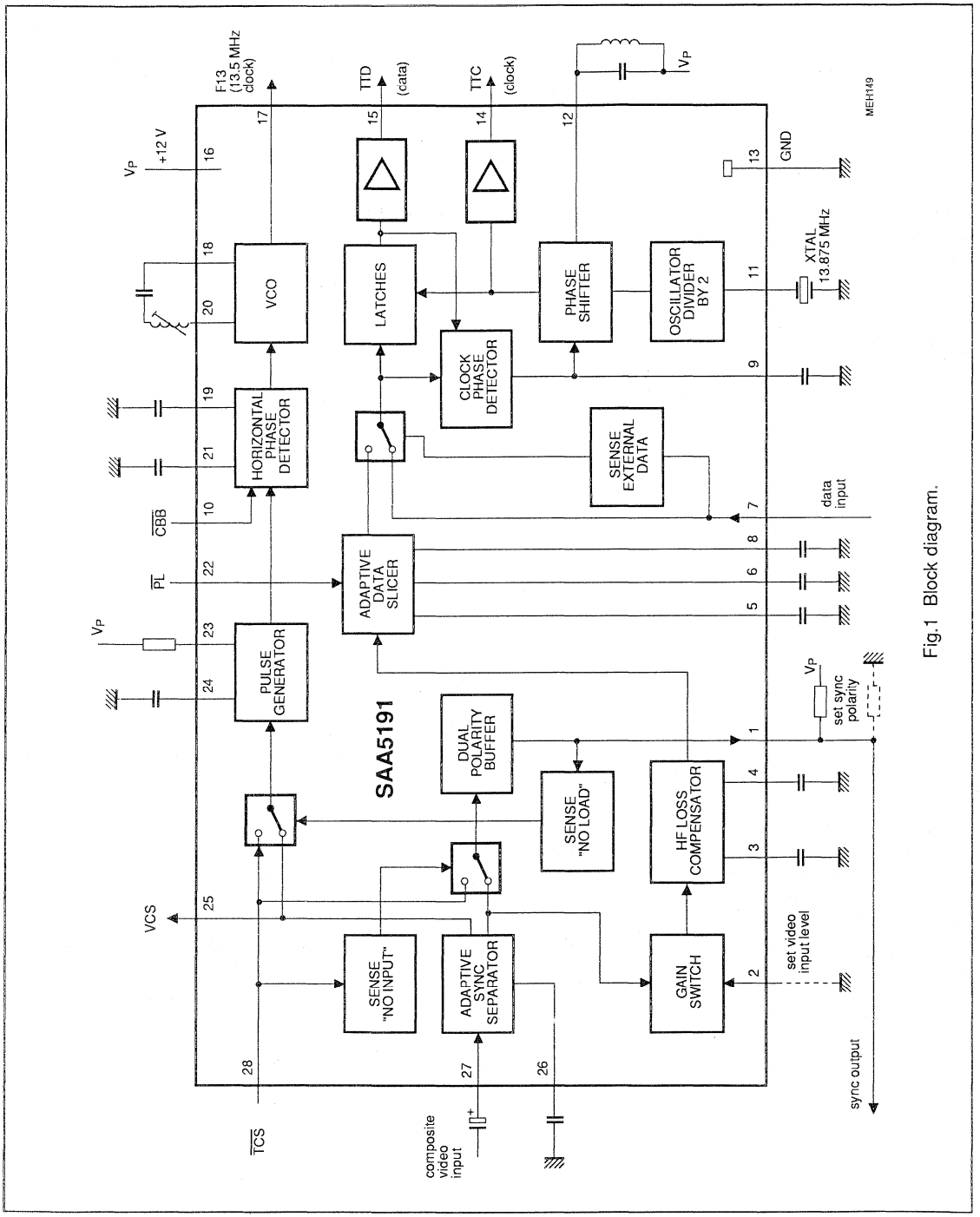


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STTV	1	sync output signal to TV (positive or negative going)
VILS	2	level select input of video input (LOW equals 1 V)
C_{filt}	3	video filtering capacitor of HF loss compensation
C_{store}	4	HF storage capacitor
C_{ampl}	5	amplitude capacitor
C_{zero}	6	zero level capacitor
EXD	7	external data current input (1)
C_{time}	8	data timing capacitor for the adaptive data slicer
C_{CLK}	9	clock phase detector capacitor
$\overline{CBB}$	10	blanking insertion input
XTAL	11	13.875 MHz crystal (double of data rate)
CLF	12	6.9375 MHz clock frequency filter
GND	13	ground (0 V)
TTC	14	teletext clock output (for computer controlled teletext)
TTD	15	teletext data output (for computer controlled teletext)
V_P	16	+12 V supply voltage
F13	17	13.5 MHz VCO output (for sandcastle generation)
OSCO	18	oscillator output to series LC-circuit or crystal
C_{VCR}	19	short time constant capacitor at video recorder mode (2)
OSCI	20	oscillator input from series LC-circuit or crystal
C_{hor}	21	horizontal phase capacitor / VCR mode
$\overline{PL}$	22	sandcastle input (generated in CCT)
R_T	23	timing resistor for pulse generator
C_T	24	timing capacitor for pulse generator
VCS	25	video composite sync output to CCT
C_{BL}	26	black level capacitor
CVBS	27	composite video input signal from TV
$\overline{TCS}$	28	text-composite/scan-composite sync input ($\overline{TSC}$/$\overline{SCS}$)

PIN CONFIGURATION

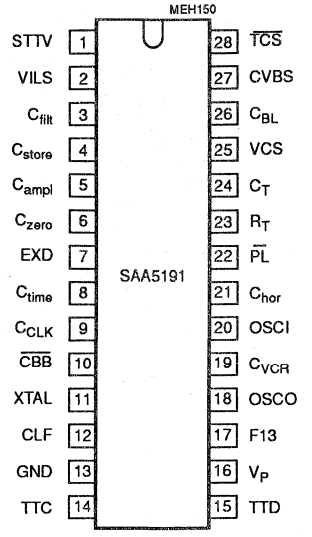


Fig.2 Pin configuration.

Notes to the pinning

(1) Sliced teletext data from external: active HIGH level (current), low impedance input.
(2) While the loop is locking up.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

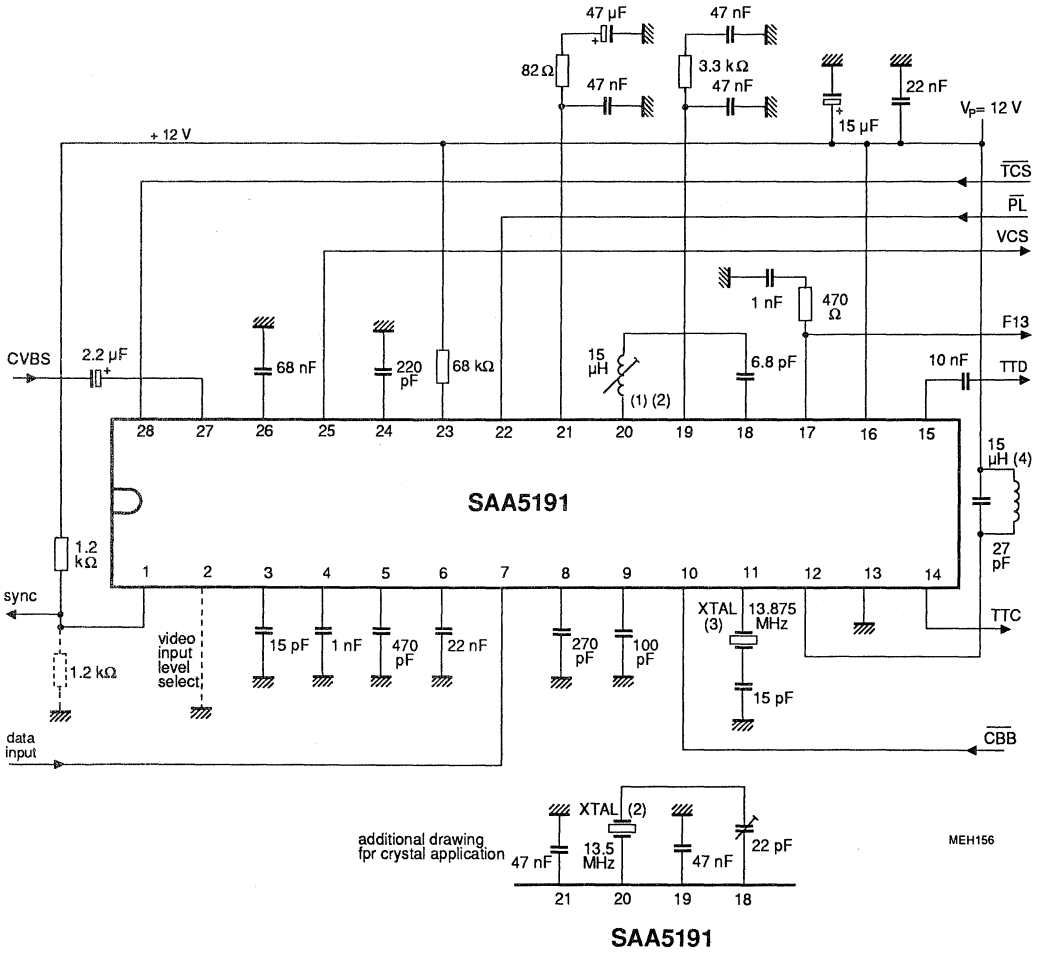
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 16)	0	13.2	V
V_5	voltage on pin 5	0	5.5	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C and measurements taken in Fig.3, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 16)		10.8	12.0	13.2	V
I_P	supply current		50	70	105	mA
Video input, sync separator and data slicer		$Z_S \leq 250\ \Omega$				
$V_{i\ CVBS}$	input signal sync to white (peak-to-peak value, pin 27)	V_2 = LOW	0.7	1	1.4	V
		V_2 = HIGH	1.75	2.5	3.5	V
	sync amplitude (peak-to-peak value)		0.1	-	1	V
	data slicing level	V_2 = LOW	0.3	0.46	0.7	V
		V_2 = HIGH	0.75	1.15	1.75	V
V_2	input voltage LOW (pin 2)		0	-	0.8	V
	input voltage HIGH	open-circuit equals HIGH	2.0	-	5.5	V
I_2	input current LOW		0	-	–150	µA
	input current HIGH	V_2 < 5.5 V	0	-	1	mA
Teletext data output (TTD)						
V_{22}	phase lock pulse (PL) input voltage (peak-to-peak value, pin 22)	phase locked	0	-	3	V
		phase unlocked	3.9	-	5.5	V
$V_{o\ TTD}$	data output signal on pin 15 (peak-to-peak value)		2.5	3.5	4.5	V
V_{15}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 15		-	-	40	pF
t_r, t_f	rise and fall time		20	30	45	ns
Teletext clock output (TTC)						
$V_{o\ TTC}$	clock output signal on pin 14 (peak-to-peak value)		2.5	3.5	4.5	V
V_{14}	DC output voltage	mean level	3	4	5	V
C_L	load capacitance on pin 14		-	-	40	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r, t_f	rise and fall time		20	30	45	ns
t_d	delay time of falling edge relative to other edges of TTD		-	-	±20	ns
Text/ scan composite sync input ($\overline{TCS}$/$\overline{SCS}$)						
V_{28}	input voltage LOW for $\overline{TCS}$ (pin 28)		0	-	0.8	V
	input voltage HIGH for $\overline{TSC}$		2.0	-	7.0	V
	input voltage LOW for $\overline{SCS}$		0	-	1.5	V
	input voltage HIGH for $\overline{SCS}$		3.5	-	7.0	V
I_{28}	input current	V_{28} = 0 to 7 V	–40	–70	–100	µA
		V_{28} = 10 to V_P	-	-	±5	µA
SYNC output buffer						
V_o	CVBS sync output signal on pin 1 (peak-to-peak value)	$R_{L\,1}$ = 1.2 kΩ to V_P	-	-	1	V
	$\overline{TCS}$ output signal	$R_{L\,1}$ = 1.2 kΩ to GND	200	450	650	mV
V_1	DC output voltage at positive sync signal	$R_{L\,1}$ = 1.2 kΩ to GND	1.0	1.4	2.0	V
	DC output voltage at negative sync signal	$R_{L\,1}$ = 1.2 kΩ to V_P	9.0	10.1	11.0	V
I_1	output current		-	-	±3	mA
Video composite sync output (VCS)						
V_{25}	output voltage LOW (pin 25)		0	-	0.4	V
	output voltage HIGH		2.4	-	5.5	V
I_{25}	output current LOW		0	-	0.5	mA
	output current HIGH		0	-	–1.5	mA
t_d	sync separator delay time		250	350	400	ns
Horizontal phase detector and 13.5 MHz VCO						
V_{10}	input voltage LOW ($\overline{CBB}$), pin 10	blanking inserted	0	-	0.5	V
	blanking insertion HIGH	no blanking	1.0	-	5.5	V
I_{10}	input current		-	-	–5	µA
V_o	13.5 MHz clock output signal (peak-to-peak value, pin 17)		1	2	3	V
V_{17}	DC output voltage	maximum swing	4	-	8.5	V
C_L	load capacitance on pin 17		-	-	40	pF
t_r, t_f	rise and fall time		10	-	30	ns



(1) inductance 15 µH at 1 kHz, C_o = 2.2 pF. Adjust free-running frequency to 13.5 ± 0.1 MHz or apply 13.5 MHz quarz crystal as shown in additional drawing

(2) Crystal: f = 13.5 MHz (e.g. Philips catalogue number 4322 143 04101); adjustment tolerance ±40 • 10^{-6}; load capacitance C_L = 22 pF; resonance resistance R_r = 22 pF; typical motional capacitance C_1 = 23 fF; static parallel capacitance C_o = 5.5 pF; frequency tolerance ±30• 10^{-6} in temperature range T = −20 to +70°. Adjust free-running frequency to 13.5 ± 0.5 MHz.

(3) Crystal: f = 13.875 MHz; adjustment tolerance ±40 • 10^{-6}; load capacitance C_L = 15 pF; typical resonance resistance R_r = 15 Ω (maximum 60 Ω); typical motional capacitance C_1 = 19 fF; static parallel capacitance C_o = 5 pF; frequency tolerance ±30• 10^{-6} in temperature range T = −20 to +70°.

(4) Coil: Fixed inductance 15 µH ±20%, quality factor Q > 20.

Fig.3 Test circuit and application circuit using LC-circuit or a crystal for VCO (clock F13).

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12 V
Supply current (pin 16)	I_{CC}	typ.	70 mA
Video input amplitude (pin 27) (peak-to-peak value)			
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1 V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

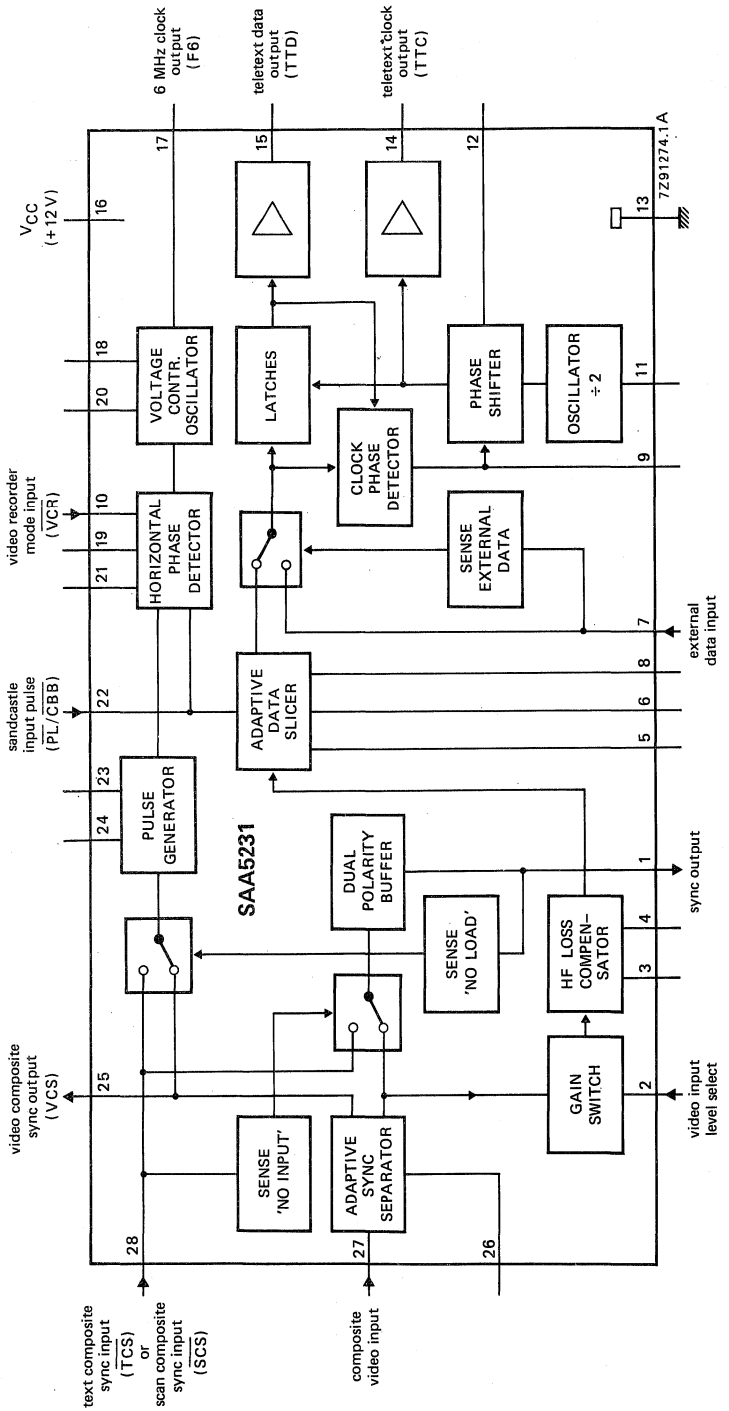


Fig. 1 Block diagram.

PINNING

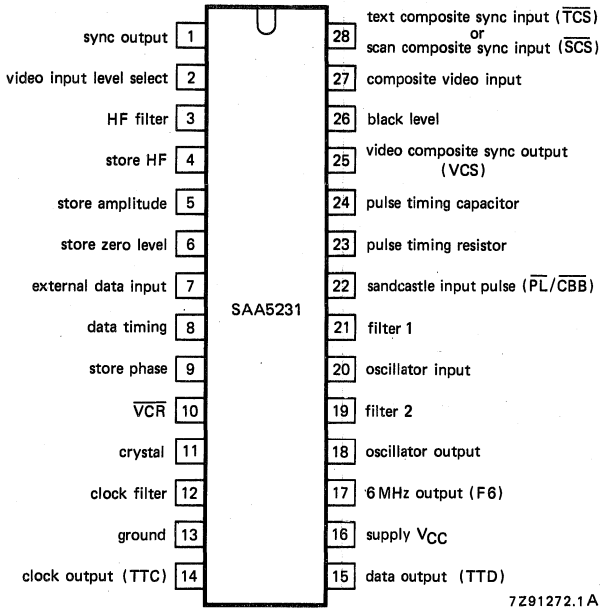


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max. 13,2 V
Storage temperature range	T_{stg}	−20 to + 125 °C
Operating ambient temperature	T_{amb}	0 to + 70 °C

CHARACTERISTICS

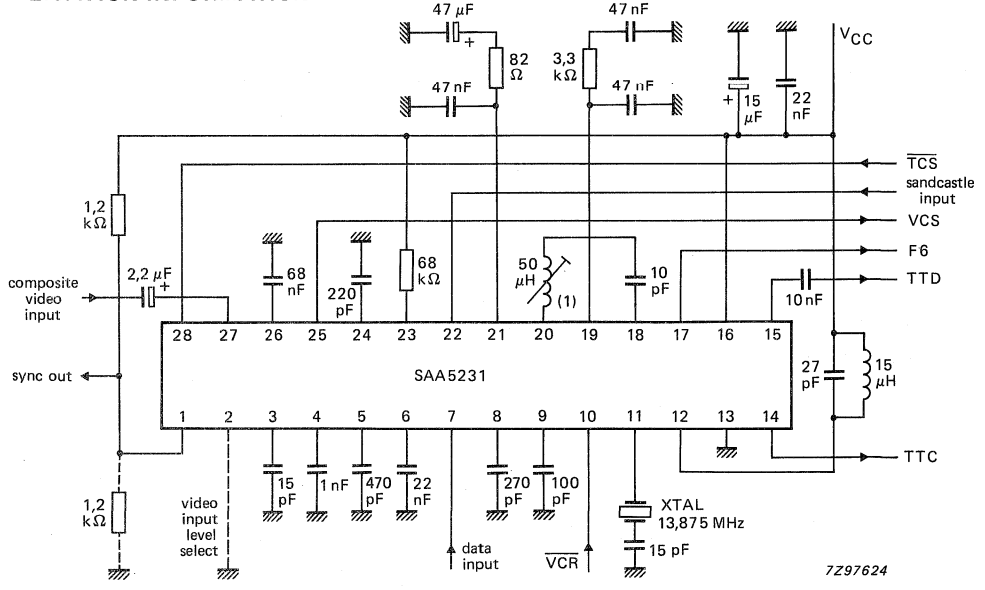
V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in application circuits unless otherwise stated.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	50	70	105	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_{28} = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_{28} = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	0,25	0,35	0,40	μs

parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	0,20	0,45	0,65	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	–3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	1,0	1,4	2,0	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	9,0	10,1	11,0	V
Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	2,0	2,4	2,8	μs
using scan composite sync	t_p	3,0	3,5	4,0	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	t_r; t_f	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+ 10	μA

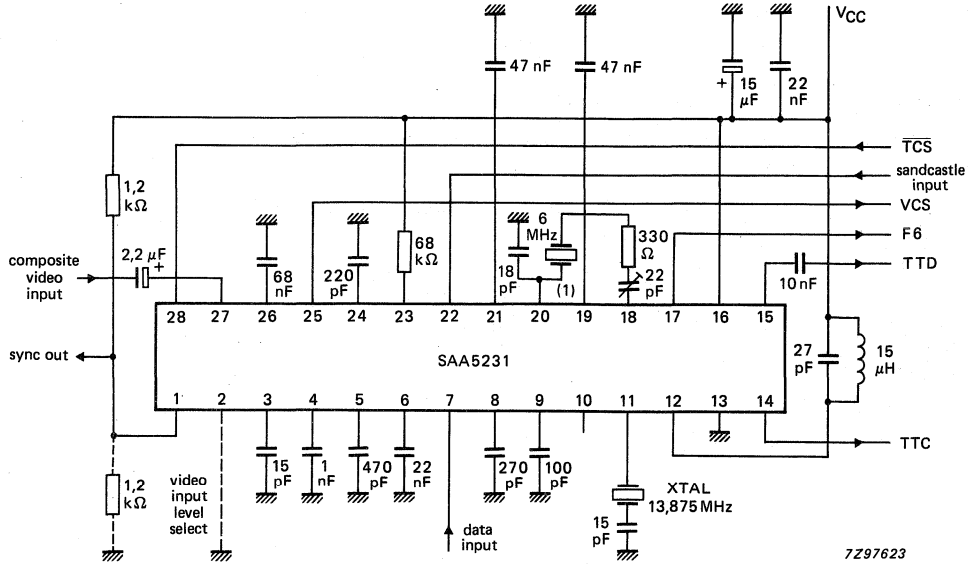
parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	V_{27-13}	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	V_{27-13}	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{14-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	–20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{15-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns

APPLICATION INFORMATION



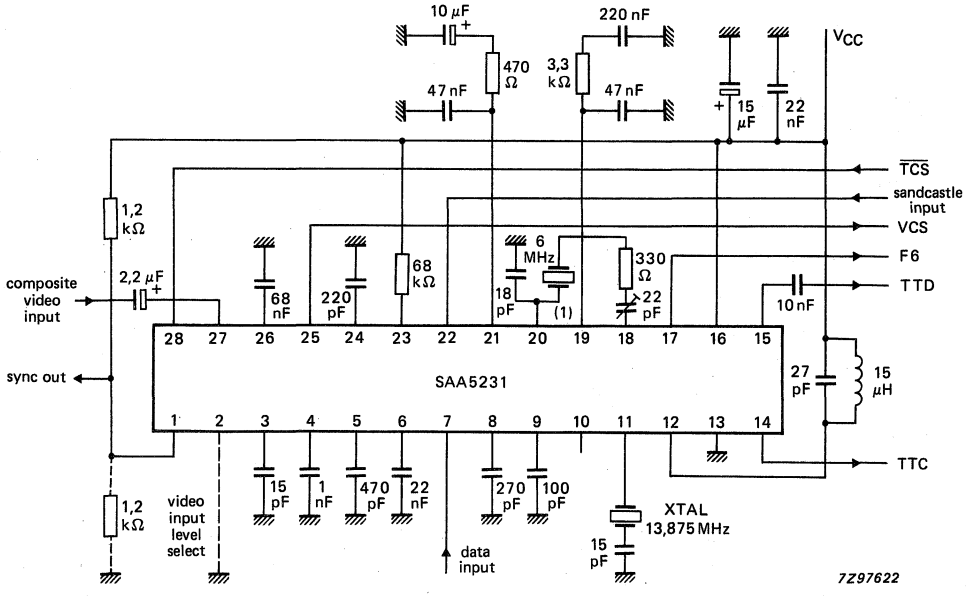
(1) Coil: 50 µH at 1 kHz, C_o = 4 pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig. 3a Application circuit using L/C circuit in PLL.



(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3c Application circuit using ceramic resonator in PLL.

Component specifications

Specifications of some external components in Figs 3a, 3b and 3c.

Quartz crystal 13,875 MHz; Figs 3a, 3b and 3c

Load resonance frequency (f) 13,875 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± $30 \cdot 10^{-6}$

Resonance resistance (R_r) typical 10 Ω maximum 60 Ω

Motional capacitance (C_1) typical 19 fF

Static parallel capacitance (C_o) typical 5 pF

Fixed inductance Figs 3a, 3b and 3c

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

Variable inductance Fig. 3a

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance (C_o) typical 4 pF

Quartz crystal Fig. 3b

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance ± $30 \cdot 10^{-6}$

Resonance resistance (R_r) 60 Ω

Motional capacitance (C_1) typical 28 fF

Static parallel capacitance (C_o) typical 7 pF

Ceramic resonator; Fig. 3c

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance (R_r) typical 6 Ω

Motional capacitance (C_1) typical 9 pF

Static parallel capacitance (C_o) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3b or Fig. 3c.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

See pin 18.

21. **Filter 1**

A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

The current for the pulse generator is defined by a 68 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

This output signal is for CCT.

26. **Black level**

The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

$\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

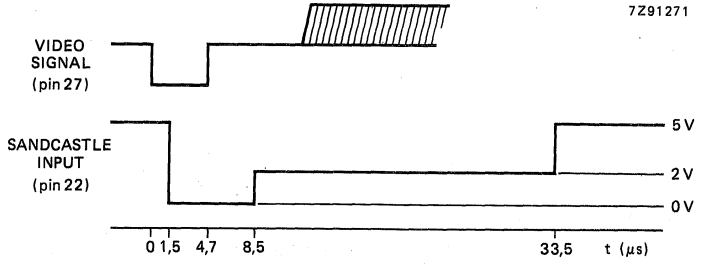


Fig. 4 Sandcastle waveform and timing.

DATALINE SLICER

The SAA5235 is a bipolar integrated circuit for dataline receivers. It extracts the dataline signal from the video signal and regenerates the dataline clock. It also provides signals for the dataline decoder.

Features

- Adaptive dataline slicer
- Dataline clock regenerator
- Buffered clock and data outputs
- Buffered composite sync output
- Gain switch for the video input signal

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 16)	V_{CC}	10,8	12	13,2	V
Supply current at V_{CC} = 12 V	I_{CC}	–	70	–	mA
Composite video amplitude					
pin 2 LOW	$V_{27(p\text{-}p)}$	–	1	–	V
pin 2 floating	$V_{27(p\text{-}p)}$	–	2,5	–	V
Storage temperature range	T_{stg}	–20	–	+ 125	°C
Operating ambient temperature	T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

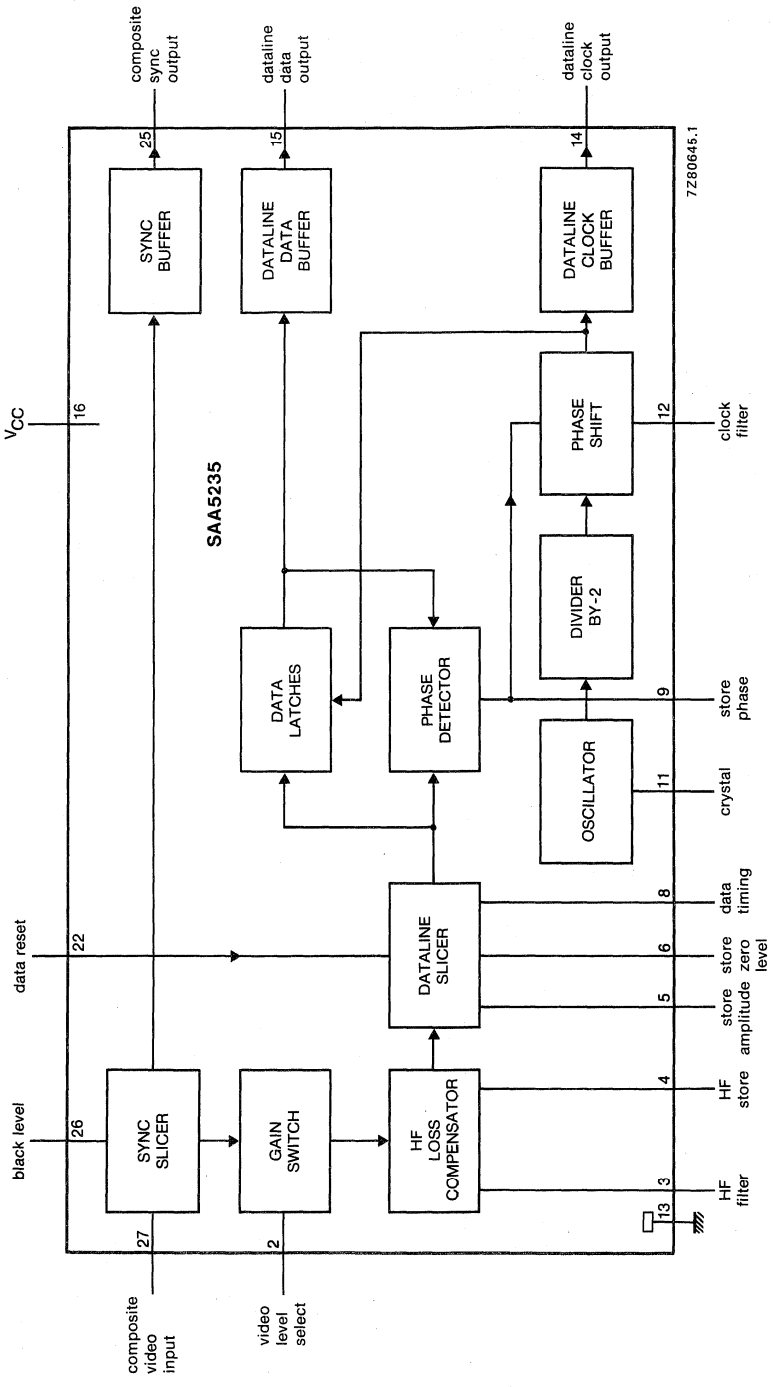


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	–	–	13,2	V
Storage temperature range	T_{stg}	–20	–	125	°C
Operating ambient temperature	T_{amb}	0	–	70	°C

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; with external components as shown in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Composite video input (CV)					
Level select input (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
Level select input (pin 2) HIGH	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video level select					
Input voltage					
LOW	$V_{2\text{-}13}$	0	–	0,8	V
HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current					
LOW	I_2	0	–	–150	μA
HIGH	I_2	0	–	1	mA
Video composite sync output (VCS)					
Output voltage					
LOW	$V_{25\text{-}13}$	0	–	0,4	V
HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
Sync separator delay time	t_d	–	0,35	–	μs
Data reset input (DAR)					
Input voltage					
LOW (DAR on)	$V_{22\text{-}13}$	0	–	0,5	V
HIGH (DAR off)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Dataline slicer					
Dataline amplitude (pin 27)					
Video select voltage (pin 2) LOW	$V_{27\text{-}13(p\text{-}p)}$	0,3	0,46	0,7	V
Video select (pin 2) FLOATING	$V_{27\text{-}13(p\text{-}p)}$	0,75	1,15	1,75	V
Dataline clock output (DLCL)					
A.C. output voltage	$V_{14\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{14\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns
Delay of falling edge relative to edges of DLD	t_d	–20	–	20	ns
Dataline data output (DLD)					
A.C. output voltage	$V_{15\text{-}13(p\text{-}p)}$	2,5	3,5	4,5	V
Output voltage (d.c.) centre	$V_{15\text{-}13}$	–	4,0	–	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r, t_f	20	30	45	ns

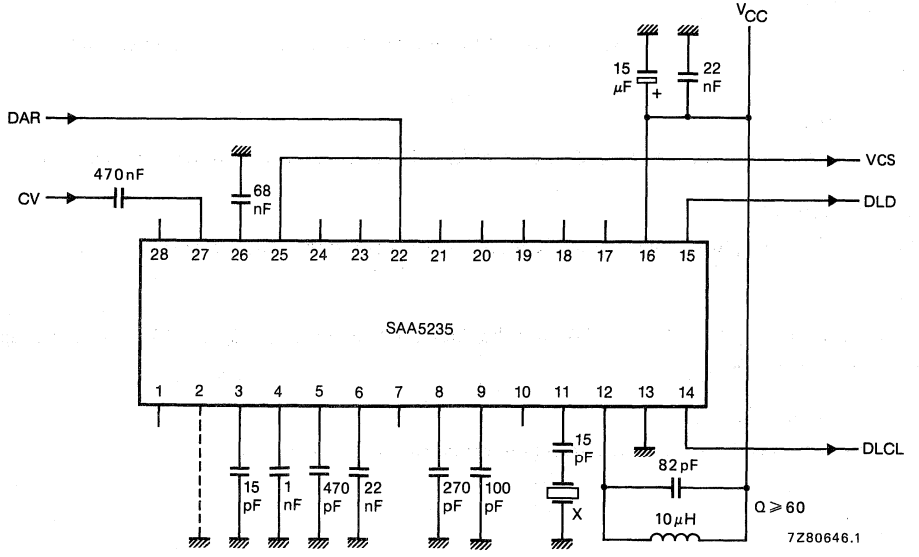


Fig. 2 Application circuit; crystal X; f = 10,000 MHz.

APPLICATION DATA

Composite video input CV (pin 27)

The composite video has to be fed into this input via a clamp capacitor. The input amplitude depends on the position of the gain switch at pin 2.

Video gain switch (pin 2)

Low level selects 1 V video input amplitude at pin 27. With no connection pin 2 floats HIGH, selecting 2,5 V video amplitude.

Black level (pin 26)

A capacitor connected to this pin stores the black level for the adaptive sync separator.

Video composite sync output VCS (pin 25)

This pin provides a video composite sync signal for the data-line decoder.

H.F. loss compensator (pins 3 and 4)

The h.f. loss compensator needs two capacitors for operation. The capacitor at pin 3 filters the video signal for the h.f. loss compensator. The h.f. amplitude information is stored in the capacitor connected to pin 4.

Dataline slicer (pins 5, 6 and 8)

A capacitor at pin 5 stores the amplitude information for the dataline slicer. The zero-level information is stored in a capacitor connected to pin 6. The capacitor at pin 8 is necessary for timing of the dataline slicer.

Phase detector (pin 9)

The phase information which is detected from the phase detector is stored in a capacitor connected to pin 9.

Oscillator (pin 11)

The one-pin oscillator needs a 10,000 MHz crystal (2 x dataline frequency) connected to pin 11.

Phase shifter (pin 12)

A clock filter for the dataline clock of 5,000 MHz is connected to the phase shifter at pin 12.

Outputs

The dataline clock output DLCL (pin 14) and the dataline data output DLD (pin 15) provide signals for the dataline decoder.

Data reset DAR (pin 22)

The dataline slicer needs a reset signal each line, for signal timing see Fig. 3.

APPLICATION DATA (continued)

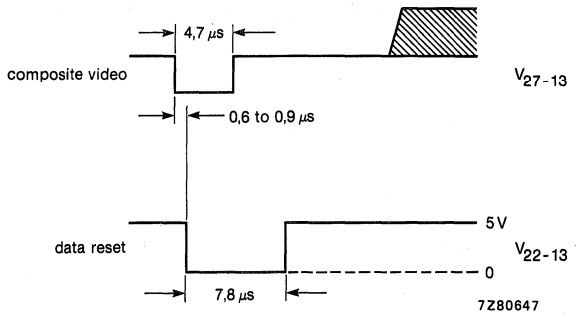


Fig. 3 Data-reset input signal timing in relation to composite video signal.

DATALINE SLICER

GENERAL DESCRIPTION

The SAA5236 is a bipolar integrated circuit for dataline receivers. It extracts the dataline signal from the video signal and regenerates the dataline clock. It also provides signals for the dataline decoder.

Features

- Adaptive dataline slicer
- Dataline clock regenerator
- Buffered clock and data outputs
- Buffered composite sync output
- Gain switch for the video input signal

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)		V_{CC}	10,8	12,0	13,2	V
Supply current	V_{CC} = 12 V	I_{13}	–	70	–	mA
Composite video input (pin 19) (peak-to-peak value)	pin 1 LOW	$V_{19(p-p)}$	0,7	1,0	1,4	V
	pin 1 floating	$V_{19(p-p)}$	1,75	2,5	3,5	V
Storage temperature range		T_{stg}	−20	–	+125	°C
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

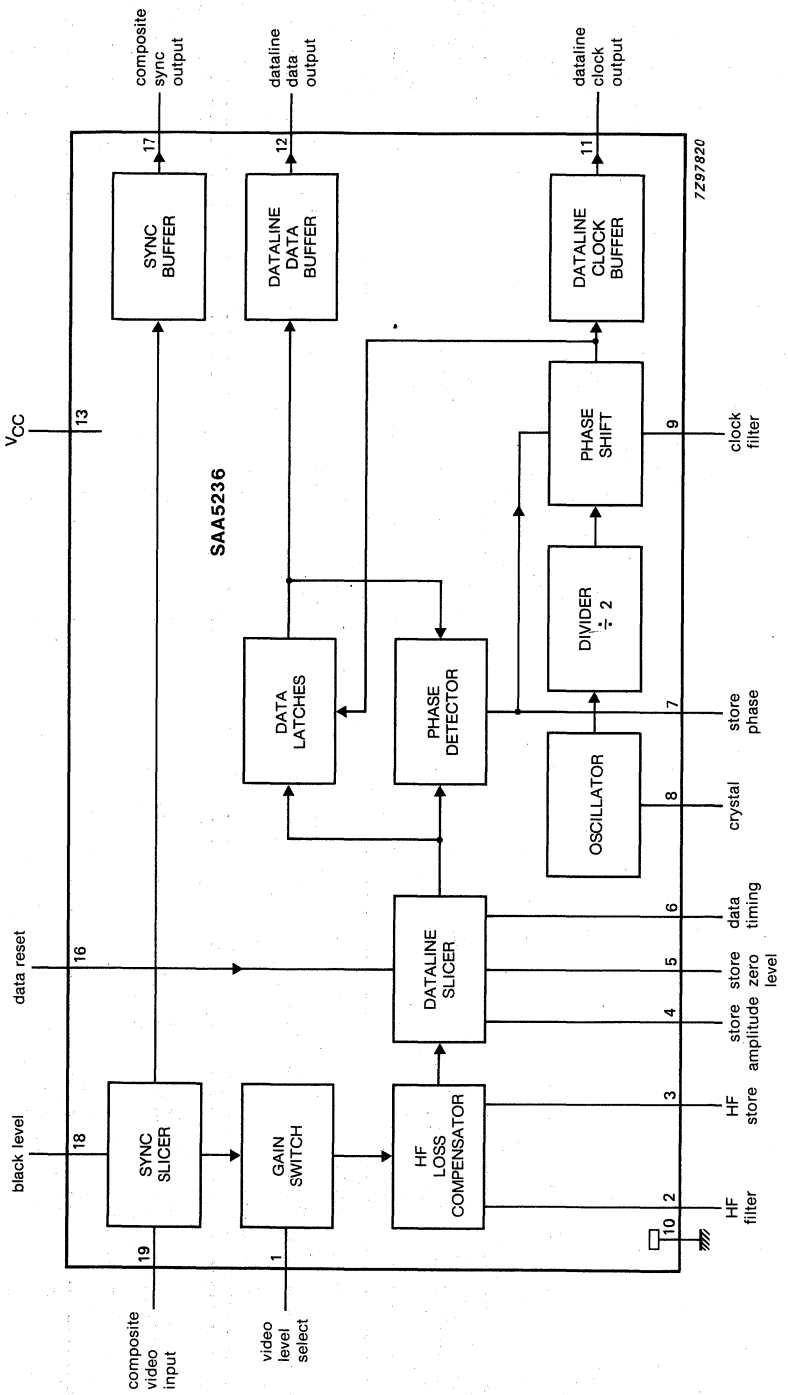


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)		V_{CC}	–	13,2	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 62 K/W

CHARACTERISTICS

V_{CC} = 12 V, T_{amb} = 25 °C, external components as shown in Fig. 2; all voltages are with reference to pin 10 (ground); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)		V_{CC}	10,8	12,0	13,2	V
Supply current	V_{CC} = 12 V	I_{13}	–	70	–	mA
Video input and sync separator (pin 19)						
Composite video input (peak-to-peak value)	pin 1 LOW	$V_{19(p\text{-}p)}$	0,7	1,0	1,4	V
	pin 1 floating	$V_{19(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance		$\lvert Z_{source}\rvert$	–	–	250	Ω
Sync amplitude (peak-to-peak value)		$V_{19(p\text{-}p)}$	0,1	–	1,0	V
Video level select (pin 1)						
Low level						
input voltage		V_1	0	–	0,8	V
input current		$-I_1$	0	–	150	μA
High level						
input voltage		V_1	2,0	–	5,5	V
input current		I_1	0	–	1	mA
Composite sync output (pin 17)						
Low level output voltage		V_{17}	0	–	0,4	V
High level output voltage		V_{17}	2,4	–	5,5	V
Sync separation delay time		t_d	–	0,35	–	μs

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Data reset input (pin 16)						
Data reset ON		V_{16}	0	–	0,5	V
Data reset OFF		V_{16}	1,0	–	5,5	V
Input current		I_{16}	−10	–	+10	μA
Dataline slicer (pin 19)						
Dataline amplitude (peak-to-peak value)	pin 1 LOW	$V_{19(p-p)}$	0,3	0,46	0,7	V
	pin 1 floating	$V_{19(p-p)}$	0,75	1,15	1,75	V
Dataline clock output (pin 11)						
A.C. output voltage (peak-to-peak value)		$V_{11(p-p)}$	2,5	3,5	4,5	V
Output voltage (d.c. centre)		V_{11}	–	4,0	–	V
Load capacitance		C_L	–	–	40	pF
Rise and fall times		t_r, t_f	20	30	45	ns
Delay of falling edge relative to edges of dataline data output		t_d	−20	–	+20	ns
Dataline data output (pin 12)						
A.C. output voltage (peak-to-peak value)		$V_{12(p-p)}$	2,5	3,5	4,5	V
Output voltage (d.c. centre)		V_{12}	–	4,0	–	V
Load capacitance		C_L	–	–	40	pF
Rise and fall times		t_r, t_f	20	30	45	ns

APPLICATION INFORMATION

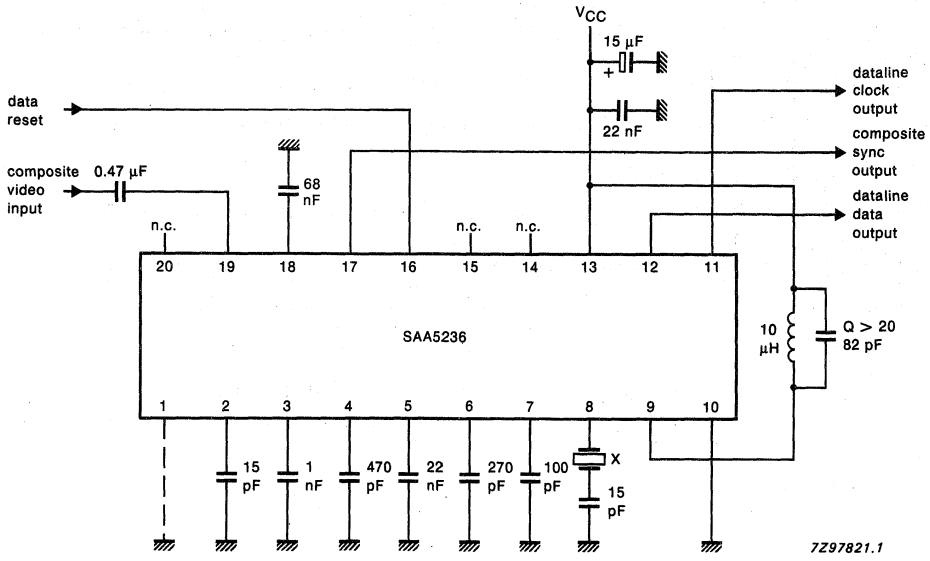


Fig. 2 Application circuit; crystal (X) frequency = 10,000 MHz.

DEVELOPMENT DATA

Composite video input (pin 19)

The composite video has to be fed into this input via a clamp capacitor. The input amplitude depends on the position of the gain switch at pin 1.

Gain switch (pin 1)

Low level selects 1 V video input amplitude at pin 19. With no connection, pin 1 floats HIGH and selects 2,5 V video amplitude.

Black level (pin 18)

A capacitor connected to this pin stores the black level for the adaptive sync separator.

Composite sync output (pin 17)

This pin provides a composite sync signal for the dataline decoder.

HF loss compensator (pins 2 and 3)

The HF loss compensator requires two capacitors for operation. The capacitor at pin 2 filters the video signal for the HF loss compensator, and the capacitor at pin 3 stores HF amplitude information.

Dataline slicer (pins 4, 5 and 6)

The capacitor at pin 4 stores amplitude information for the dataline slicer, the capacitor at pin 5 stores zero-level information and the capacitor at pin 6 is for dataline slicer timing.

APPLICATION INFORMATION (continued)

Phase detector (pin 7)

The phase information detected by the phase detector is stored in the capacitor at pin 7.

Oscillator (pin 8)

The single-pin oscillator requires a 10,000 MHz crystal (2 x dataline frequency) connected to pin 8.

Phase shift (pin 9)

A filter for the dataline clock (5,000 MHz) is connected to the phase shift circuit at pin 9.

Dataline clock and data outputs (pins 11 and 12)

Signals for the dataline decoder are provided from these outputs.

Data reset (pin 16)

The dataline slicer needs a reset signal for each line, for signal timing see Fig. 3.

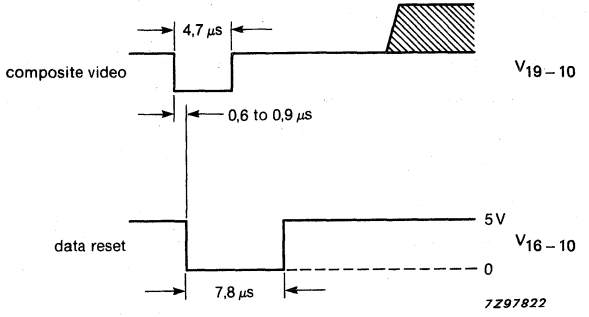


Fig. 3 Timing relationship of data reset input to composite video signal.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I²C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

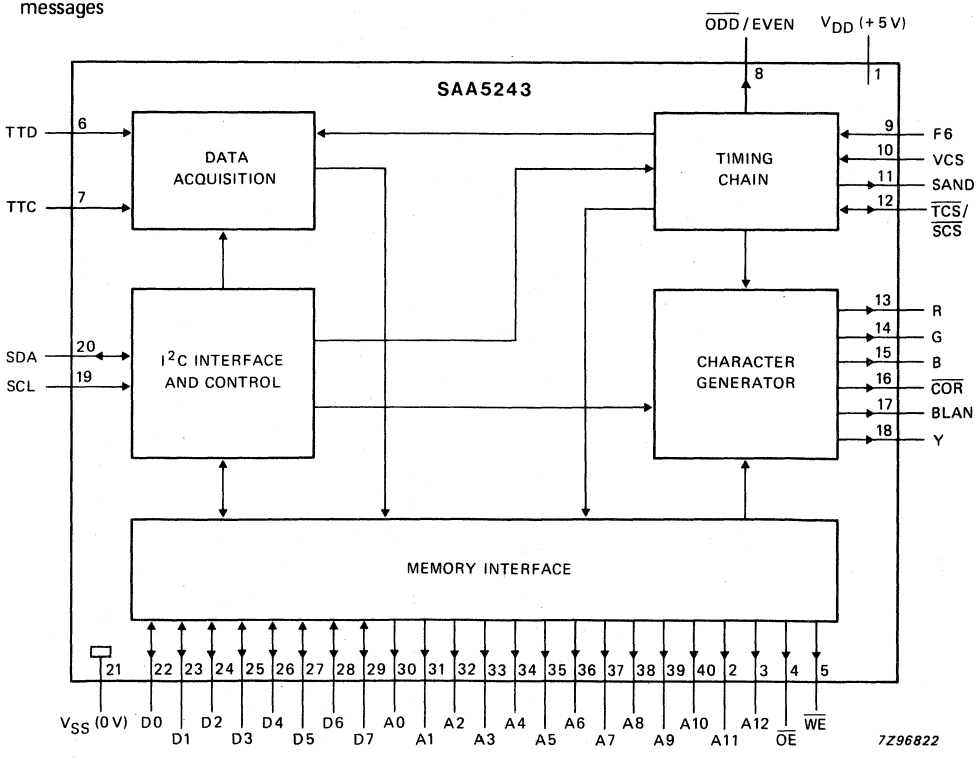


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages
SAA5243P/T	West European and Turkish languages

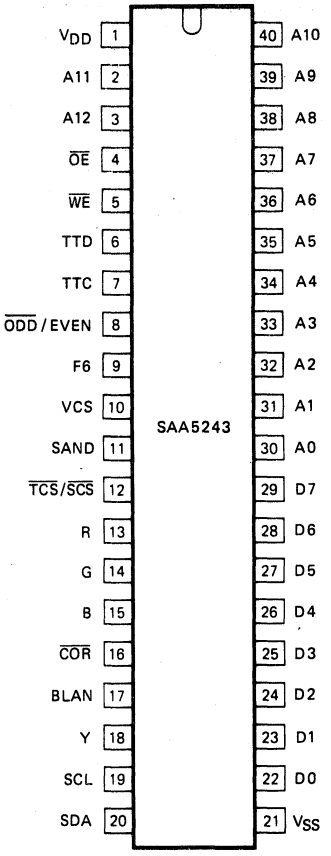


Fig.2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply:** + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address:** three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable:** active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock**: 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{ODD}$/EVEN	**$\overline{Odd}$/Even**: for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction:** open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking:** open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground:** open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	D0-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	−0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	−0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$		V_I	−0.3	10.0	V
Output voltage range					
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y		V_O	−0.3	7.5	V
$\overline{TCS}/\overline{SCS}$		V_O	−0.3	10.0	V
Storage temperature range		T_{stg}	−20	+125	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable $1 \geqslant 2.0$ V; data stable $0 \leqslant 0.8$ V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^2C-bus timings are referred to $V_{IH} = 3$ V and $V_{IL} = 1.5$ V. For waveforms see Fig.8.
12. The memory interface timings are referred to $V_{IL} = 1.5$ V. For waveforms see Fig.9.

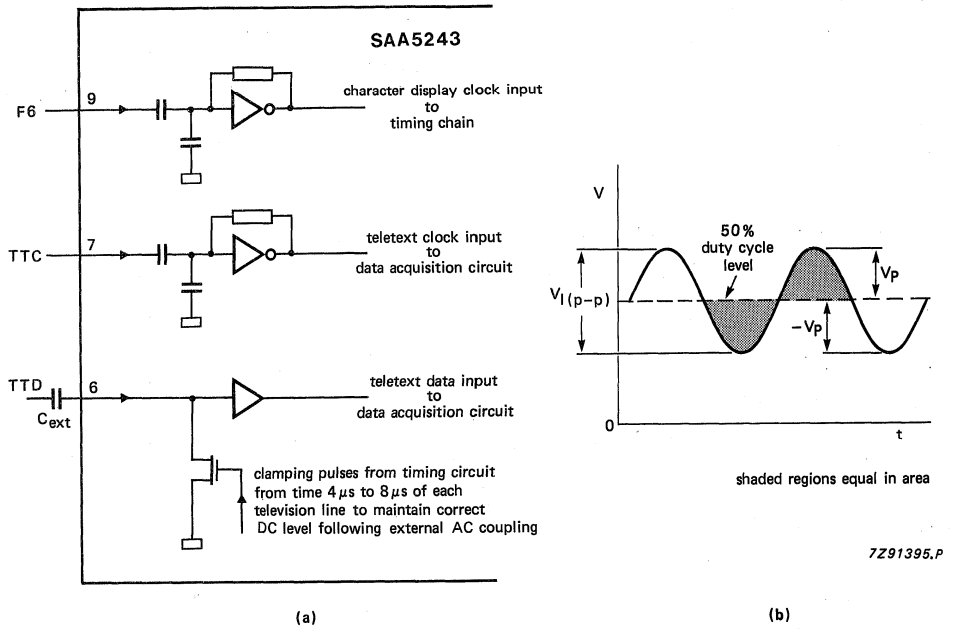
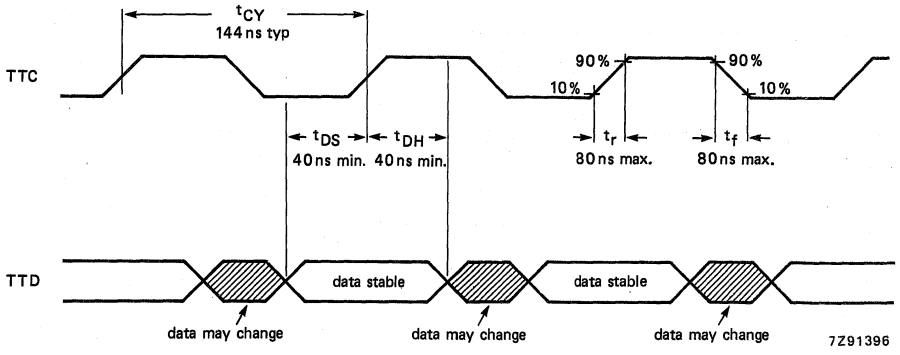


Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig.4 Teletext data input timing.

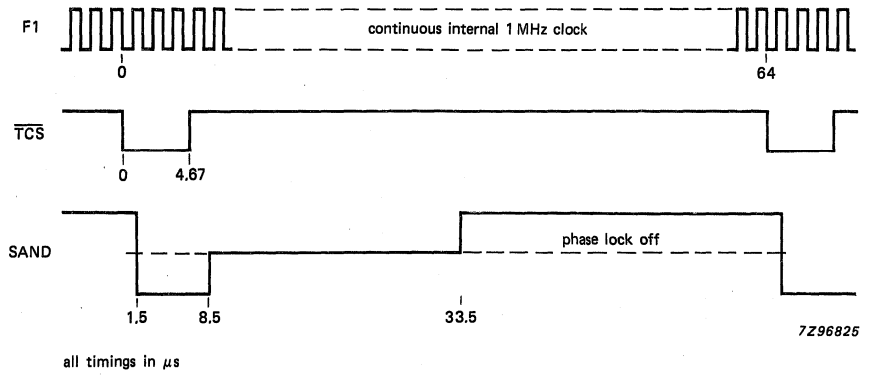
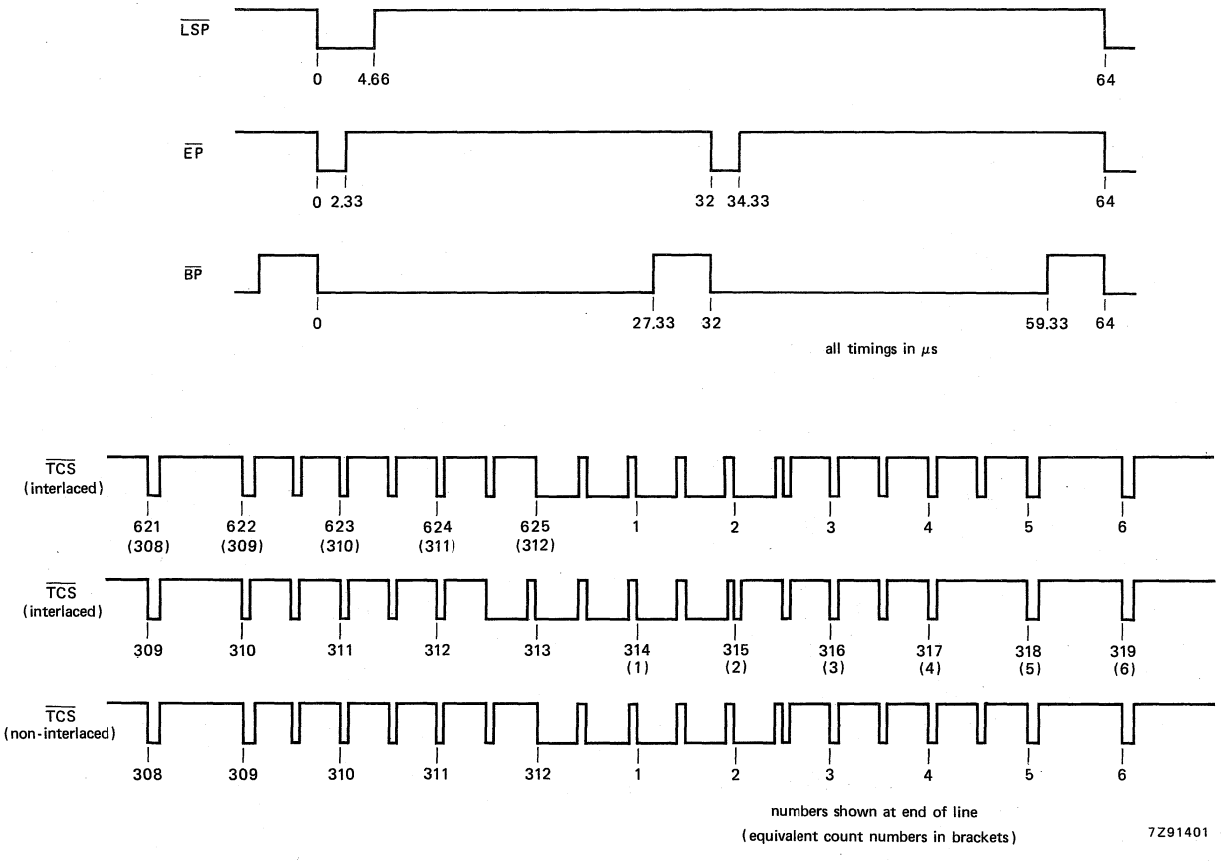


Fig.5 Synchronization timing.



Line sync pulses ($\overline{\text{LSP}}$), equalizing pulses ($\overline{\text{EP}}$) and broad pulses ($\overline{\text{BP}}$) are combined to provide the text composite sync waveform ($\overline{\text{TCS}}$) as shown. All timings measured from falling edge of $\overline{\text{LSP}}$ with a tolerance of ± 100 ns.

Fig.6 Composite sync waveforms.

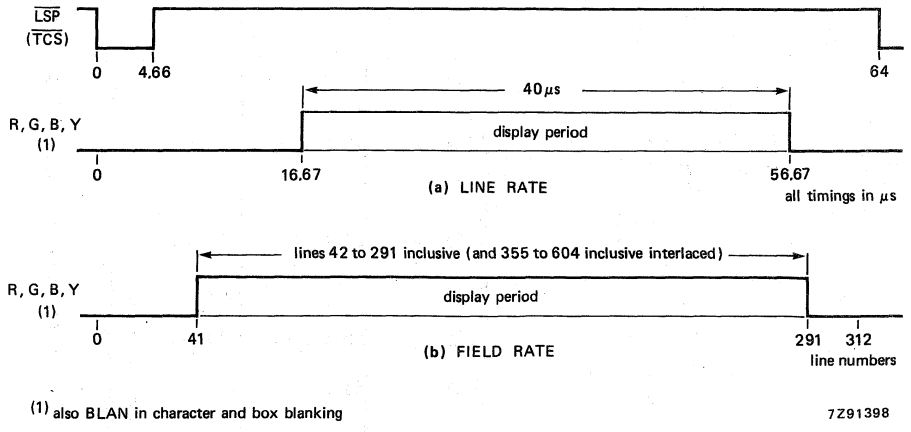


Fig.7 Display output timing (a) line rate (b) field rate.

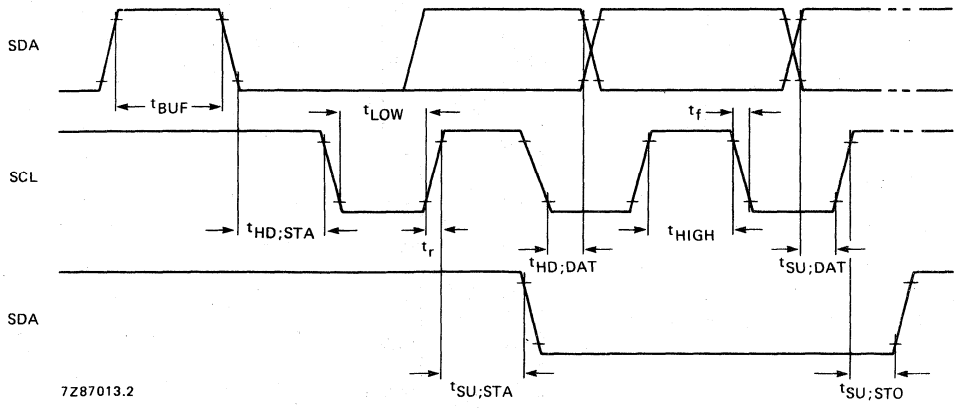


Fig.8 I^2C-bus timing.

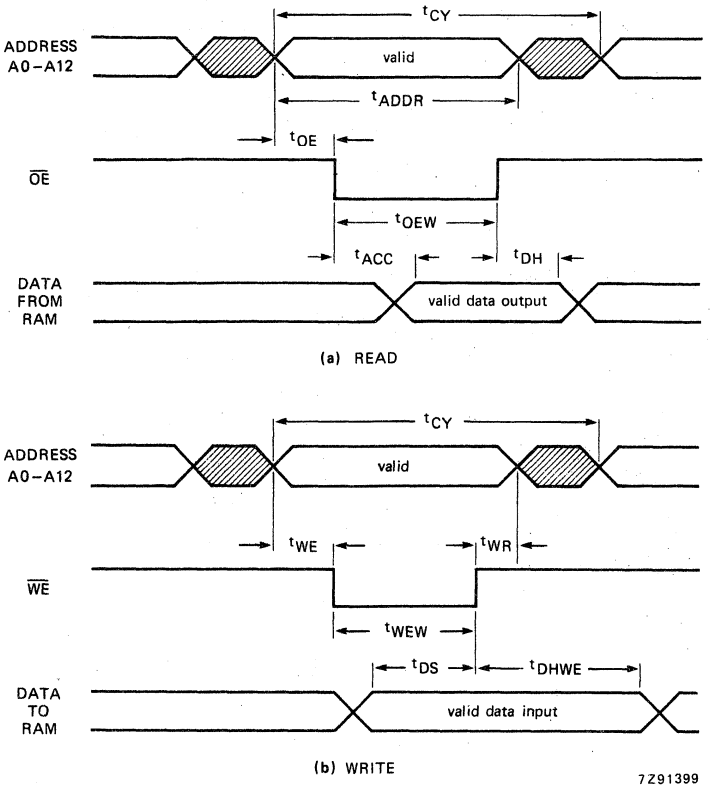
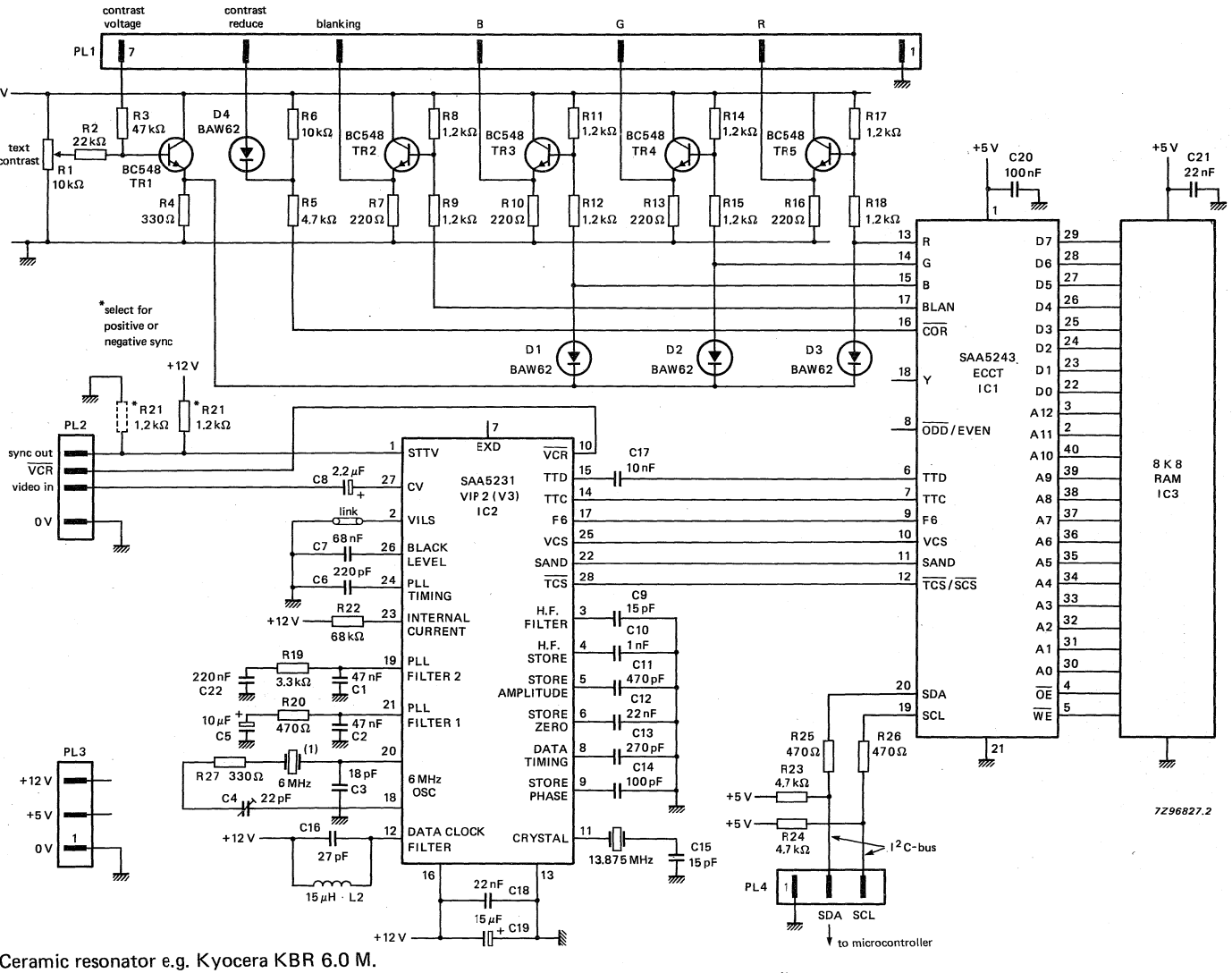


Fig.9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION



(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

Fig. 10 ECCT based multi[illegible]ge decoder circuit diagram.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

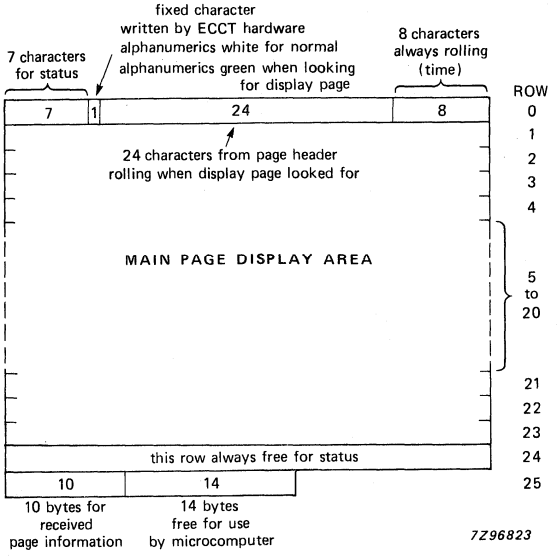


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
$\overline{\text{PBLF}}$	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode	
T0, T1	interlace/non-interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for DO CARE bits.
When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

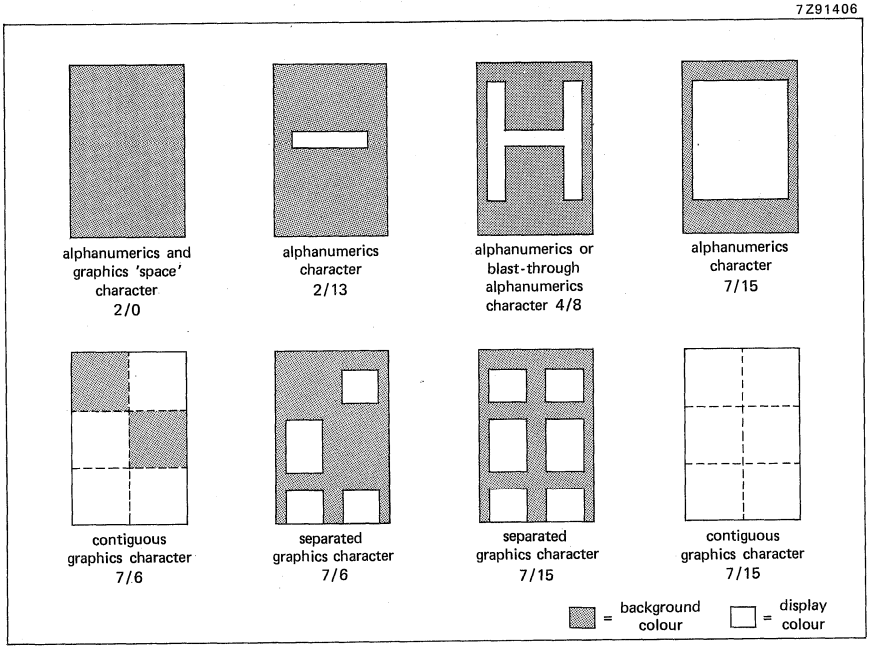


Fig.12 Alphanumeric and graphic options.

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black																
0	0	0	1	1	alpha - numerics red	graphics red																
0	0	1	0	2	alpha - numerics green	graphics green																
0	0	1	1	3	alpha - numerics yellow	graphics yellow																
0	1	0	0	4	alpha - numerics blue	graphics blue																
0	1	0	1	5	alpha - numerics magenta	graphics magenta																
0	1	1	0	6	alpha - numerics cyan	graphics cyan																
0	1	1	1	7	alpha - ** numerics white	graphics white																
1	0	0	0	8	flash	conceal display																
1	0	0	1	9	** steady	** contiguous graphics																
1	0	1	0	10	** end box	separated graphics																
1	0	1	1	11	start box	* ESC																
1	1	0	0	12	** normal height	** black back - ground																
1	1	0	1	13	double height	new back - ground																
1	1	1	0	14	* SO	hold graphics																
1	1	1	1	15	* SI	** release graphics																

MBA429

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4b Character data input decoding, East European languages (SAA5243P/H)

B I T S b_8 b_7 b_6 b_5	0 0 0 0	0 0 0 1	0 or 1 0 1 0	0 0 1 1	0 or 1 0 1 1	0 0 1 0 0	0 0 1 0 1	0 1 1 0 0	0 1 1 0 1	0 1 1 1 0	0 1 1 1 1	1 0 0 0 0	1 0 0 0 1	1 1 0 0 0	1 1 0 0 1	1 1 1 1 0	1 1 1 1 1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ column → row ↓	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	* ESC															
1 1 0 0	12	** normal height	black ** background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22497.5

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4c Character data input decoding, Arabic and English languages (SAA5243P/K)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b_7	0	0	1	0	1	1	0	0	1	1	1	1	0	0	1	1	1	1
b_6	0	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1	1	1
b_5	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	** normal height	black ** back–ground															
1 1 0 1	13	double height	new back–ground															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22660.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1
b_6	0	0	1	1	1	1	0	0	1	1	1	1	0	0	1	1	1
b_5	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black															
0 0 0 1	1	alpha-numerics red	graphics red															
0 0 1 0	2	alpha-numerics green	graphics green															
0 0 1 1	3	alpha-numerics yellow	graphics yellow															
0 1 0 0	4	alpha-numerics blue	graphics blue															
0 1 0 1	5	alpha-numerics magenta	graphics magenta															
0 1 1 0	6	alpha-numerics cyan	graphics cyan															
0 1 1 1	7	alpha-** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	TWIST															
1 1 0 0	12	** normal height	** black background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22679.4

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

Table 4e Character data input decoding, West European and Turkish languages (SAA5243P/T)

BITS b_8				0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7				0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6				0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5				0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4	b_3	b_2	b_1	column / row 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0	0	0	0	0	alpha - numerics black	graphics black															
0	0	0	1	1	alpha - numerics red	graphics red															
0	0	1	0	2	alpha - numerics green	graphics green															
0	0	1	1	3	alpha - numerics yellow	graphics yellow															
0	1	0	0	4	alpha - numerics blue	graphics blue															
0	1	0	1	5	alpha - numerics magenta	graphics magenta															
0	1	1	0	6	alpha - numerics cyan	graphics cyan															
0	1	1	1	7	** alpha - numerics white	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	** steady	** contiguous graphics															
1	0	1	0	10	** end box	separated graphics															
1	0	1	1	11	start box	* ESC															
1	1	0	0	12	** normal height	** black back - ground															
1	1	0	1	13	double height	new back - ground															
1	1	1	0	14	* SO	hold graphics															
1	1	1	1	15	* SI	** release graphics															

MBA428

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 4f Character data input decoding, Baltic and Cyrillic Russian (SAA5243P/R)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1		1		1	0	0	0	1	1
b_6	0	0	1	1	1	1	0	0	1		1		1	0	0	1	1	1
b_5	0	1	0	1	1	1	0	1	0		1		1	0	1	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0 alpha - numerics black	graphics black																
0 0 0 1	1 alpha - numerics red	graphics red																
0 0 1 0	2 alpha - numerics green	graphics green																
0 0 1 1	3 alpha - numerics yellow	graphics yellow																
0 1 0 0	4 alpha - numerics blue	graphics blue																
0 1 0 1	5 alpha - numerics magenta	graphics magenta																
0 1 1 0	6 alpha - numerics cyan	graphics cyan																
0 1 1 1	7 ** alpha - numerics white	graphics white																
1 0 0 0	8 flash	conceal display																
1 0 0 1	9 ** steady	** contiguous graphics																
1 0 1 0	10 ** end box	separated graphics																
1 0 1 1	11 start box	* ESC																
1 1 0 0	12 ** normal height	** black back - ground																
1 1 0 1	13 double height	new back - ground																
1 1 1 0	14 * SO	hold graphics																
1 1 1 1	15 * SI	** release graphics																

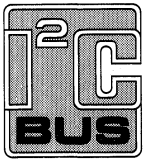
MBA648

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

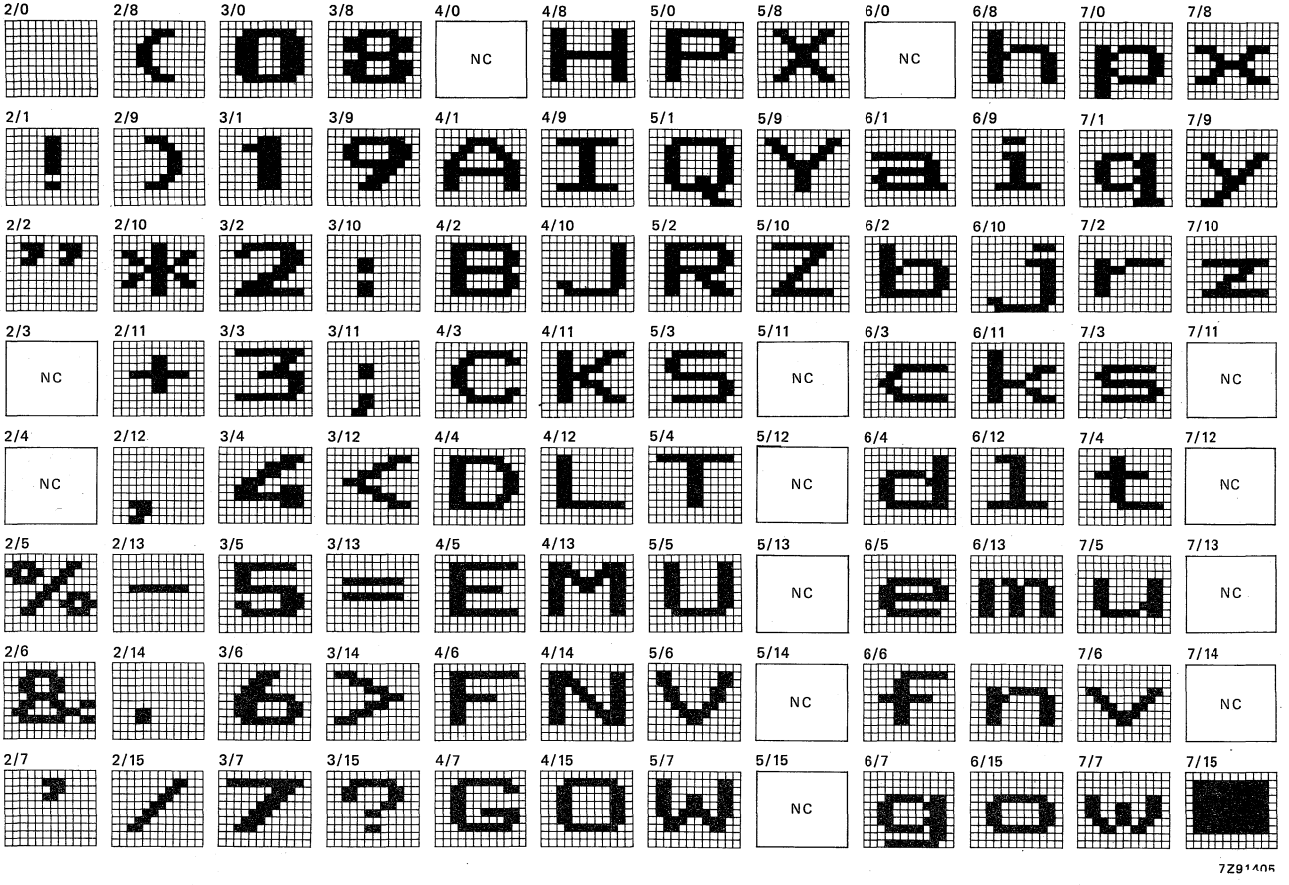
Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Table 5 SAA5243 basic character matrix



Where: NC national option character position.

APPLICATION INFORMATION (continued)

Table 6a SAA5243P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6b SAA5243P/H national option character set

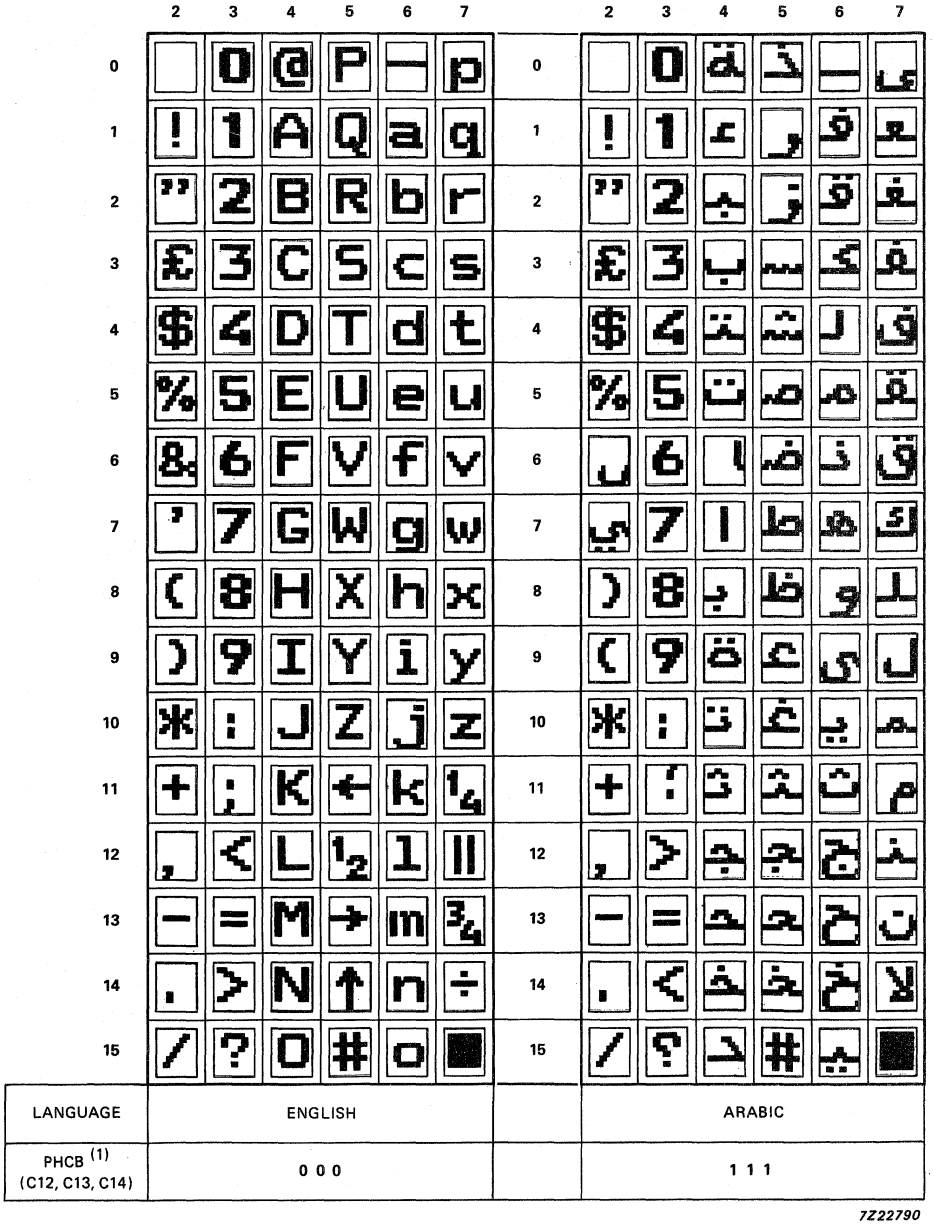
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

APPLICATION INFORMATION (continued)

Table 6c SAA5243P/K national option character set

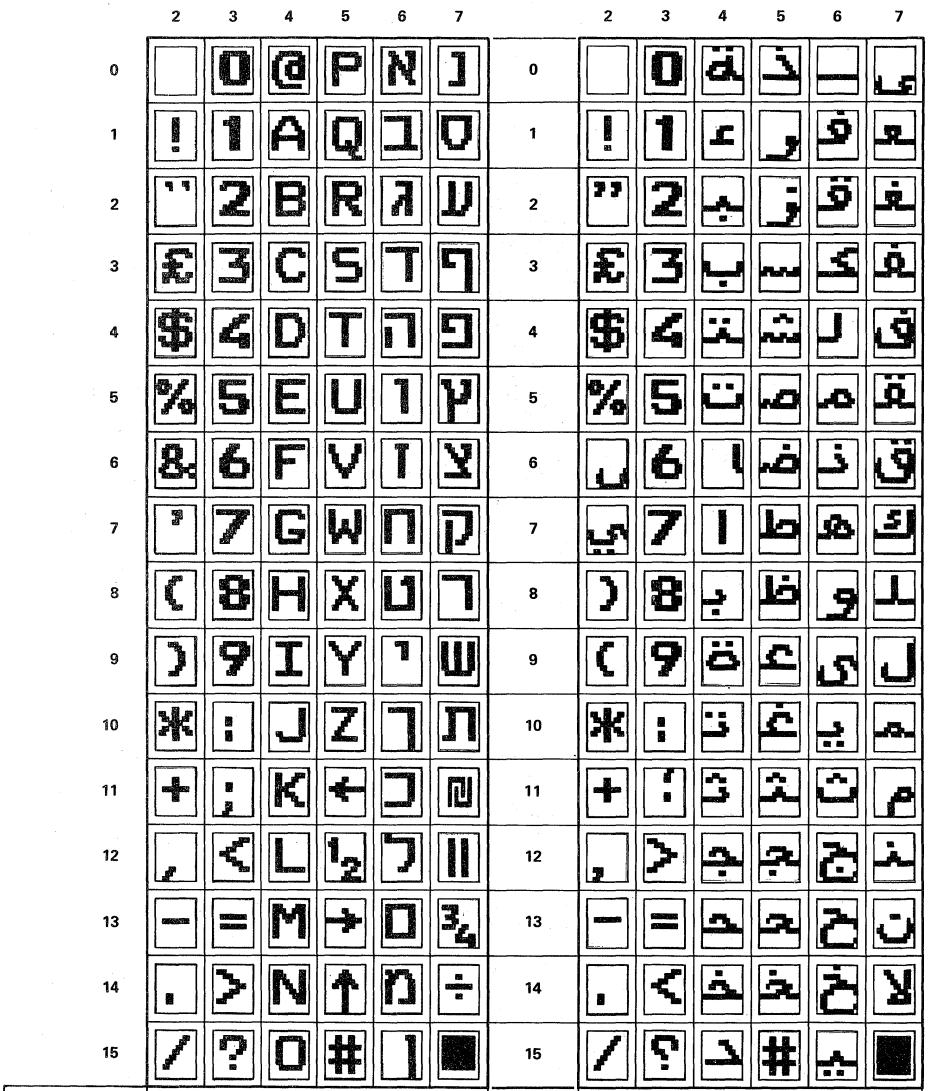


LANGUAGE	ENGLISH	ARABIC
PHCB (1) (C12, C13, C14)	0 0 0	1 1 1

7Z22790

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

Table 6d SAA5243P/L national option character set



LANGUAGE	HEBREW/ENGLISH		ARABIC
PHCB (1) (C12, C13, C14)	1 0 1		1 1 1

7Z22789

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

APPLICATION INFORMATION (continued)

Table 6e SAA5243P/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 5.

Table 6f SAA5243R/L national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ESTONIAN	0	1	0	#	Õ	Š	Ä	Ö	Ž	Ü	õ	š	ä	ö	ž	ü
LETTISH / LITHUANIAN	0	1	1	#	$	Š	ė	ę	Ž	č	ū	š	ą	ų	ž	į
RUSSIAN	1	0	0		0	Ю	П	ю	п							
				!	1	А	Я	а	я							
				"	2	Б	Р	б	р							
				#	3	Ц	С	ц	с							
				$	4	Д	Т	д	т							
				%	5	Е	У	е	у							
				ы	6	Ф	Ж	ф	ж							
				'	7	Г	В	г	в							
				(	8	Х	Ь	х	ь							
				)	9	И	Ъ	и	ъ							
				ж	:	Й	З	й	з							
				+	;	К	Ш	к	ш							
				,	<	Л	Э	л	э							
				−	=	М	Щ	м	щ							
				.	>	Н	Ч	н	ч							
				/	?	О	Ы	о	■							

MBA647

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

INTEGRATED VIP AND TELETEXT (IVT1.1)

GENERAL DESCRIPTION

The Integrated VIP and Teletext (IVT1.1) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on a reduced function version of the Enhanced Computer Controlled Teletext (ECCT) device (SAA5243).
The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critial or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

Features

- Complete teletext decoder including page memory in a single 40-pin DIL package
- Single + 5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I^2C-bus
- Option for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I^2C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I^2C-bus
- VCS to SCS mode for stable 525 line status display

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Supply current	I_{DD}	–	74	148	mA
Sync amplitude	V_{syn}	0.1	0.3	0.6	V
Video amplitude	V_{vid}	0.7	1.0	1.4	V
Crystal frequency	f_{XTAL}	–	27	–	MHz
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

SAA5244P : 40-lead DIL; plastic (SOT129).
SAA5244P : 42-lead SDIL; plastic (SOT270).
SAA5244GP : 44-lead QFP; plastic (SOT205A).

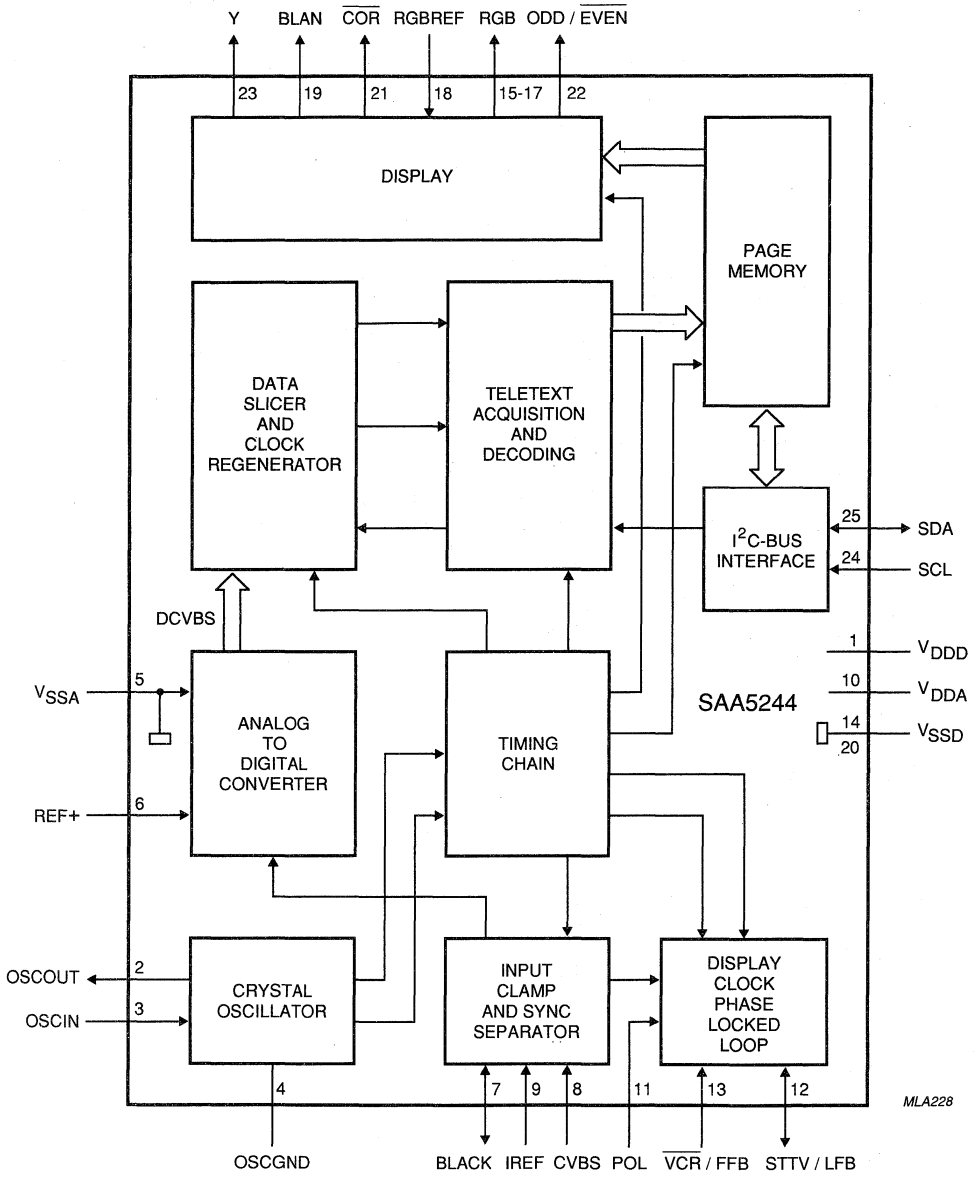


Fig.1 Block diagram for SOT129 (DIL40) package.

DEVELOPMENT DATA

PINNING

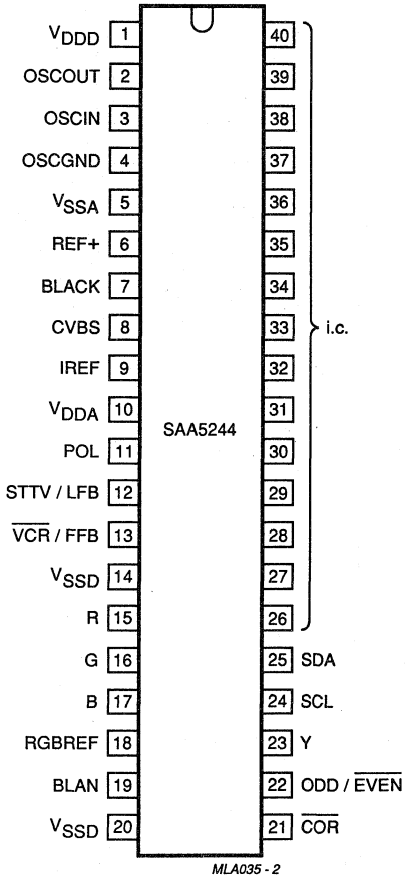


Fig.2(a) Pinning diagram; SOT129 (DIL40).

PINNING (continued)

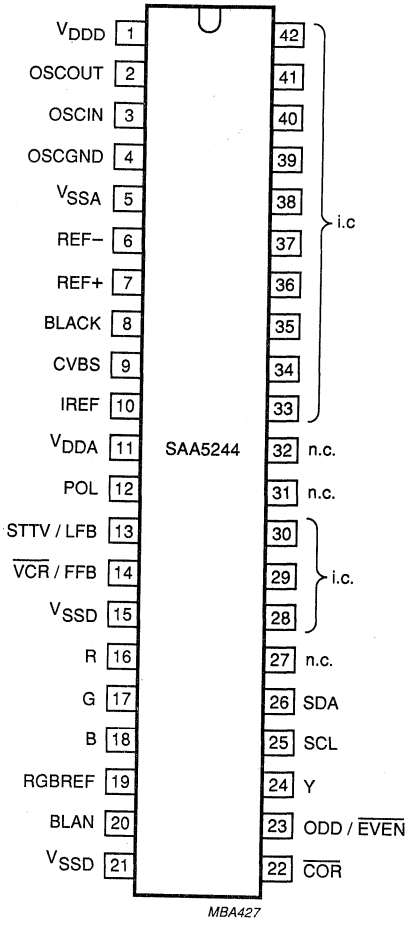


Fig.2(b) Pinning diagram; SOT270 (SDIL42).

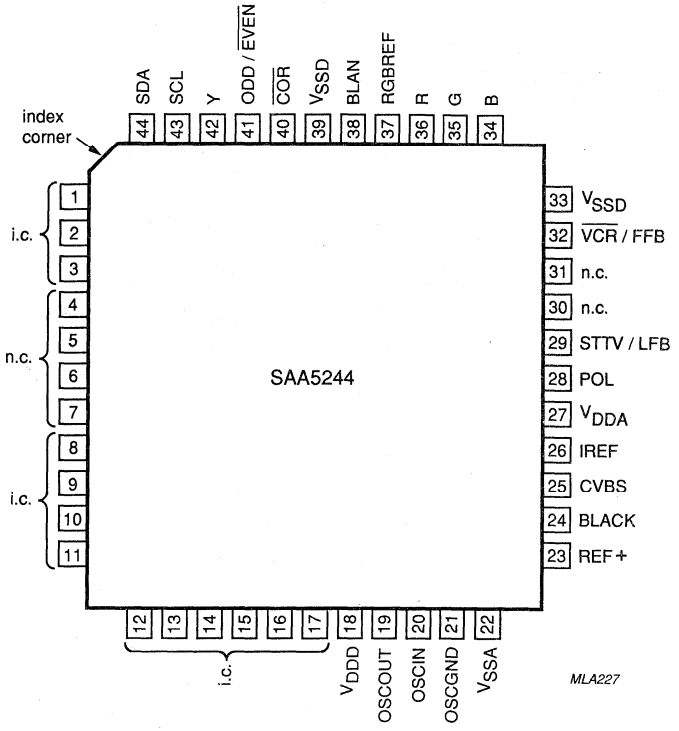


Fig.2(c) Pinning diagram; SOT205A (QFP44).

DEVELOPMENT DATA

Pinning description

SOT129	SOT270	SOT205A	Mnemonic	Description
1	1	18	V_{DDD}	+ 5 V supply to the digital sections of the device.
2	2	19	OSCOUT	27 MHz crystal oscillator output.
3	3	20	OSCIN	27 MHz crystal oscillator input.
4	4	21	OSCGND	0 V crystal oscillator ground.
5	5	22	V_{SSA}	0 V analog ground.
–	6	–	REF–	Negative reference voltage for the ADC. The pin should be connected to analog 0 V.
6	7	23	REF+	Positive reference voltage for the ADC. The pin should be connected to analog + 5 V.
7	8	24	BLACK	Video black level storage pin, connected to analog ground via a 100 nF capacitor.

Pinning description (continued)

SOT129	SOT270	SOT205A	Mnemonic	Description
8	9	25	CVBS	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
9	10	26	IREF	Reference current input pin, connected to analog ground via a 27 kΩ resistor.
10	11	27	V_{DDA}	+5 V supply to the analog sections of the device.
11	12	28	POL	STTV/LFB/FFB polarity selection pin.
12	13	29	STTV/LFB	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
13	14	32	$\overline{VCR}$/FFB	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode).
14	15	33	V_{SSD}	Connected to V_{SSD} for normal operation.
15	16	34	R	Dot rate character output of the RED colour information.
16	17	35	G	Dot rate character output of the GREEN colour information.
17	18	36	B	Dot rate character output of the BLUE colour information.
18	19	37	RGBREF	Input DC voltage to define the output high level on the RGB pins.
19	20	38	BLAN	Dot rate for blanking output.
20	21	39	V_{SSD}	0 V digital ground.
21	22	40	$\overline{COR}$	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output.
22	23	41	ODD/$\overline{EVEN}$	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
23	24	42	Y	Dot rate character output of teletext foreground colour information. Open drain output.
24	25	43	SCL	Serial clock input for I²C-bus. It can still be driven during power-down of the device.
25	26	44	SDA	Serial data port for the I²C-bus. Open drain output. It can still be driven during power-down of the device.
–	27,31, 32	4-7 30,31	n.c.	Not connected.
26-40	28-30 33-42	1-3 8-17	i.c.	Internally connected. Must be left open-circuit in application.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (all supplies)	V_{DD}	−0.3	6.5	V
Input voltage (any input)	V_I	−0.3	V_{DD} + 0.5	V
Output voltage (any output)	V_O	−0.3	V_{DD} + 0.5	V
Difference between V_{SSD} V_{SSA} and REF−	V_{Sdif}	−	± 0.25	V
Difference between V_{DDD} V_{DDA} and REF+	V_{Ddif}	−	± 0.25	V
Output current (each output)	I_O	−	± 10	mA
DC input or output diode current	I_{IOK}	−	± 20	mA
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 125	°C
Electrostatic handling*	V_{stat}	−2000	+ 2000	V

Failure rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

DEVELOPMENT DATA

* Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLIES						
Supply voltage range (V_{DD}–V_{SS})		V_{DD}	4.5	5.0	5.5	V
Total supply current		I_{DD}	–	74	148	mA
V_{DDD} supply current		I_{DDD}	–	50	100	mA
V_{DDA} supply current		I_{DDA}	–	16	32	mA
REF+ supply current		I_{REF+}	–	8	16	mA
INPUTS						
CVBS						
Sync amplitude		V_{syn}	0.1	0.3	0.6	V
Delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		t_{syn}	−150	0	150	ns
Change in sync delay between all black and all white video input at nominal levels		t_{syd}	0	–	25	ns
Video input amplitude (peak-to-peak)		$V_{vid(p-p)}$	0.7	1.0	1.4	V
Display PLL catching range			± 7	–	–	%
Source impedance		Z_{src}	–	–	250	Ω
Input capacitance		C_I	–	–	10	pF
IREF						
Resistor to ground		R_g	–	27	–	kΩ

parameter	conditions	symbol	min.	typ.	max.	unit
INPUTS (continued)						
POL						
Input voltage LOW		V_{IL}	−0.3	–	+ 0.8	V
Input voltage HIGH		V_{IH}	2	–	V_{DDD} + 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
LFB						
Input voltage LOW		V_{IL}	−0.3	–	+ 0.8	V
Input voltage HIGH		V_{IH}	2	–	V_{DDD} + 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input current	note 1	I_I	−1	–	+ 1	mA
Delay between LFB front edge and input video line sync		t_{lfb}	–	250	–	ns
$\overline{\text{VCR}}$/FFB						
Input voltage LOW		V_{IL}	−0.3	–	+ 0.8	V
Input voltage HIGH		V_{IH}	2	–	V_{DDD} + 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input current	note 1	I_I	−1	–	+ 1	mA
RGBREF						
Input voltage		V_I	−0.3	–	V_{DDD} + 0.5	V
Leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
DC current		I_{DC}	–	–	10	mA
SCL						
Input voltage LOW		V_{IL}	−0.3	–	+ 1.5	V
Input voltage HIGH		V_{IH}	3	–	V_{DDD} + 0.5	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Clock frequency		f_{scl}	0	–	100	kHz
Input rise time	10% - 90%	t_r	–	–	2	μs
Input fall time	90% - 10%	t_f	–	–	2	μs
Input capacitance		C_I	–	–	10	pF
INPUTS/OUTPUTS						
Crystal oscillator (OSCIN; OSCOUT)						
Crystal frequency		f_{XTAL}	–	27	–	MHz
Internal bias resistance (between OSCIN and OSCOUT)		$R_{x(bias)}$	40	–	1500	kΩ
Small signal voltage gain		G_v	3.5	–	–	–
Mutual conductance	f = 100 kHz	G_m	1.5	–	–	mA/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
BLACK						
Storage capacitor to ground		C_{blk}	–	100	–	nF
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
SDA						
Input voltage LOW		V_{IL}	−0.3	–	+ 1.5	V
Input voltage HIGH		V_{IH}	3	–	V_{DDD} + 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
Input rise time	10% - 90%	t_r	–	–	2	μs
Input fall time	90% - 10%	t_f	–	–	2	μs
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time	3 V to 1 V	t_f	–	–	200	ns
Load capacitance		C_L	–	–	400	pF

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
STTV						
Gain of STTV relative to video input		G_{stt}	0.9	1	1.1	
TCS amplitude		V_{tcs}	0.2	0.3	0.45	V
DC shift between TCS output and nominal video output		V_{DCs}	–	–	0.15	V
Output drive		I_O	–	–	3	mA
Load capacitance		C_L	–	–	100	pF
R, G and B						
Output voltage LOW		V_{OL}	0	–	0.2	V
Output voltage HIGH	$I_{OH} = \pm 2$ mA; RGBREF $\leqslant$ $V_{DD}-1.5$ V	V_{OH}	−10%	RGBREF	+ 10%	V
Output impedance		$\|Z_o\|$	–	–	200	Ω
Load capacitance		C_L	–	–	50	pF
DC current		I_{DC}	–	–	−3.3	mA
Output rise time	10% - 90%	t_r	–	–	20	ns
Output fall time	90% - 10%	t_f	–	–	20	ns
BLAN						
Output voltage LOW		V_{OL}	0	–	0.4	V
Output voltage HIGH		V_{OH}	1.1	–	2.8	V
Load capacitance		C_L	–	–	50	pF
Output rise time	10% - 90%	t_r	–	–	20	ns
Output fall time	90% - 10%	t_f	–	–	20	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
ODD/$\overline{\text{EVEN}}$						
Output voltage LOW	I_{OL} = + 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = –0.2 mA	V_{OH}	V_{DDD} –0.4	–	V_{DD}	V
Load capacitance		C_L	–	–	120	pF
Output rise time	0.6 to 2.2 V	t_r	–	–	50	ns
Output fall time	2.2 to 0.6 V	t_f	–	–	50	ns
$\overline{\text{COR}}$ and Y (open drain)						
Pull-up voltage at pin		V_{OH}	–	–	V_{DDD}	V
Output voltage LOW	I_{OL} = + 2 mA	V_{OL}	0	–	0.4	V
	I_{OL} = + 5 mA	V_{OL}	0	–	1	V
Load capacitance		C_L	–	–	25	pF
Output fall time	load resistor of 1.2 kΩ to V_{DDD}; measured between V_{DDD} –0.5 and 1.5 V	t_f	–	–	50	ns
Output leakage current	V_I = 0 to V_{DD}	I_{LO}	–10	–	+ 10	μA
Skew delay between display outputs R, G, B, $\overline{\text{COR}}$, Y, BLAN		T_{SK}	–	–	20	ns
TIMING						
I²C-bus						
Clock LOW period		t_{LOW}	4	–	–	μs
Clock HIGH period		t_{HIGH}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	170	–	–	ns
Set-up time from clock HIGH to STOP		$t_{SU;STO}$	4	–	–	μs
START set-up time following a STOP		t_{BUF}	4	–	–	μs
START hold time		$t_{HD;STA}$	4	–	–	μs
START set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs

Note to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

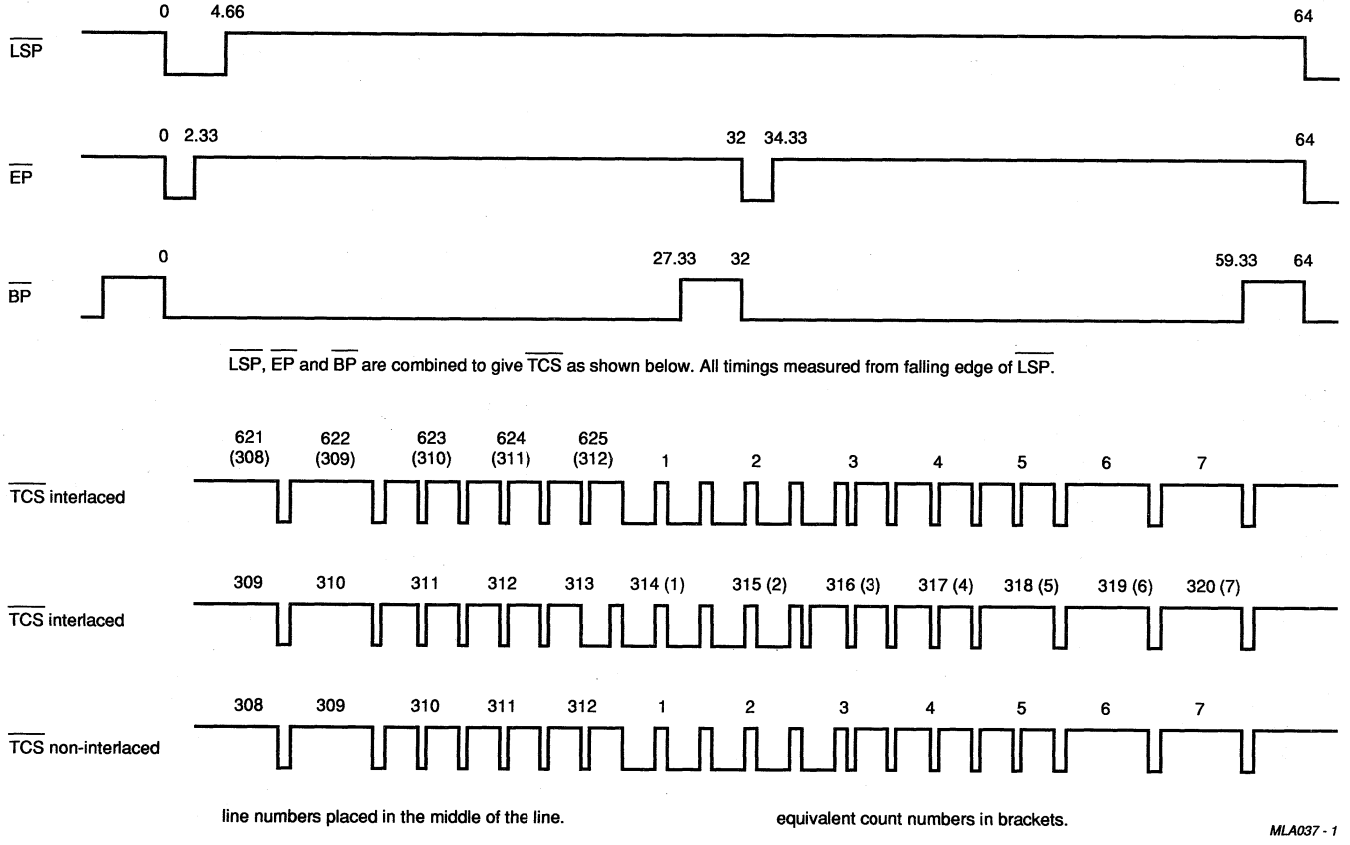


Fig.3 Composite sync waveforms.

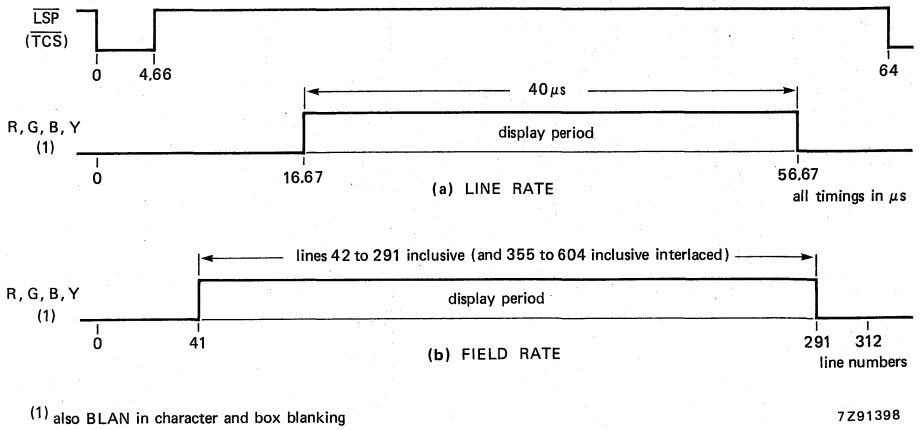


Fig.4 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

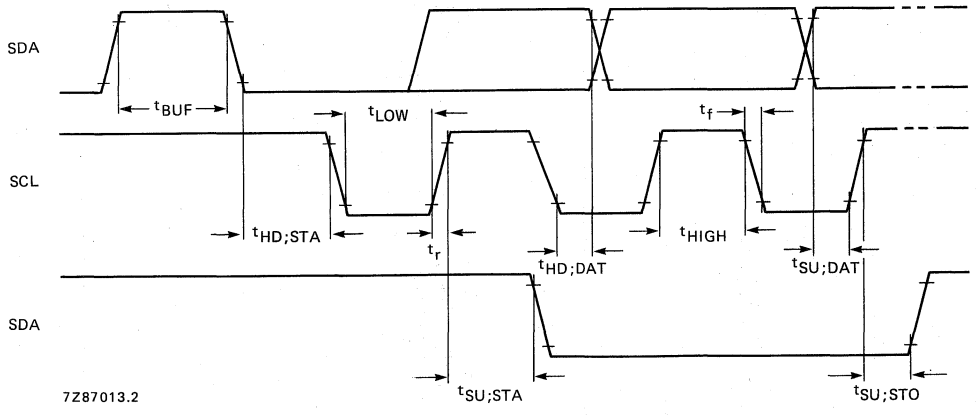


Fig.5 I²C-bus timing.

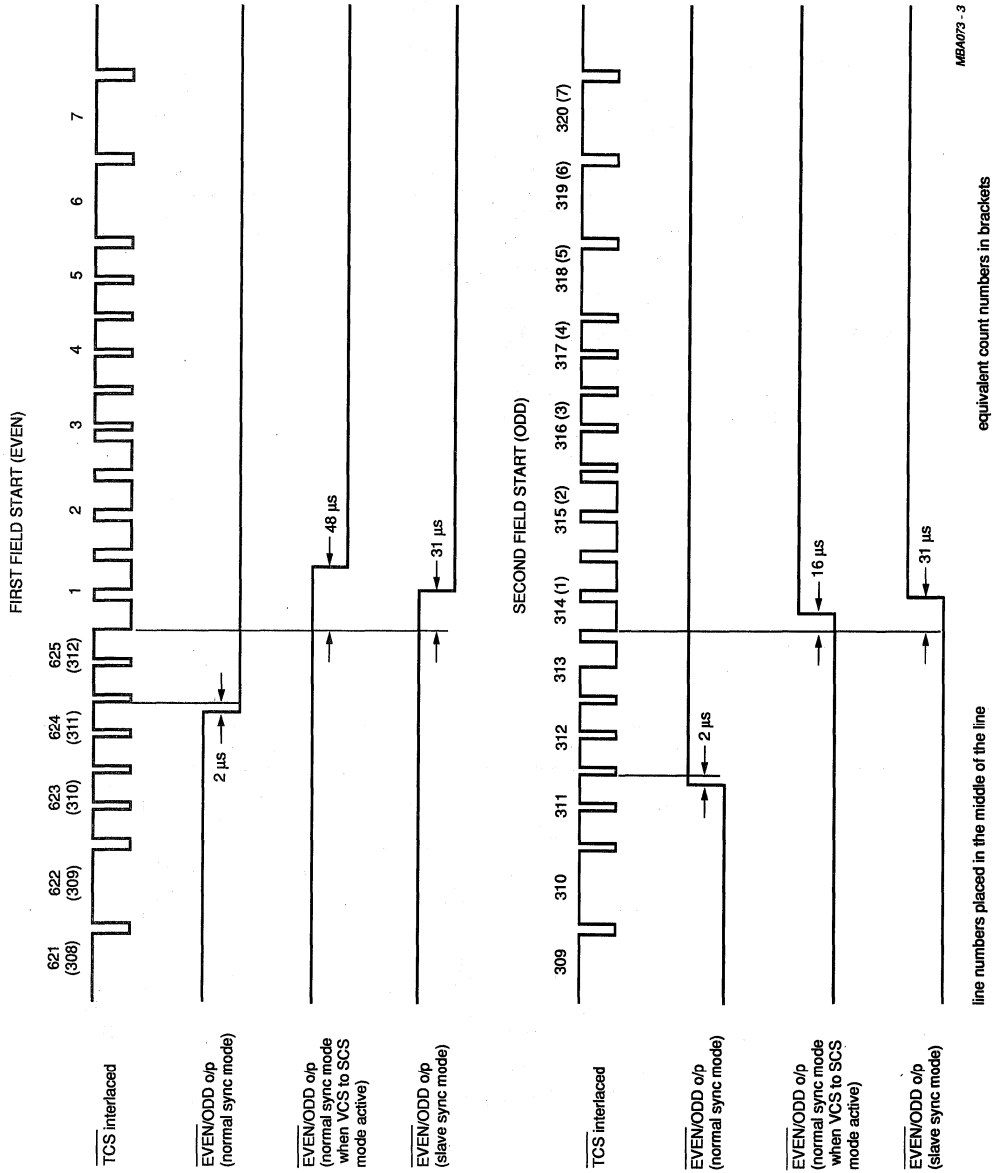
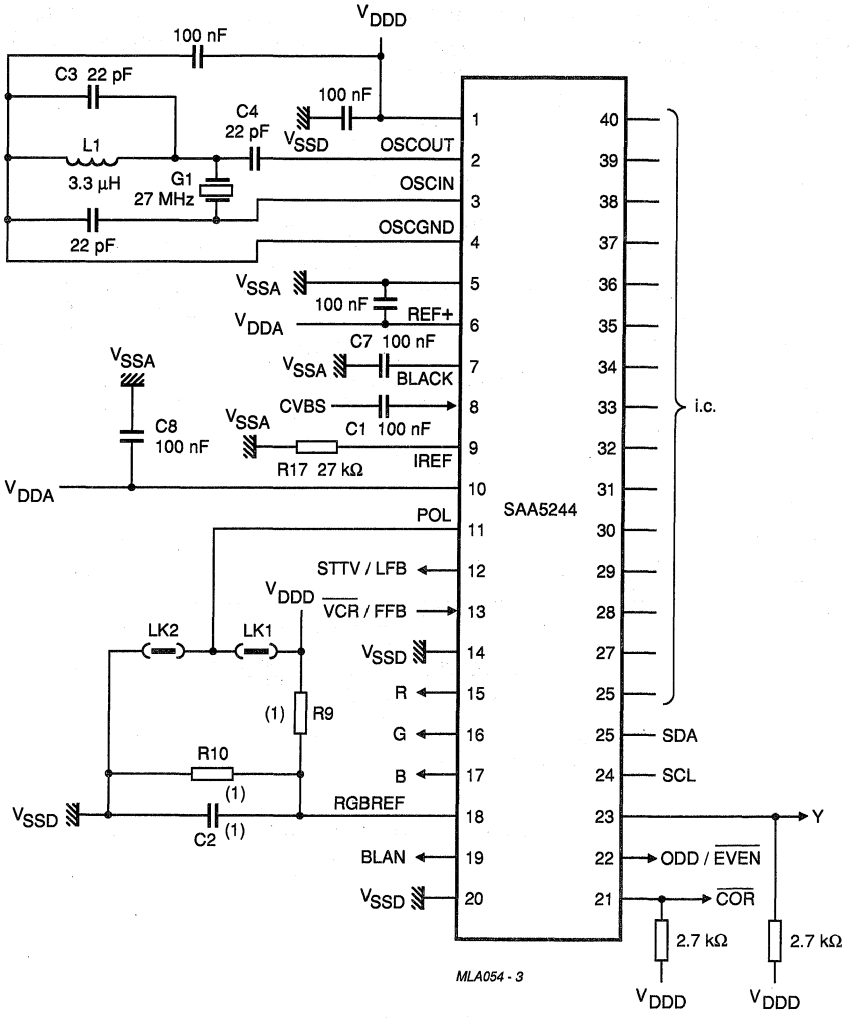


Fig.6 ODD/$\overline{\text{EVEN}}$ timing.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.7 Application diagram.

APPLICATION INFORMATION (continued)

IVT1.1 page memory organization

The organization of the page memory is illustrated by Fig.8. The IVT1.1 provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

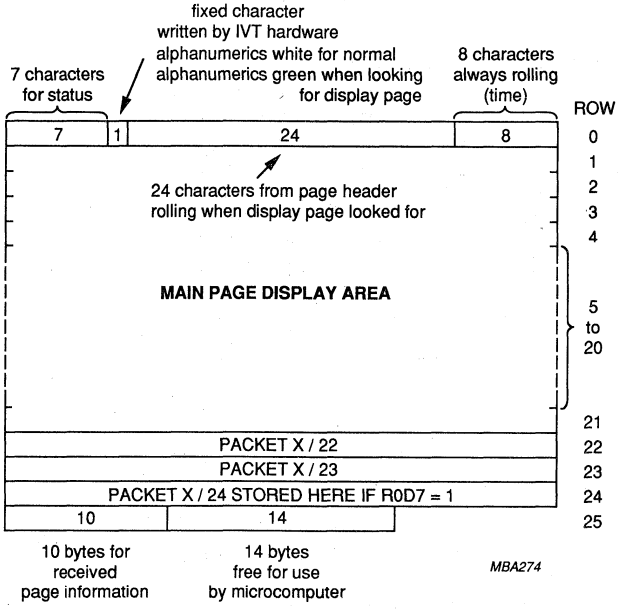


Fig.8 Basic page memory organization.

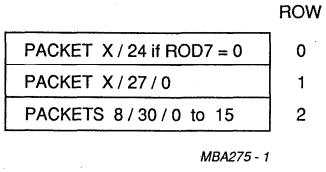


Fig.9 Organization of the extension memory.

Note to Fig.9

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT1.1 to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine
PU	page units page number
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
MU	minutes units
MT	minutes tens page sub-code
HU	hours units
HT	hours tens
C4-C14	transmitted control bits

APPLICATION INFORMATION (continued)

Register maps

IVT 1.1 mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 IVT1.1 register map

	register	D7	D6	D5	D4	D3	D2	D1	D0
Advanced control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	–	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	–	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	COL SC2	COL SC1	COL SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (news-flash/ subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	–	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Where: – indicates a bit which does not exist and must be written to 0 for future compatability.

Notes to Table 2

1. The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C-bus transmission byte.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. I^2C slave address is 0010001.

Where:

R0 Advanced control

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B.
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1.
DISABLE HDR ROLL	Disables green rolling header and time.
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0.
FREE RUN PLL	Will force the PLL to free run in all conditions.
X24 POS	Automatic display of FASTEXT prompt row when logic 1.

R1 Mode

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4).
TCS ON	Text composite sync or direct sync select.
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode.
ACQ $\overline{ON}$/OFF	Aquisition circuits turned off when logic 1.
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal.

R2 Page request address

COL SC0 - SC2	Point to start column for page request data (see Table 3).
TB	See note 4.

R3 Page request data — See Table 3.

R5, R6 Display control for normal and newsflash/subtitle

PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	Boxing function allowed on row 0 (row 1-23, 24).
DOUBLE HEIGHT	To display double height text.
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1.
REVEAL ON	To reveal concealed text.
CURSOR ON	To display cursor.
STATUS TOP	Row 25 displayed above or below the main text.

R9 Cursor row	
R0 to R4	Active row for data written to or read from memory via the I^2C-bus.
A0	Selects display memory page (when = 0) or extension packet memory (when = 1).
CLEAR MEM	When set to 1, clears the display memory. This bit is automatically reset.
SUPPL. BLAST	When set to 1, column 4b and 5b (of Table 5) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode.
R10 Cursor column	
C0 to C5	Active column for data written to or read from memory via the I^2C-bus.
SUPPL. ROW 0	When set to 1, column 4b and 5b (of Table 5) are mapped into columns 6 and 7 respectively, just for row 0 columns 0 to 7.
SUPPL. ROW 24	When set to 1, column 4b and 5b (of Table 5) are mapped into columns 6 and 7 respectively just for row 24.
R11 Cursor data	
D0 to D6	Data read from/written to memory via I^2C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed.
R11B Device status	
VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1.
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01000.
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1.

Table 3 Register map for page requests (R3)

start column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	Result
0	0	Interlaced 312.5/312.5 lines
0	1	Non-interlaced 312/313 lines*
1	0	Non-interlaced 312/312 lines*
1	1	SCS mode (scan composite sync)

* Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.10.

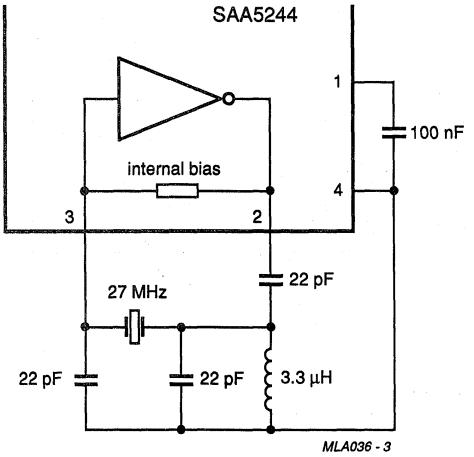
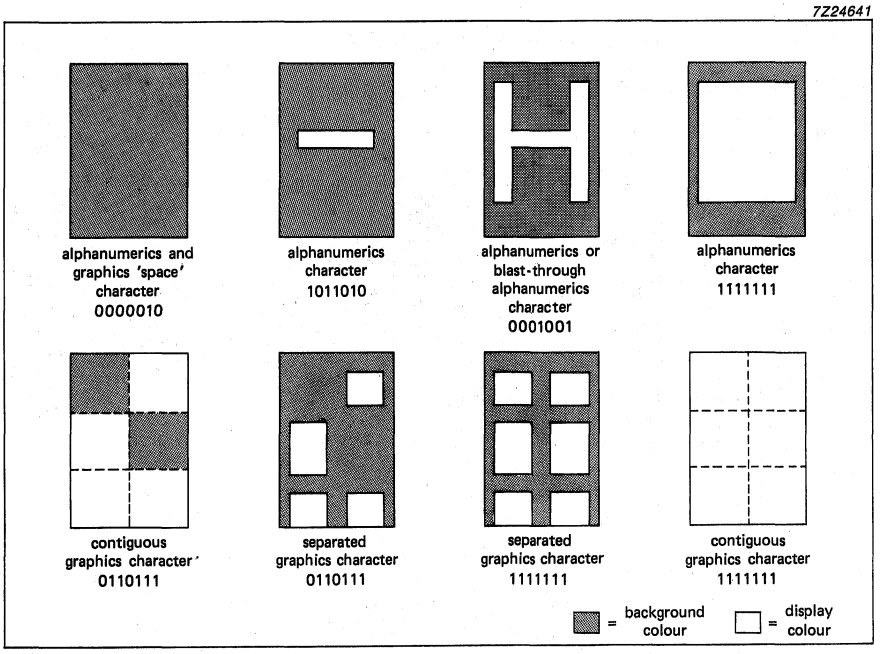


Fig.10 Crystal oscillator application diagram.

parameter	conditions	symbol	min.	typ.	max.	unit
CRYSTAL (27 MHz, 3rd overtone)						
Series capacitance		C1	–	1.7	–	fF
Parallel capacitance		C0	–	5.2	–	pF
Resonant resistance		Rr	–	–	50	Ω
Series resistance		R1	–	20	–	Ω
Ageing			–	± 5	–	10^{-6}/yr
Adjustment tolerance			–	± 40	–	10^{-6}
Drift			–	± 40	–	10^{-6}
Load capacitance		C_L	–	20	–	pF

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character set differs only in the 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix illustrated in Table 6. The IVT1.1 automatically decodes transmission bits C12 to C14.
Table 5 illustrates the character matrixes.



Character bytes are listed as transmitted from b1 to b7.

Fig.11 Character format.

APPLICATION INFORMATION (continued)

Table 5 Character data input decoding (SAA5244P/A)

BITS b_7 b_6 b_5 / b_4 b_3 b_2 b_1	row / column	0	1	2	2a	3	3a	4	4b+	5	5b+	6	6a	7	7a	AVAILABLE AS NATIONAL OPTIONS ONLY			
0 0 0 0	0	alpha - numerics black	graphics black			0		§		P		°		p		@	É	é	à
0 0 0 1	1	alpha - numerics red	graphics red	!		1		A		Q		a		q			é	ù	è
0 0 1 0	2	alpha - numerics green	graphics green	"		2		B		R		b		r		¼	ä	à	â
0 0 1 1	3	alpha - numerics yellow	graphics yellow	#		3		C		S		c		s		£	#	£	é
0 1 0 0	4	alpha - numerics blue	graphics blue	$		4		D		T		d		t		$	¤	$	ï
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%		5		E		U		e		u					
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&		6		F		V		f		v					
0 1 1 1	7	alpha - numerics white **	graphics white	'		7		G		W		g		w					
1 0 0 0	8	flash	conceal display	(		8		H		X		h		x		|	ö	ò	ô
1 0 0 1	9	steady **	contiguous graphics **	)		9		I		Y		i		y		¾	å	è	û
1 0 1 0	10	end box **	separated graphics	*		:		J		Z		j		z		÷	ü	ì	ç
1 0 1 1	11	start box	ESC *	+		;		K		Ä		k		ä		←	Ä	°	ë
1 1 0 0	12	normal hight **	black back - ground **	,		<		L		Ö		l		ö		½	Ö	ç	ê
1 1 0 1	13	double height	new back - ground	-		=		M		Ü		m		ü		→	Å	→	ù
1 1 1 0	14	SO *	hold graphics	.		>		N		^		n		ß		↑	Ü	↑	î
1 1 1 1	15	SI *	release graphics **	/		?		O		_		o				#	_	#	#

MBA266 - 1

For character version number (01000) see Register 11B.

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

\+ Columns 4b and 5b can only be accessed when supplementary character bits are set (see Registers 9 and 10).

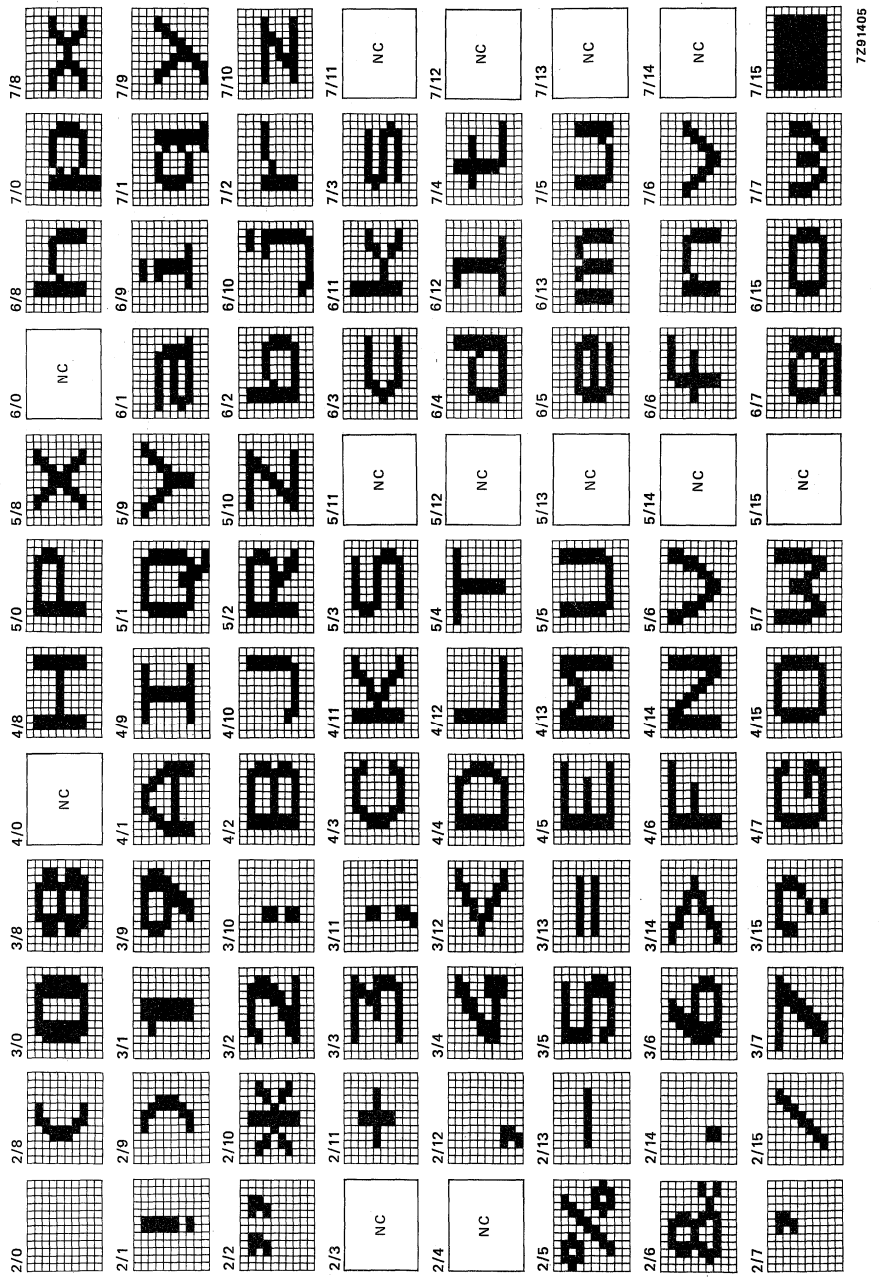
Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, for example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: 
5. The SAA5244 national option characters are illustrated in Table 7.
6. Characters 4b/11, 4b/12, 5b/10, 5b/11 and 5b/12 are special characters for combining with character 4b/10.
7. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 7.
8. Columns 4b and 5b are mapped into 4 and 5 respectively (replacing blast-through alphanumerics in the graphics mode) when enabled by R9 bit D7 set to 1.
9. Columns 4b and 5b are mapped into columns 6 and 7 respectively when enabled by R10 bit D6 (row 0 columns 0 to 7) and R10 bit D7 (row 24) set to 1.
10. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Table 6 SAA5244 basic character matrix



Where: NC = national option character position

Table 7 SAA5244A national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

7Z26538

Where: PHCB are the Page Header Control Bits. Other combinations default to English.

DEVELOPMENT DATA

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUIT

(USECCT)

GENERAL DESCRIPTION

The SAA5245 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 525-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5231, standard static RAMs and is controlled via the 2-wire I²C-bus The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 8 character matrix
- Field flyback (lines 5 to 19), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to seven different languages
- 25th display row for software generated status messages
- Automatic processing of gearing function
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I²C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- Odd/even field output for de-interlaced displays

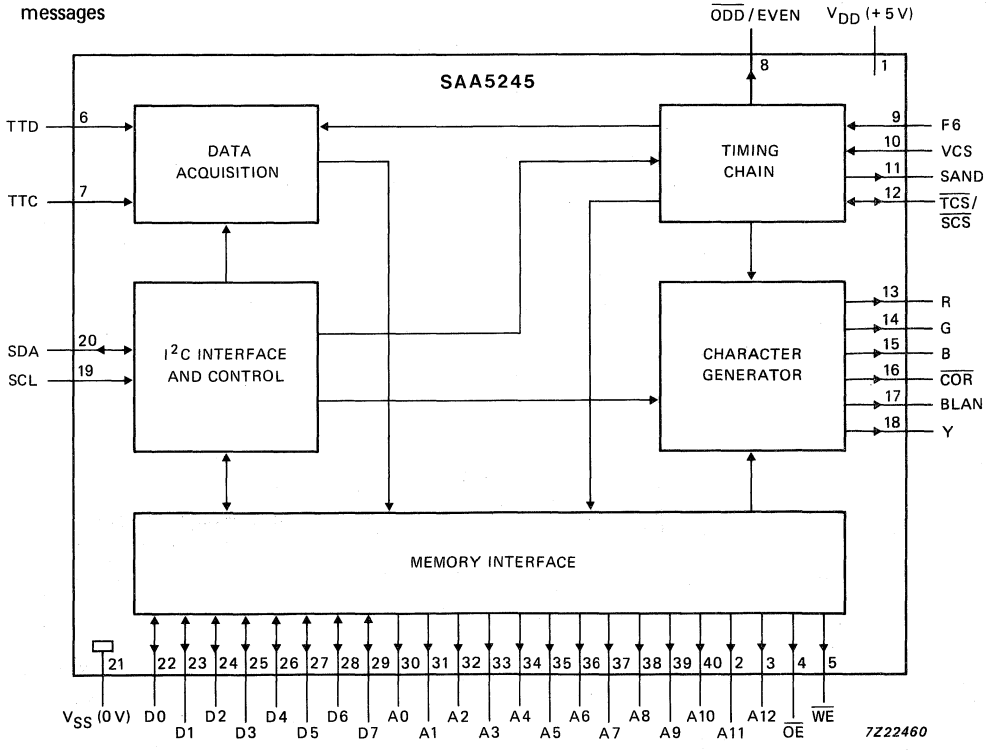


Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

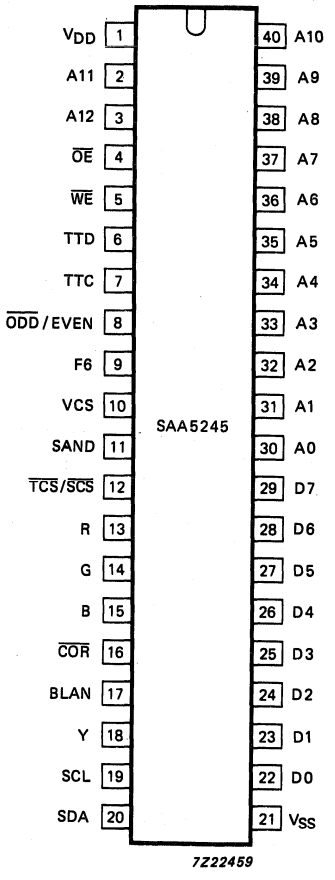


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply:** + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address:** three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable:** active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable:** active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data:** input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.

7	TTC	**Teletext Clock:** 5.727 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even:** for interlaced mode, the output changes once per field at 2 μs before the end of line 1 (263). The output is high for even fields and low for odd fields.
9	F6	**Character display clock:** 6.042 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync:** input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle:** 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}/\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync:** as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction:** open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking:** open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground:** open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data:** is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground:** 0 volts.
22-29	D0-D7	**8 RAM data lines:** 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address:** 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 1)	V_{DD}	−0.3	+ 7.5	V
Input voltage range				
VCS, SDA, SCL, D0 - D7	V_I	−0.3	+ 7.5	V
TTC, TTD, F6, $\overline{TCS}$/$\overline{SCS}$	V_I	−0.3	+ 10.0	V
Output voltage range				
SAND, A0 - A12, $\overline{OE}$, $\overline{WE}$, D0 - D7, SDA, $\overline{ODD}$/EVEN R, G, B, BLAN, $\overline{COR}$, Y	V_O	−0.3	+ 7.5	V
$\overline{TCS}$/$\overline{SCS}$	V_O	−0.3	+ 10.0	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	5.727	–	MHz
F6 clock frequency	f_{F6}	–	6.042	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
at I_{OH} = 0.1 mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5.5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	495	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	495	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns
QUALITY (note 13)					
Failure rate					
Failure rate at T_{amb} = 55 °C (1×10^{-6} failures per hour)		–	–	1000	FITS

DEVELOPMENT DATA

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C-bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig. 9.
13. This device shall meet the requirements of the Elcoma General Quality and Specification for ICs: URV - 4 - 2 - 59/601 (LSI).

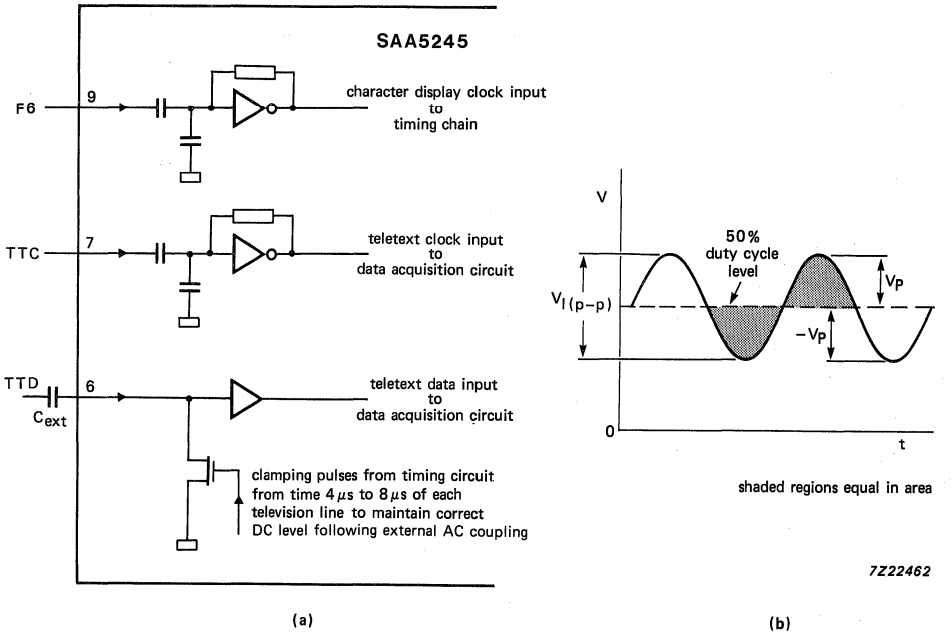
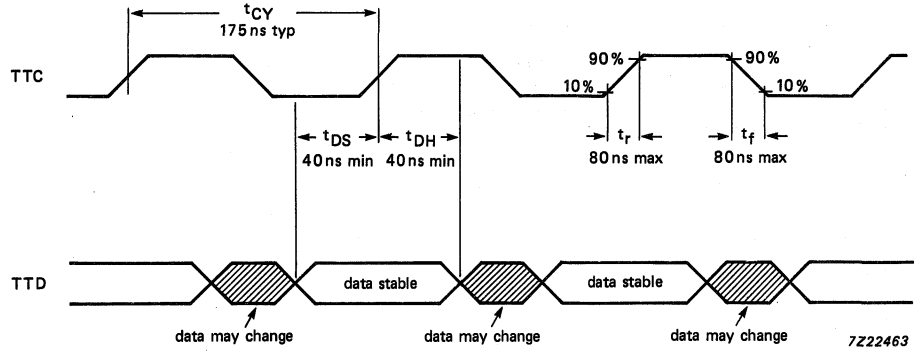


Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2.0 V; 0 is $\leqslant$ 0.8 V.

Fig. 4 Teletext data input timing.

DEVELOPMENT DATA

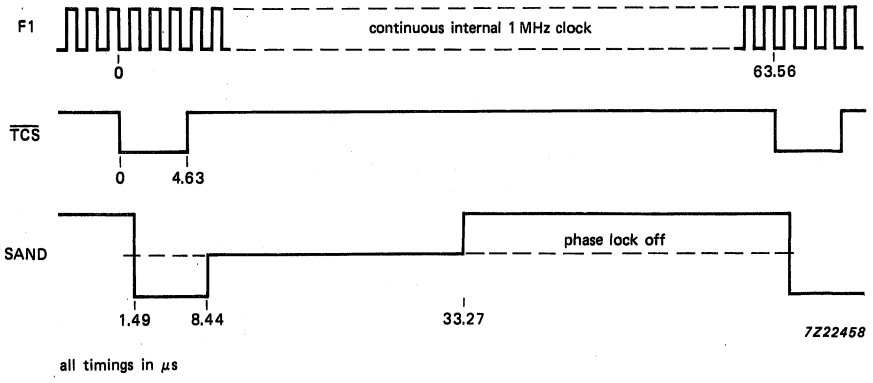
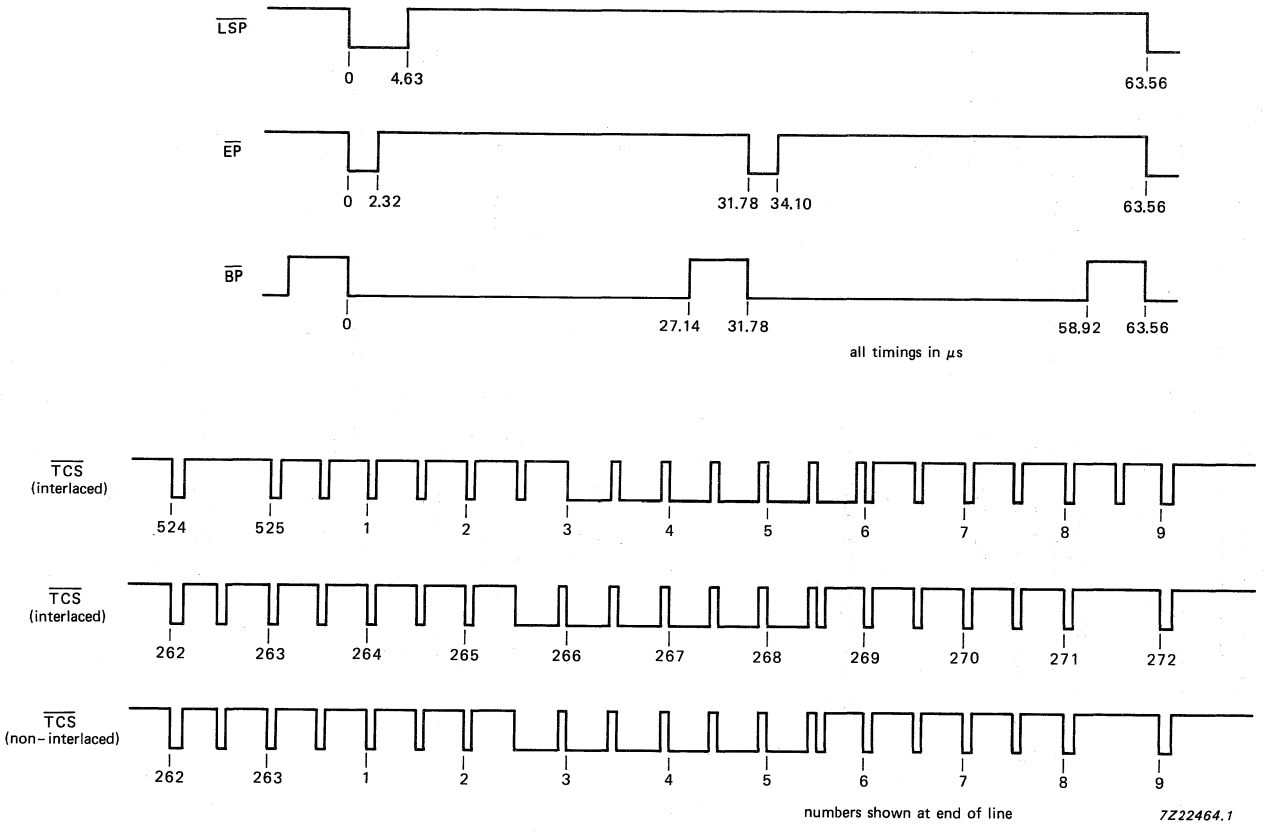


Fig. 5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms (525-line version).

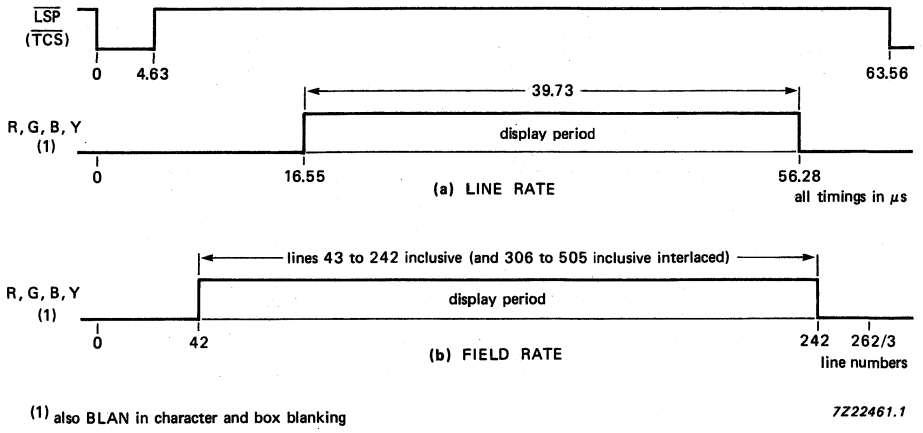


Fig. 7 Display output timing (a) line rate (b) field rate.

DEVELOPMENT DATA

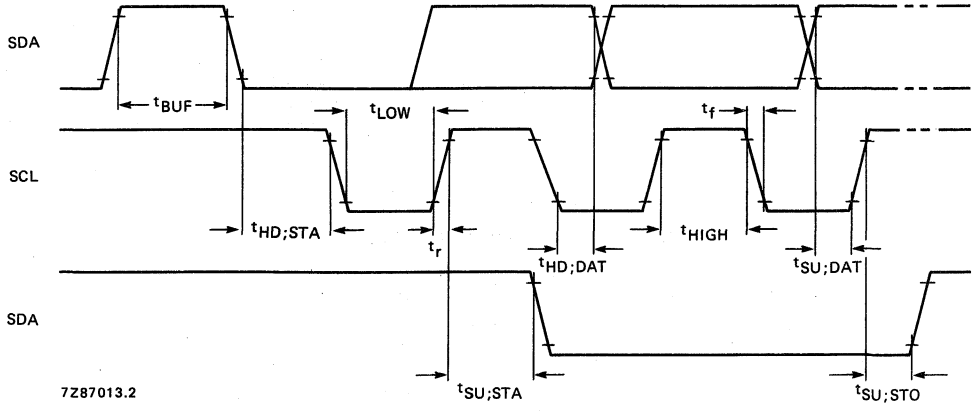


Fig. 8 I²C-bus timing.

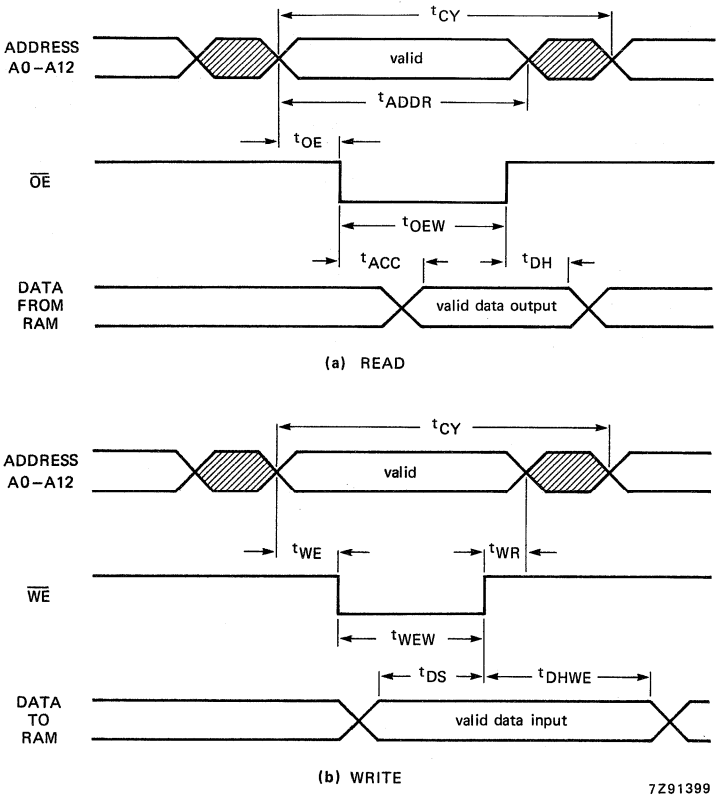


Fig. 9 Memory interface timing (a) read (b) write.

DEVELOPMENT DATA

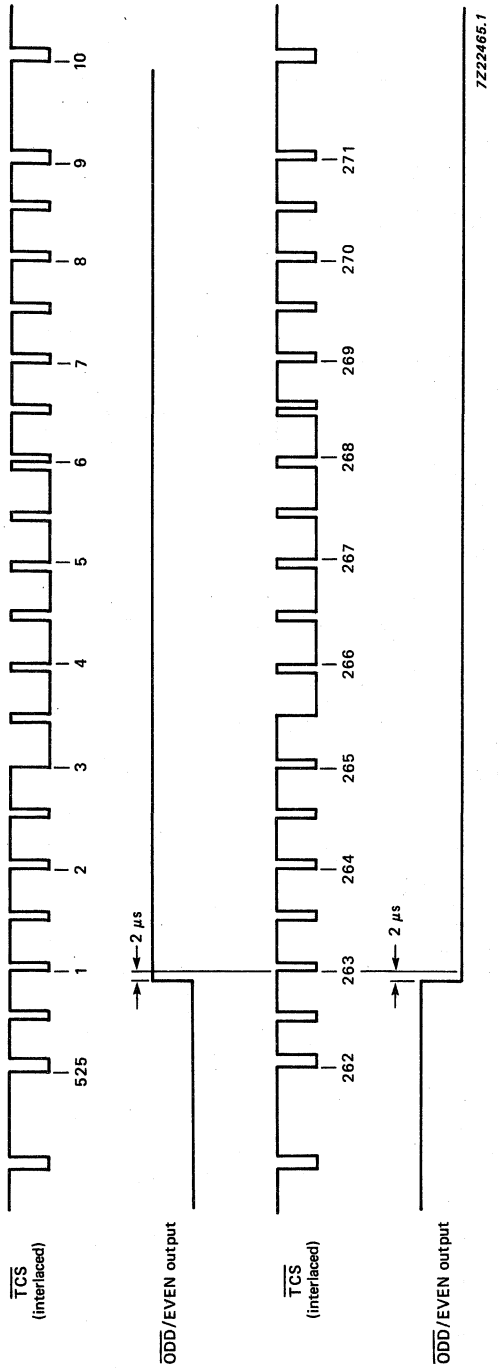


Fig. 10 ODD/EVEN timing diagram.

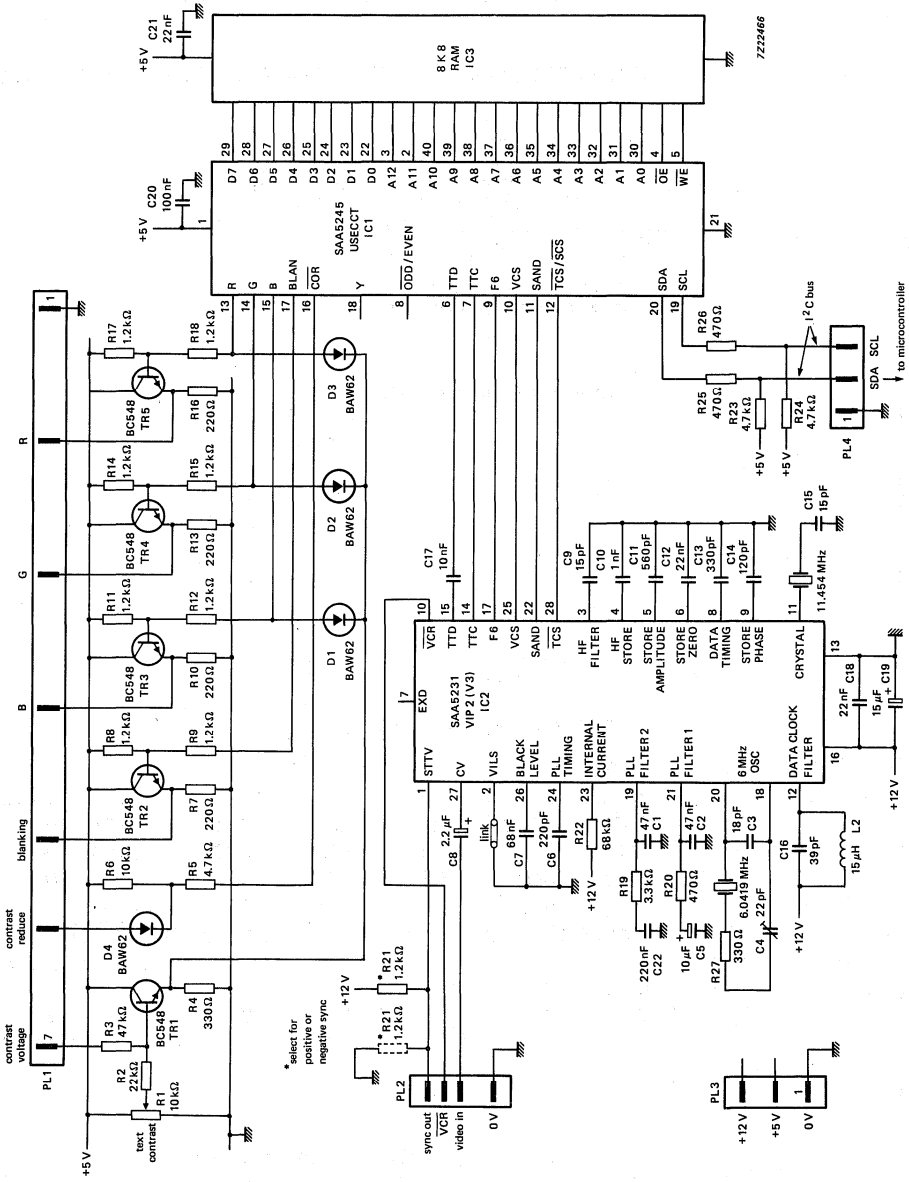


Fig. 11 USECCT based multi-page decoder circuit diagram.

DEVELOPMENT DATA

USECCT page memory organization

The organization of a page memory is shown in Fig. 12. The USECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF USECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

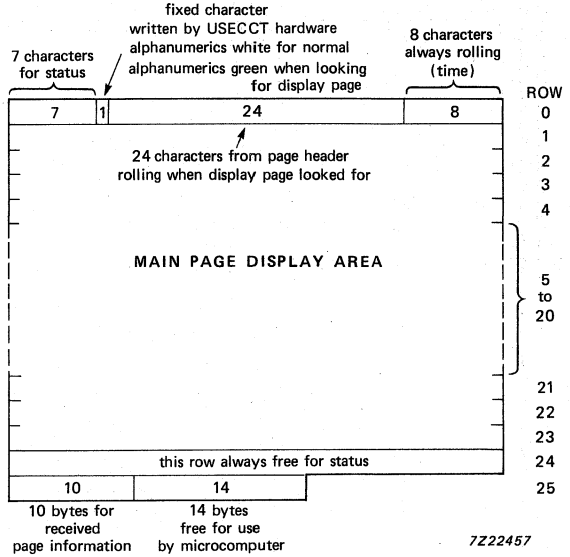


Fig. 12 Page memory organization.

Table 1 Row 25 received control data format

	Column 0	1	2	3	4	5	6	7	8	9
D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	0	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0

Where:

MAG	magazine	MU	minutes units
PU	page units } page number	MT	minutes tens } page sub-code
PT	page tens	HU	hours units
$\overline{\text{PBLF}}$	page being looked for	HT	hours tens
$\overline{\text{FOUND}}$	LOW for page has been found	C4-C14	transmitted control bits
HAM.ER	Hamming error in corresponding byte		

APPLICATION INFORMATION (continued)

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by USECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

USECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 USECCT register map

		D7	D6	D5	D4	D3	D2	D1	D0
Operating mode	R1	TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	R2	–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	R3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	R4	–	–	–	–	–	A2	A1	A0
Display control (normal)	R5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash/subtitle)	R6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	R7	STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	R8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Active row	R9	–	–	–	R4	R3	R2	R1	R0
Active column	R10	–	–	C5	C4	C3	C2	C1	C0
Active data	R11	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

–bit does not exist

DEVELOPMENT DATA

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

Where:

R1 Mode

T0, T1	interlace/non-interlace 262/263 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
$\overline{7+P}$/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation

R2 Page request address

START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition

R3 Page request data — see Table 3

R4 Display chapter — determines which of the 8 pages is displayed

R5, R6 Display control — for normal and newsflash/subtitle

PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text

R8 to R11 — active chapter, row, column and data information written to or read from page memory via the I^2C-bus

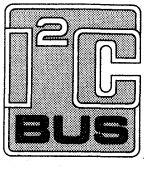
APPLICATION INFORMATION (continued)

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	X	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.



DEVELOPMENT DATA

CHARACTER SETS

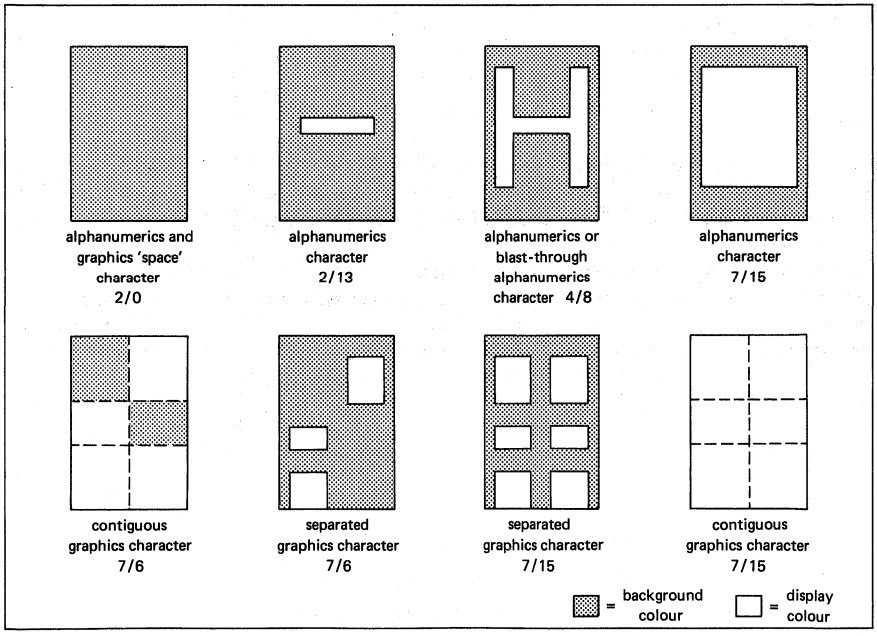
The US teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4.
USECCT automatically decodes transmission bits C12 to C14. Other combinations of C12 to C14 are defaulted to English in SAA5245P/A. With 8-bit decoding the character matrices are shown in Table 5.

Table 4 Selection of national character sets (SAA5245P/A)

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0	0	0	0	1	1
C13	0	0	1	1	0	0
C14	0	1	0	1	0	1

Where:

PHCB page header control bits.



Character bytes are listed as transmitted from b_1 to b_7.

Fig. 13 Character format.

APPLICATION INFORMATION (continued)

Table 5 Character data input decoding (SAA5245A).

BITS b8	0	0	0 or 1		0 or 1		0	0	0		0		1	1	1	1	1	1
b7	0	0	0		0		1	1	1		1		0	0	0	1	1	1
b6	0	0	1		1		0	0	1		1		0	0	1	0	1	1
b5	0	1	0		1		0	1	0		1		0	1	0	1	0	1
b4 b3 b2 b1 \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0 / 0	alpha–numerics black	graphics black																
0 0 0 1 / 1	alpha–numerics red	graphics red																
0 0 1 0 / 2	alpha–numerics green	graphics green																
0 0 1 1 / 3	alpha–numerics yellow	graphics yellow																
0 1 0 0 / 4	alpha–numerics blue	graphics blue																
0 1 0 1 / 5	alpha–numerics magenta	graphics magenta																
0 1 1 0 / 6	alpha–numerics cyan	graphics cyan																
0 1 1 1 / 7	alpha–numerics white **	graphics white																
1 0 0 0 / 8	flash	conceal display																
1 0 0 1 / 9	steady **	contiguous graphics **																
1 0 1 0 / 10	end box **	separated graphics																
1 0 1 1 / 11	start box	ESC *																
1 1 0 0 / 12	normal height **	black background **																
1 1 0 1 / 13	double height	new background																
1 1 1 0 / 14	SO *	hold graphics																
1 1 1 1 / 15	SI *	release graphics **																

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Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
6. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

INTEGRATED VIP AND TELETEXT (IVT)

GENERAL DESCRIPTION

The Integrated VIP and Teletext (IVT) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled Teletext (ECCT) device (SAA5243) with some additional features; existing ECCT software remains compatible.
The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critial or adjustable components are required.

Features

- Complete teletext decoder in a single package
- Single + 5 V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- 4/8 page acquisition system is software compatible with ECCT
- RGB interface to standard colour decoder ICs, push-pull output drive; requires only 2 external resistors
- Data capture performance comparable with SAA5231 (VIP2)
- Software compatibility with ECCT maintained
- Interfaces with 8 K x 8-bit static RAM
- Optional storage of packet 24 in the display memory
- Packet 8/30/2 mapped to a different extension chapter, as an aid for VCR programming applications
- Automatic $\overline{ODD}$/EVEN output control
- Control of display PLL free-run and rolling header via I²C-bus
- Software readable ROM version national option

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current	I_{DD}	–	64	128	mA
Sync amplitude	V_{syn}	0.1	0.3	0.6	V
Video amplitude	V_{vid}	0.7	1	1.4	V
Crystal frequency	f_{XTAL}	–	27	–	MHz
Operating ambient temperature range	T_{amb}	–20	–	+ 70	°C

PACKAGE OUTLINES

SAA5246P : 48-lead DIL; plastic (SOT240).
SAA5246P : 52-lead SDIL; plastic (SOT247).
SAA5246GP : 64-lead QFP; plastic (SOT208).

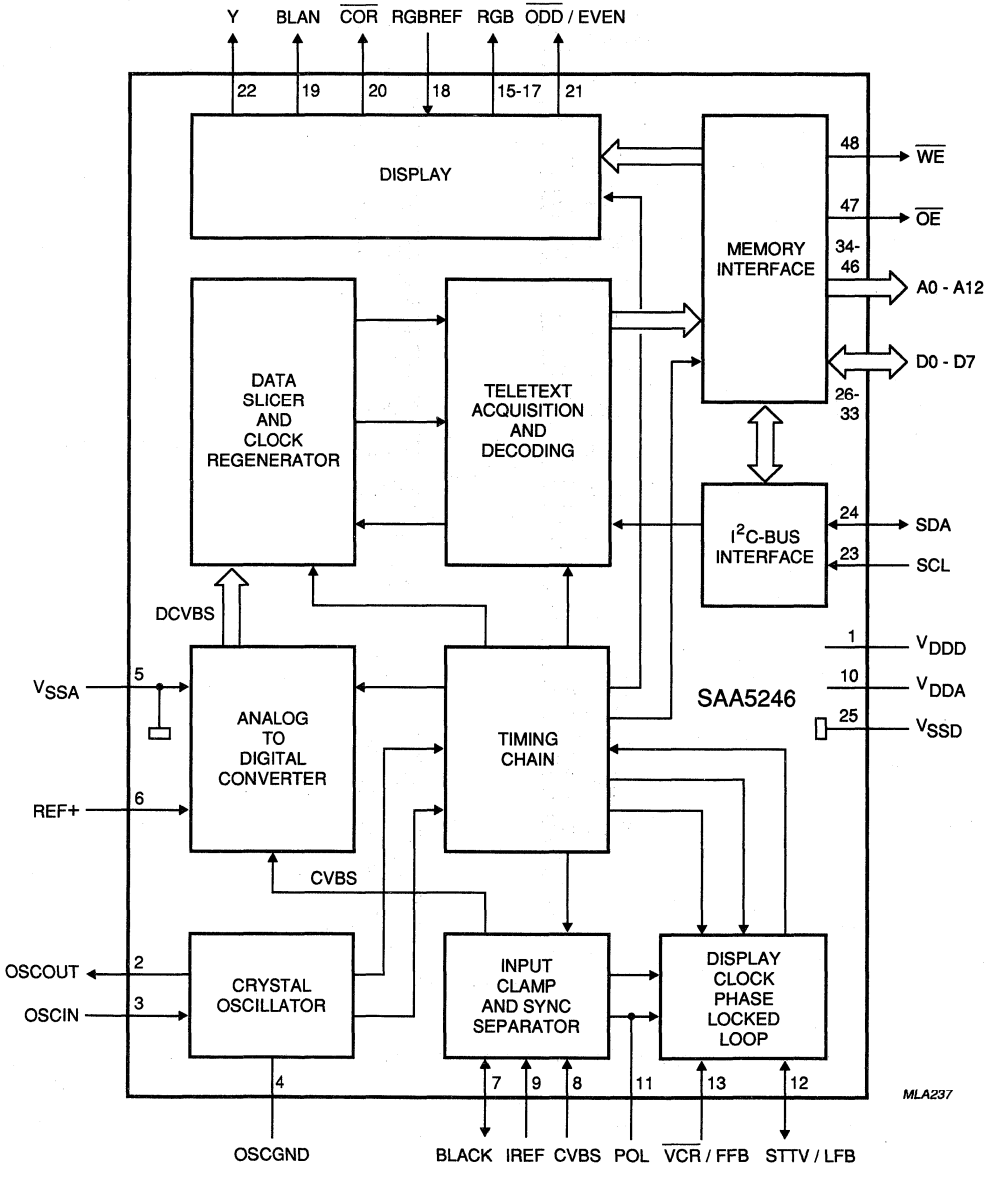


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

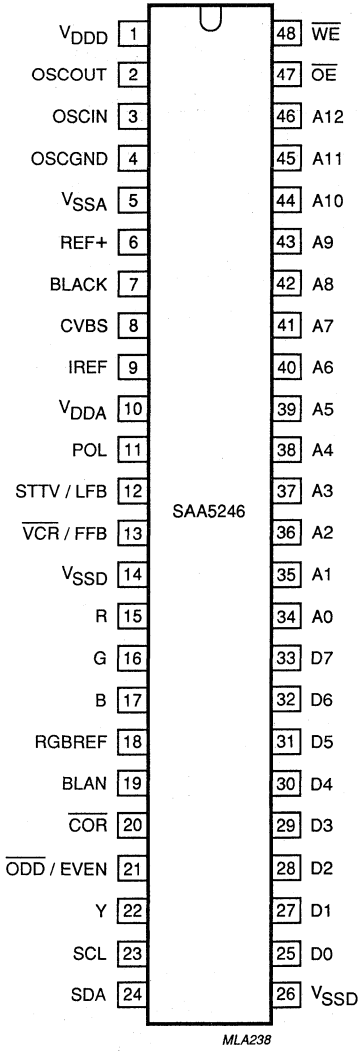


Fig.2(a) Pinning diagram; SOT240 (DIL48).

DEVELOPMENT DATA

PINNING (continued)

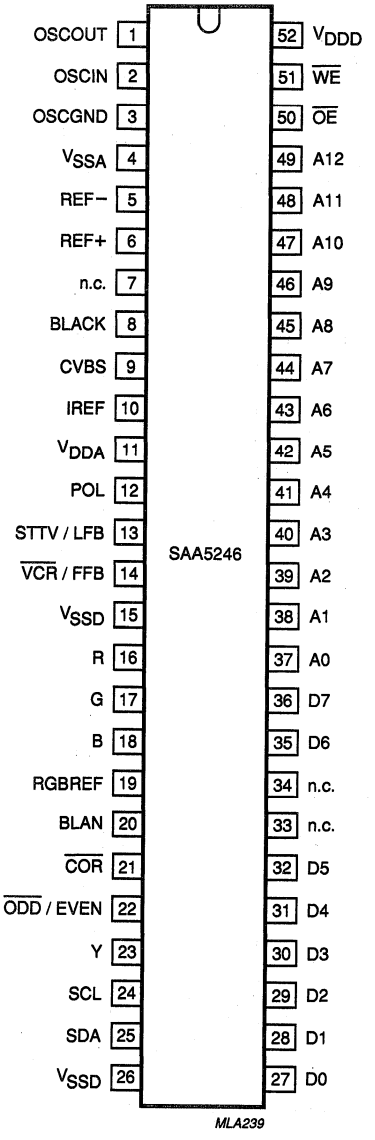


Fig.2(b) Pinning diagram; SOT247 (SDIL52).

DEVELOPMENT DATA

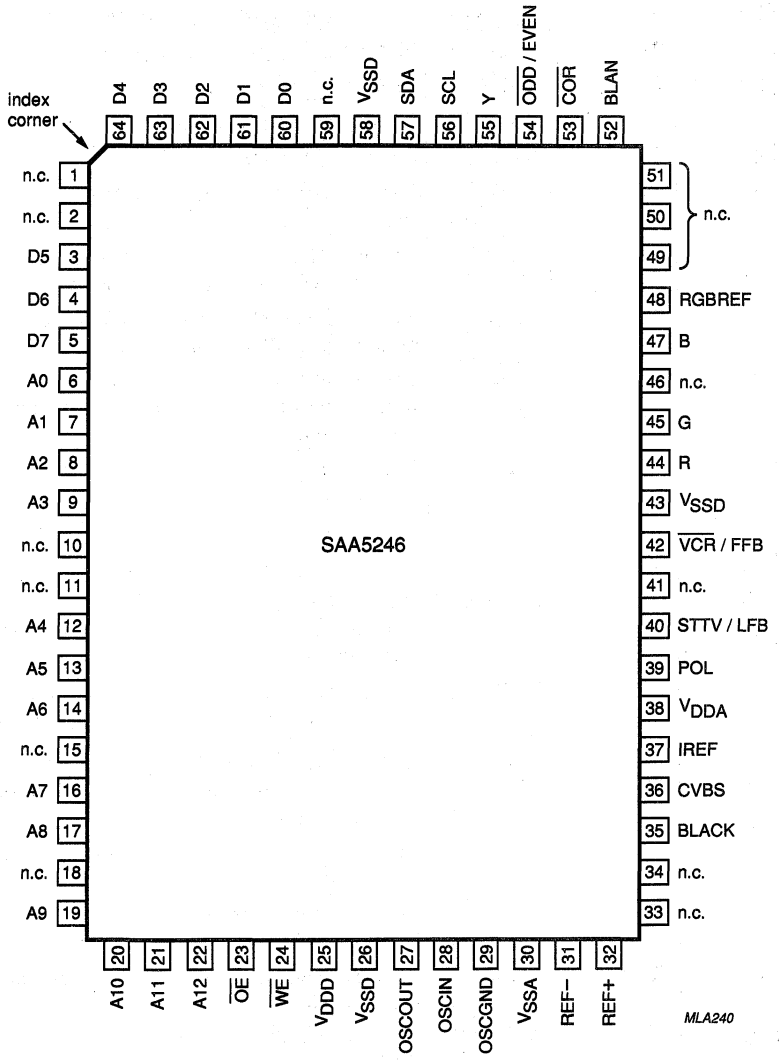


Fig.2(c) Pinning diagram; SOT208 (QFP64).

Pinning description

SOT240	SOT247	SOT208	Mnemonic	Description
1	52	25	V_{DDD}	+ 5 V supply to the digital sections of the device.
2	1	27	OSCOUT	27 MHz crystal oscillator output.
3	2	28	OSCIN	27 MHz crystal oscillator input.
4	3	29	OSCGND	0 V crystal oscillator ground.
5	4	30	V_{SSA}	0 V analog ground.
–	5	31	REF–	Negative reference voltage for the ADC. The pin should be connected to analog 0 V.
6	6	32	REF+	Positive reference voltage for the ADC. The pin should be connected to analog + 5 V.
7	8	35	BLACK	Video black level storage pin, connected to analog ground via a 100 nF capacitor.
8	9	36	CVBS	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
9	10	37	IREF	Reference current input pin, connected to analog ground via a 27 kΩ resistor.
10	11	38	V_{DDA}	+ 5 V supply to the analog sections of the device.
11	12	39	POL	STTV/LFB/FFB polarity selection pin.
12	13	40	STTV/LFB	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
13	14	42	$\overline{VCR}$/FFB	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode).
14	15	43	V_{SSD}	Connected to V_{SSD} for normal operation.
15	16	44	R	Dot rate character output of the RED colour information.
16	17	45	G	Dot rate character output of the GREEN colour information.
17	18	47	B	Dot rate character output of the BLUE colour information.
18	19	48	RGBREF	Input DC voltage to define the output high level on the RGB pins.
19	20	52	BLAN	Dot rate fast blanking output.
20	21	53	$\overline{COR}$	Programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open drain output.

SOT240	SOT247	SOT208	Mnemonic	Description
21	22	54	$\overline{ODD}$/EVEN	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
22	23	55	Y	Dot rate character output of teletext foreground colour information. Open drain output.
23	24	56	SCL	Serial clock input for I^2C-bus. It can still be driven during power-down of the device.
24	25	57	SDA	Serial data port for the I^2C-bus. Open drain output. It can still be driven during power-down of the device.
25	26	26, 58	V_{SSD}	0 V digital ground.
26-33	27-32 35, 36	60-64 3-5	D0-D7	Data lines for the page RAM.
–	7, 33, 34	1, 2, 10 11, 15, 18 33, 34, 41 46, 49-51 59	n.c.	Not connected.
34-46	37-49	6-9 12-14 16, 17 19-22	A0-A12	Address lines for the page RAM.
47	50	23	$\overline{OE}$	Output enable to the page RAM.
48	51	24	$\overline{WE}$	Write enable to the page RAM.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage (all supplies)	V_{DD}	−0.3	−	+ 6.5	V
Input voltage (any input)	V_I	−0.3	−	V_{DD} + 0.5	V
Output voltage (any output)	V_O	−0.3	−	V_{DD} + 0.5	V
Difference between V_{SSD}, V_{SSA} and OSCGND	V_{Sdif}	−0.25	−	+ 0.25	V
Difference between V_{DDD}, V_{DDA} and REF+	V_{Ddif}	−0.25	−	+ 0.25	V
Output current (each output)	I_O	−	−	± 10	mA
DC input or output diode current	I_{IOK}	−	−	± 20	mA
Operating ambient temperature range	T_{amb}	−20	−	+ 70	°C
Storage temperature range	T_{stg}	−30	−	+ 125	°C
Electrostatic handling*	V_{stat}	−2000	−	+ 2000	V

Failure rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

* Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage range		V_{DD}	4.5	5	5.5	V
Supply current		I_{DD}	–	64	120	mA
V_{DDD} supply current		I_{DDD}	–	40	80	mA
V_{DDA} supply current		I_{DDA}	–	16	32	mA
REF+ supply current		I_{REF+}	–	8	16	mA
Inputs						
CVBS						
Sync amplitude		V_{syn}	0.1	0.3	0.6	V
Delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/ trailing edge)		t_{syn}	−150	0	150	ns
Change in sync delay between all black and all white video input at nominal levels		t_{syd}	0	–	25	ns
Video input amplitude (peak-to-peak)		$V_{vid(p-p)}$	0.7	1.0	1.4	V
Display PLL catching range			± 7	–	–	%
Source impedance		Z_{src}	–	–	250	Ω
Input capacitance		C_I	–	–	10	pF
IREF						
Resistor to ground		R_9	–	27	–	kΩ

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (continued)						
POL						
Input voltage LOW		V_{IL}	−0.3	−	+ 0.8	V
Input voltage HIGH		V_{IH}	2	−	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	−	+ 10	μA
Input capacitance		C_I	−	−	10	pF
LFB						
Input voltage LOW		V_{IL}	−0.3	−	+ 0.8	V
Input voltage HIGH		V_{IH}	2	−	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	−	+ 10	μA
Input current	note 1	I_I	−1	−	+ 1	mA
Delay between input video line sync and LFB front edge		t_{lfb}	−	250	−	ns
VCR/FFB						
Input voltage LOW		V_{IL}	−0.3	−	+ 0.8	V
Input voltage HIGH		V_{IH}	2	−	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	−	+ 10	μA
Input current	note 1	I_I	−1	−	+ 1	mA
RGBREF						
Input voltage		V_I	−0.3	−	V_{DDD}	V
Leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	−	+ 10	μA
Input current		I_I	−	−	10	mA
SCL						
Input voltage LOW		V_{IL}	−0.3	−	+ 1.5	V
Input voltage HIGH		V_{IH}	3	−	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	−	+ 10	μA
Clock frequency		f_{scl}	0	−	100	kHz
Input rise and fall time	10% - 90%	t_r, t_f	−	−	2	μs
Input capacitance		C_I	−	−	10	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Input/outputs						
Crystal oscillator (OSCIN; OSCOUT)						
Crystal frequency		f_{XTAL}	–	27	–	MHz
Internal bias resistance (between OSCIN and OSCOUT)		$R_{x\,bias}$	40	–	1500	kΩ
Small signal voltage gain		G_v	3.5	–	–	–
Mutual conductance	f = 100 kHz	G_m	1.5	–	–	mA/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
BLACK						
Storage capacitor to ground		C_{blk}	–	100	–	nF
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–10	–	+ 10	μA
D0 to D7						
Input voltage LOW		V_{IL}	–0.3	–	+ 0.8	V
Input voltage HIGH		V_{IH}	2	–	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
Output voltage LOW	I_{OL} = + 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = –0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Load capacitance		C_L	–	–	120	pF
Output rise and fall times	0.6 to 2.2 V	t_r, t_f	–	–	50	ns
SDA						
Input voltage LOW		V_{IL}	–0.3	–	+ 1.5	V
Input voltage HIGH		V_{IH}	3	–	V_{DDD}+ 0.5	V
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	–10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
Input rise and fall time	10% - 90%	t_r, t_f	–	–	2	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/outputs (continued)						
SDA (continued)						
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.5	V
Output fall time	3 V to 1 V	t_f	–	–	200	ns
Load capacitance		C_L	–	–	400	pF
Outputs						
STTV						
Gain of STTV relative to video input		G_{stt}	0.9	1	1.1	
TCS amplitude		V_{tcs}	0.2	0.3	0.45	V
DC shift between TCS output and nominal video output		V_{DCs}	–	–	0.15	V
Output drive		I_O	–	–	3	mA
Load capacitance		C_L	–	–	100	pF
A0 to A12						
Output voltage LOW	I_{OL} = + 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = –0.2 mA	V_{OH}	2.4	–	V_{DDD}	V
Load capacitance		C_L	–	–	120	pF
Output rise and fall times	0.6 to 2.2 V	t_r, t_f	–	–	50	ns
$\overline{OE}$ and $\overline{WE}$						
Output voltage LOW	I_{OL} = + 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = –0.2 mA	V_{OH}	2.4	–	V_{DDD}	V
Load capacitance		C_L	–	–	120	pF
Output rise and fall times	0.6 to 2.2 V	t_r, t_f	–	–	50	ns
R, G and B						
Output voltage LOW		V_{OL}	0	–	–	V
Output voltage HIGH	I_{OH} = = 2 mA; RGBREF $\leqslant$ V_{DD}–1.5 V	V_{OH}	–10%	RGBREF	+ 10%	V
Output impedance		$\|Z_o\|$	–	–	200	Ω
Load capacitance		C_L	–	–	50	pF
Output rise and fall times	10% - 90%	t_r, t_f	–	–	20	ns

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
BLAN						
Output voltage LOW		V_{OL}	0	–	0.4	V
Output voltage HIGH		V_{OH}	1.1	–	2.8	V
Load capacitance		C_L	–	–	50	pF
Output rise time	10% - 90%	t_r	–	–	20	ns
Output fall time	10% - 90%	t_f	–	–	20	ns
$\overline{ODD}$/EVEN						
Output voltage LOW	I_{OL} = + 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = –0.2 mA	V_{OH}	V_{DDD}–0.4	–	V_{DD}	V
Load capacitance		C_L	–	–	120	pF
Output rise and fall times	0.6 to 2.2 V	t_r, t_f	–	–	50	ns
$\overline{COR}$ and Y (open drain)						
Pull-up voltage at pin		V_{OH}	–	–	V_{DDD}	V
Output voltage LOW	I_{OL} = + 2 mA	V_{OL}	0	–	0.4	V
	I_{OL} = + 5 mA	V_{OL}	0	–	1	V
Load capacitance		C_L	–	–	25	pF
Output fall time	load resistor of 1.2 kΩ to V_{DDD}; measured between V_{DDD} – 0.5 and 1.5 V	t_f	–	–	50	ns
Output leakage current	V_I = 0 to V_{DD}	I_{LO}	–10	–	+ 10	μA
Skew delay between display outputs R, G, B, $\overline{COR}$, Y, BLAN		T_{SK}	–	–	20	ns
Timing						
I²C-bus						
Clock LOW period		t_{LOW}	4	–	–	μs
Clock HIGH period		t_{HIGH}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	170	–	–	ns
Set-up time from clock HIGH to STOP		$t_{SU;STO}$	4	–	–	μs
START set-up time following a STOP		t_{BUF}	4	–	–	μs
START hold time		$t_{HD;STA}$	4	–	–	μs
START set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Timing (continued)						
Memory interface						
Cycle time		t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW		t_{OE}	55	–	–	ns
Address active time		t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse width read		t_{rOEW}	295	–	–	ns
$\overline{OE}$ pulse width write		t_{wOEW}	100	–	–	ns
Access time from address data valid		t_{ACC}	–	–	150	ns
Data hold time from $\overline{OE}$ HIGH or address change		t_{DH}	0	–	–	ns
Data enable from $\overline{WE}$ LOW		t_{DE}	60	–	–	ns
$\overline{WE}$ pulse width		t_{WEW}	100	–	–	ns
Data set-up time to $\overline{WE}$ HIGH		t_{DS}	60	–	–	ns
Data hold time from $\overline{WE}$ HIGH		t_{DHWE}	20	–	–	ns
Write recovery time		t_{WR}	20	–	–	ns

Note to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.

DEVELOPMENT DATA

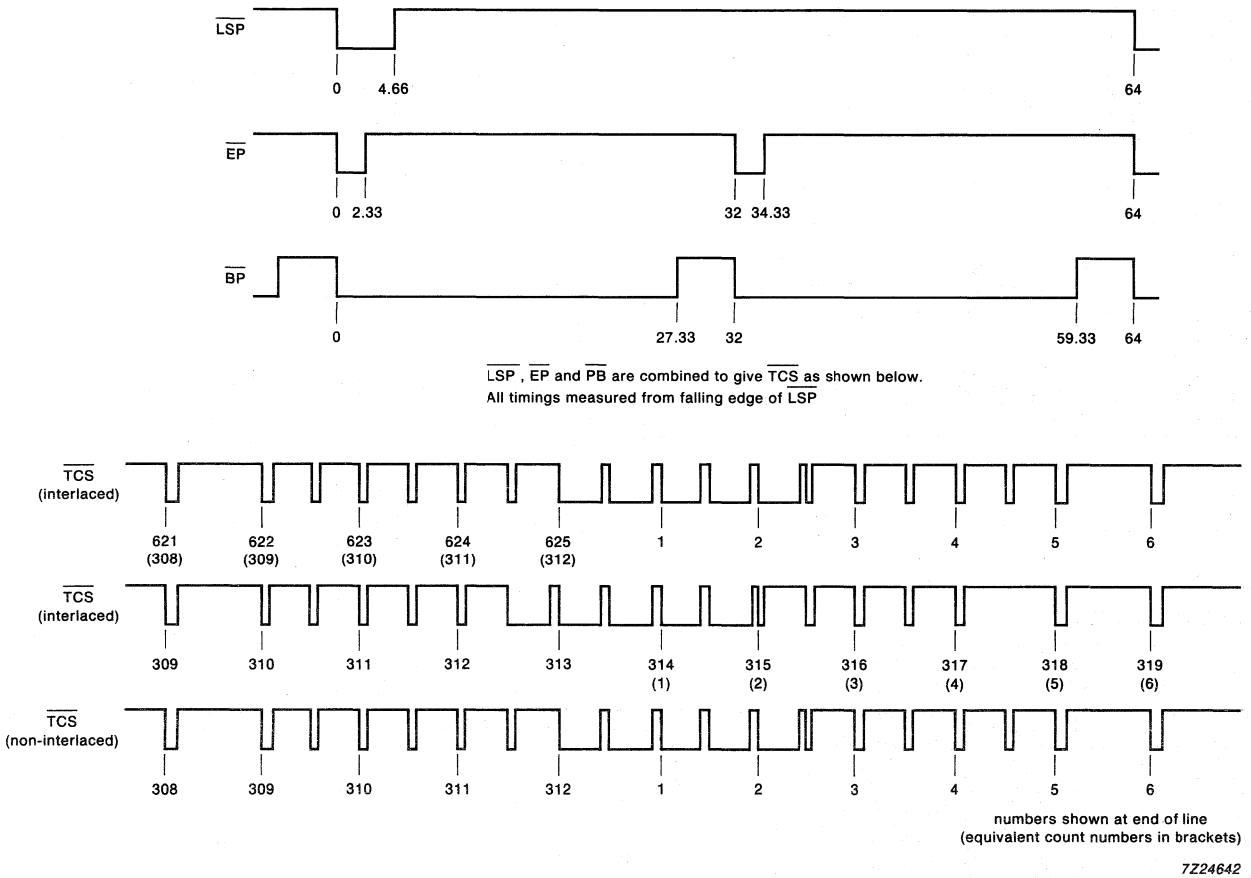


Fig.3 Composite sync waveforms.

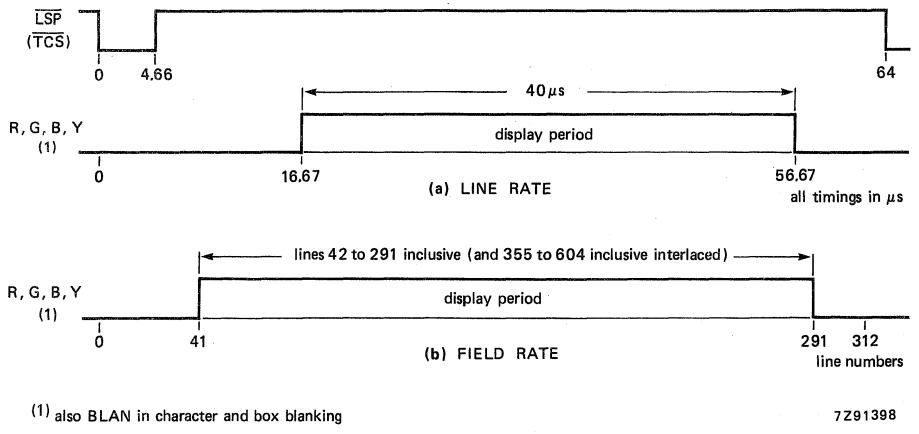


Fig.4 Display output timing (a) line rate (b) field rate.

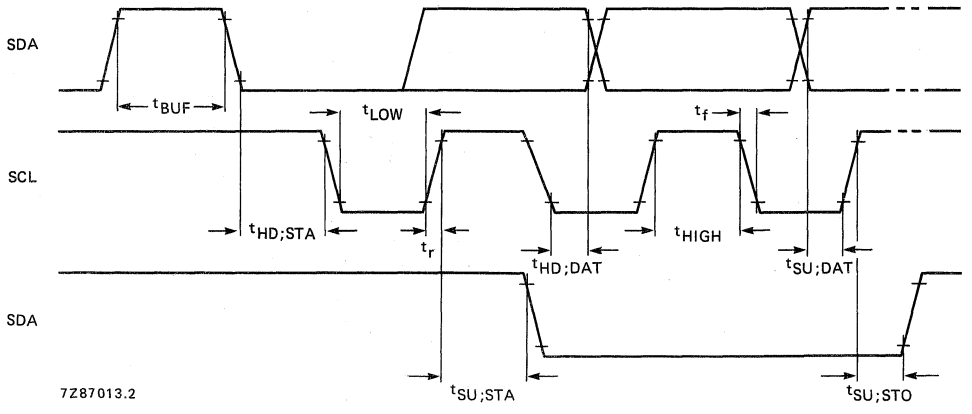
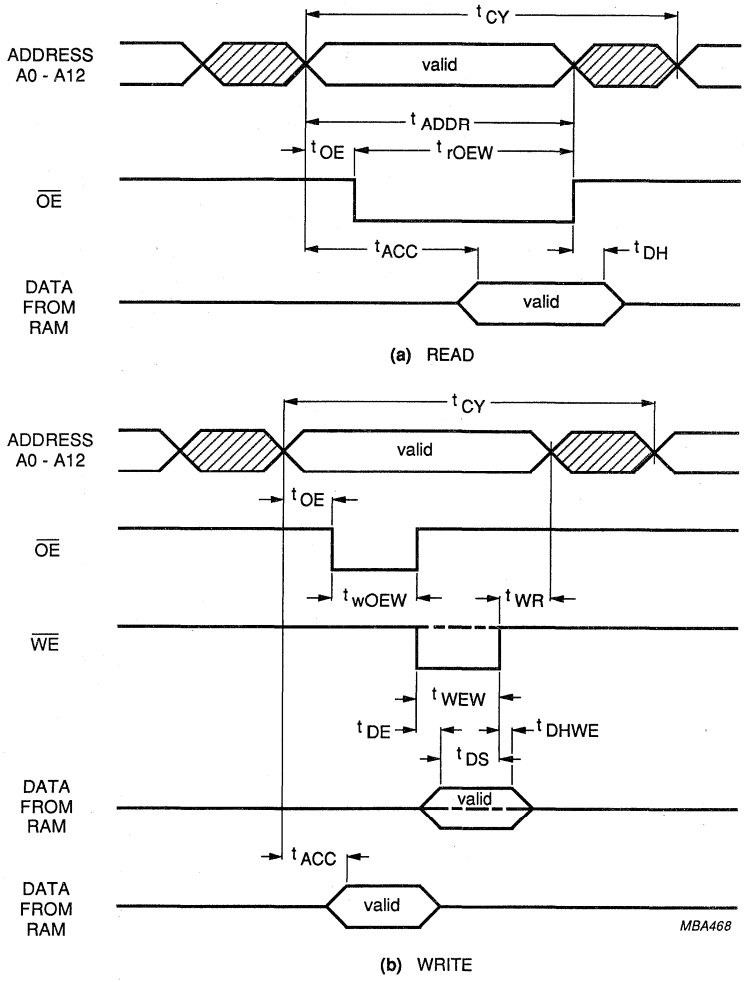


Fig.5 I²C-bus timing.



— · — · — Level during flicker stopped cycle.

Fig.6 Memory interface timing (a) read (b) write.

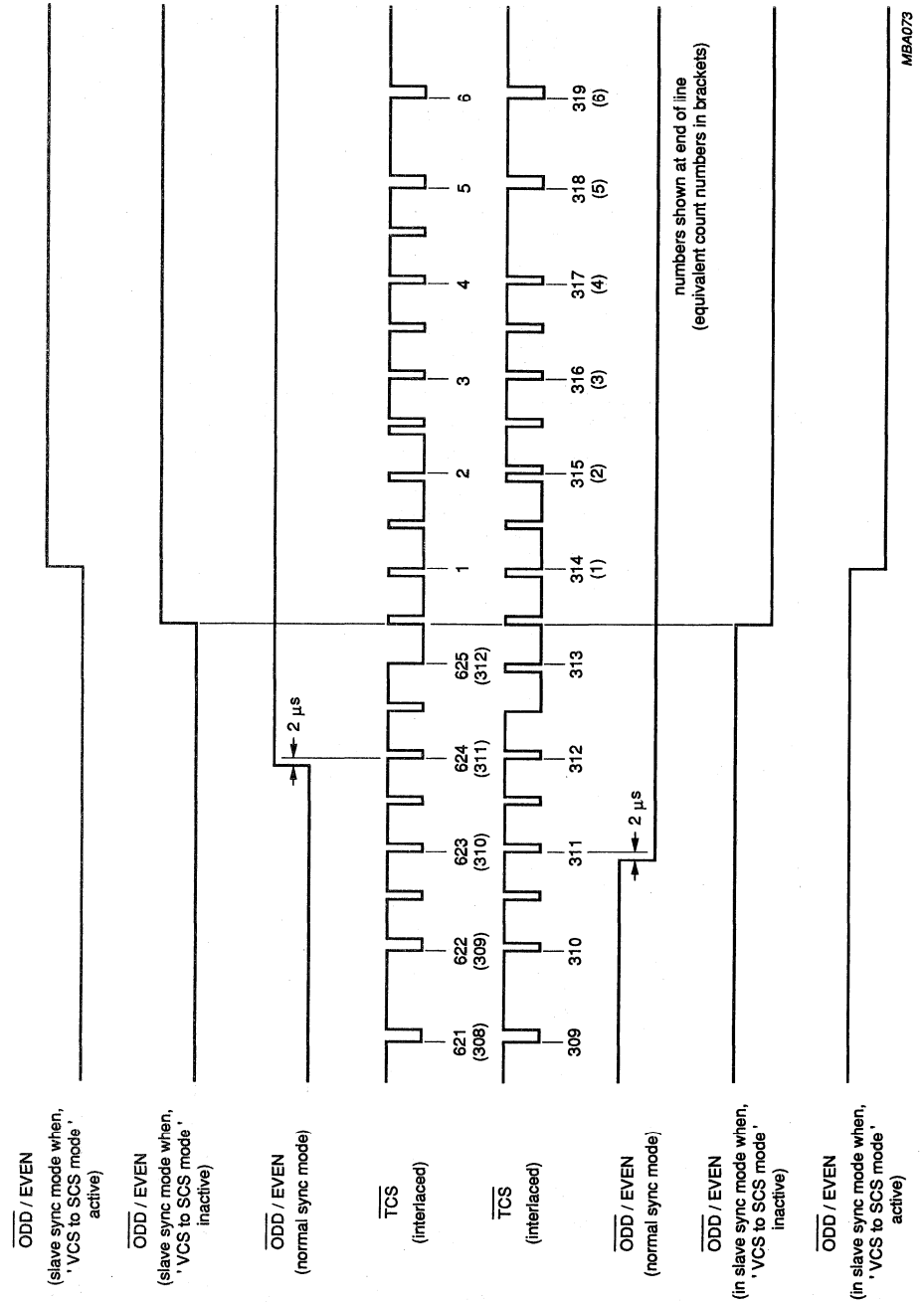
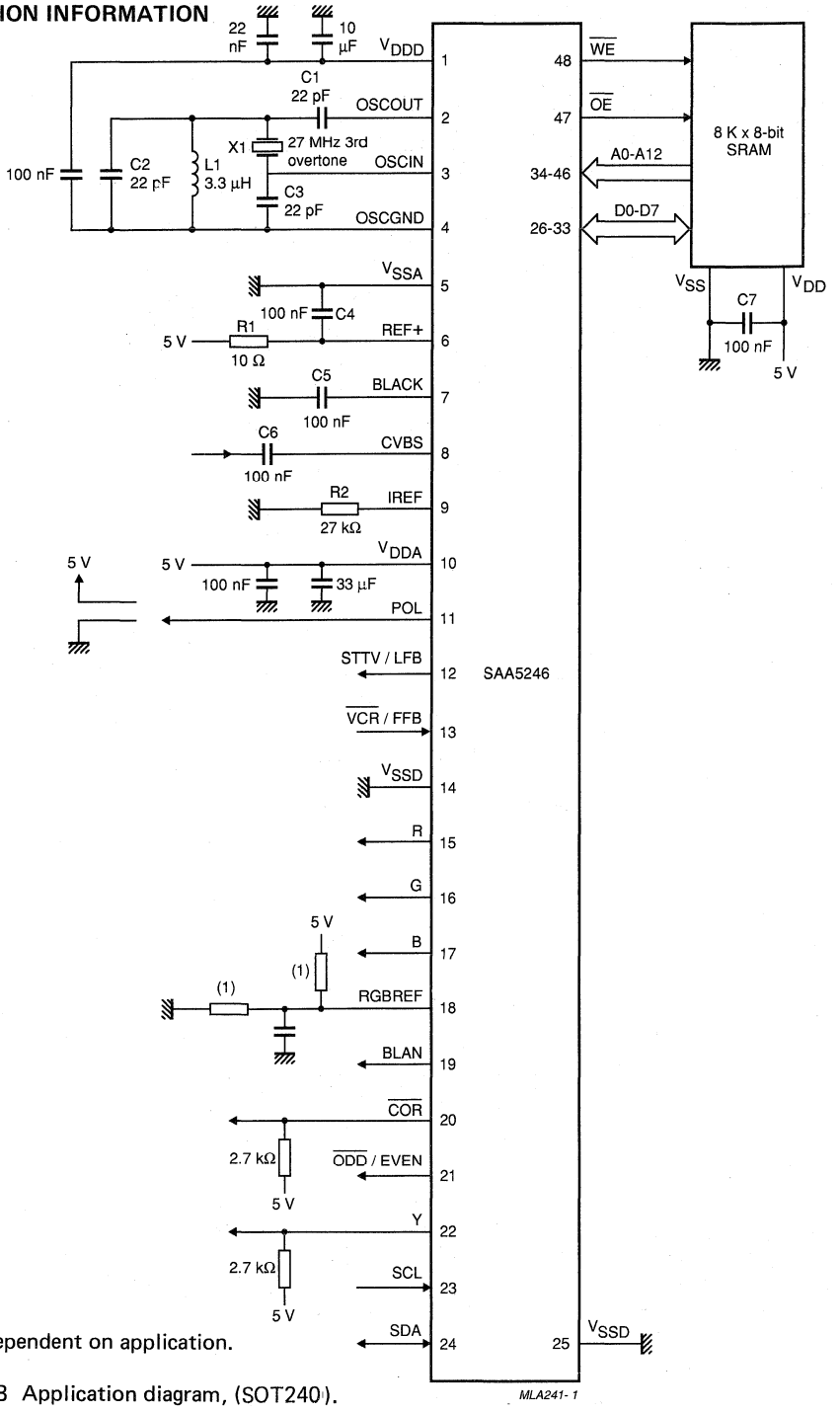


Fig.7 ODD/EVEN timing.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.8 Application diagram, (SOT240).

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

IVT page memory organization

The organization of the page memory is illustrated by Fig.9. The IVT provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

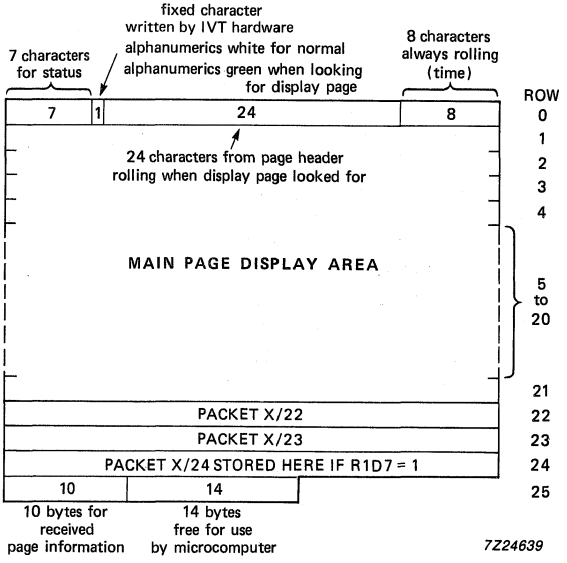


Fig.9 Basic page memory organization.

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.10.

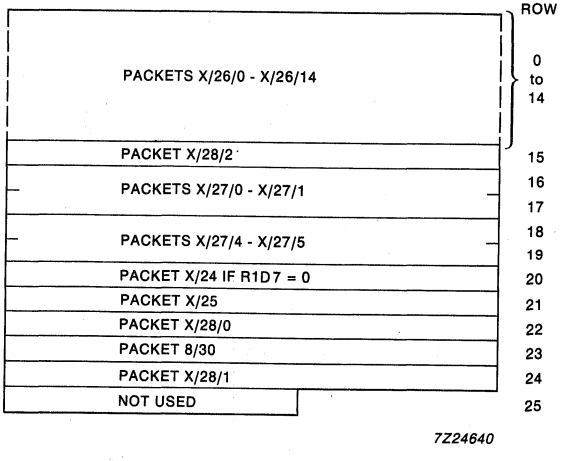


Fig.10 Organization of the extension memory.

Notes to Fig.10

1. Packet 8/30 maps into the ECCT memory as follows:
   8/30/0 and 8/30/1 to chapter 4 row 23
   8/30/2 and 8/30/3 to chapter 5 row 23
   8/30/4 to 8/30/15 to chapter 6 row 23
2. On first reception of a page or if C4 = 1 (in page header), extension memory rows 0 to 22 and 24 are cleared to space code.

Table 1 Row 24 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
	Column 0	1	2	3	4	5	6	7	8	9

DEVELOPMENT DATA

Where:

MAG magazine
PU page units } page number
PT page tens
PBLF page being looked for
$\overline{\text{FOUND}}$ LOW for page has been found
HAM.ER hamming error in corresponding byte
MU minutes units
MT minutes tens } page sub-code
HU hours units
HT hours tens
C4-C14 transmitted control bits

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by IVT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

APPLICATION INFORMATION (continued)

Register maps

IVT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 IVT register map

D7	D6	D5	D4	D3	D2	D1	D0		
X24 POS.	FREE RUN PLL	AUTO ODD-EVEN	DISABLE HDR ROLL	–	DISABLE ODD-EVEN	–	$\overline{R11}$/ R11B SELECT	R0	Advanced control
VCS TO SCS	$\overline{7+P}$/ 8 BIT	$\overline{ACQ.}$ ON/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CIRCUIT A1	ACQ. CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS $\overline{ROW}$ BTM/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data
$\overline{625}$/ 525 SYNC	ROM VER R4*	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY	R11B	Device status

Notes to Table 2

1. '–' these bits are inactive and must be written to 0 for future compatibility.
2. The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C-bus transmission byte.
3. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
4. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but all pages are on hold.
5. TB must be set to logic 0 for normal operation.

* Available from M4 version onwards.

Where:

R0 Advanced control

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B.
DISABLE $\overline{ODD}$/EVEN	Forces $\overline{ODD}$/EVEN output LOW when logic 1.
DISABLE HDR ROLL	Disables green rolling header and time.
AUTO $\overline{ODD}$/EVEN	When set forces $\overline{ODD}$/EVEN low if any TV picture displayed, if DISABLE $\overline{ODD}$/EVEN = 0.
FREE RUN PLL	Will force the PLL to free run in all conditions.
X24 POS	Automatic display of FASTEXT prompt row when logic 1.

R1 Mode

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4).
TCS ON	Text composite sync or direct sync select.
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode.
$\overline{7\ P/8\ BIT}$	7 bits with parity checking or 8-bit mode.
VCS to SCS	When logic 1 enables display of messages with 60 Hz input signal.

R2 Page request address

START COLUMN	Point to start column for page request data (see Table 3).
ACQ CCT	Selects one of four acquisition circuits.
BANK SELECT	Selects bank of four pages being addressed for acquisition.

R3 Page request data — See Table 3.

R4 Display chapter determines which of the 8 pages is displayed.

R5, R6 Display control for normal and newsflash/subtitle

PON	Picture on.
TEXT	Text on.
COR	Contrast reduction on.
BKGND	Background colour on.

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)	Boxing function allowed on row 0 (row 1-23, 24).
STATUS ROW $\overline{BTM}$/TOP	Row 25 displayed above or below main text.
R8 to R11	Active chapter, row, column and data information written to or read from page memory via the I^2C-bus.

R11B Device status

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1.
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1.
ROM VER	Identifies which ROM code is present.
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

DEVELOPMENT DATA

APPLICATION INFORMATION

Register maps (continued)

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
5. Columns auto-increment on successive I^2C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	Result
0	0	Interlaced 312.5/312.5 lines
0	1	Non-interlaced 312/313 lines*
1	0	Non-interlaced 312/312 lines*
1	1	SCS mode (scan composite sync)

* Reverts to interlaced mode if a newsflash or subtitle is being displayed.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.11.

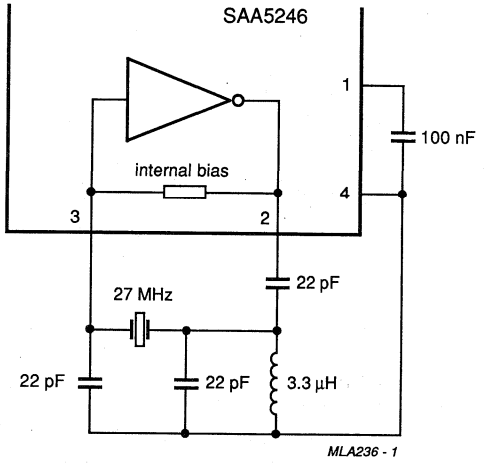


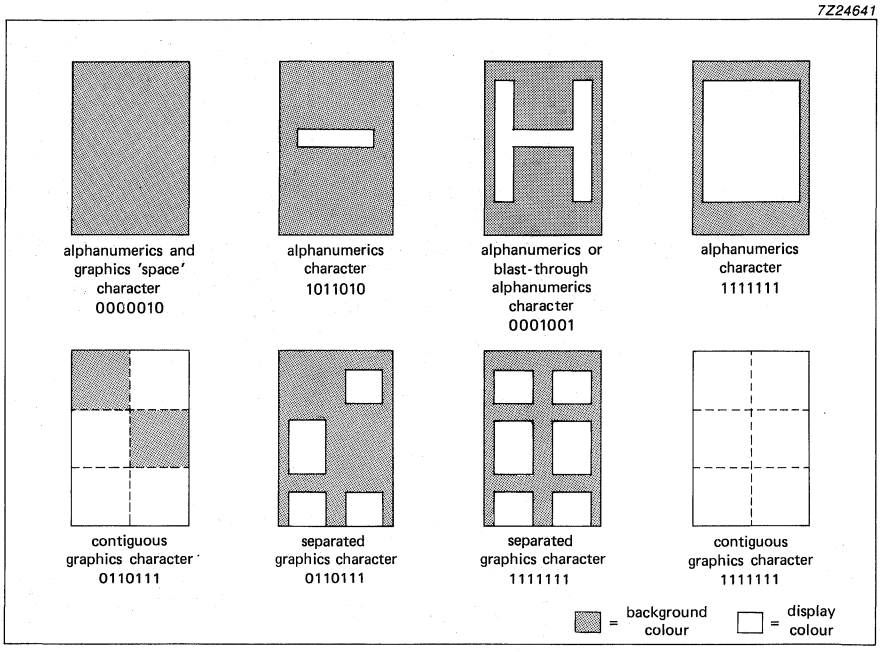
Fig.11 Crystal oscillator application diagram.

parameter	conditions	symbol	min.	typ.	max.	unit
CRYSTAL (27 MHz, 3rd overtone)						
Series capacitance		C1	–	1.7	–	fF
Parallel capacitance		C0	–	5.2	–	pF
Resonant resistance		Rr	–	–	50	Ω
Series resistance		R1	–	20	–	Ω
Ageing			–	± 5	–	10^{-6}/yr
Adjustment tolerance			–	± 40	–	10^{-6}
Drift			–	± 40	–	10^{-6}
Load capacitance		C_L	–	20	–	pF

DEVELOPMENT DATA

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character set differs only in the 13 national option characters as indicated in Table 7 with reference to their table position in the basic character matrix illustrated in Table 6. The IVT1.1 automatically decodes transmission bits C12 to C14.
Table 5 illustrates the character matrixes.



Character bytes are listed as transmitted from b1 to b7.

Fig.12 Character format.

Table 5a Character data input decoding (SAA5246P/E)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	1	1	1	1
b_7	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1
b_6	0	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1
b_5	0	1	0	0	1	0	1	0	1	1	0	1	0	0	1	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	ESC *															
1 1 0 0	12	** normal height	black ** back–ground															
1 1 0 1	13	double height	new back–ground															
1 1 1 0	14	SO *	hold graphics															
1 1 1 1	15	SI *	release ** graphics															

7Z96828.4

Version number 00000 (see Register 11B).

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

DEVELOPMENT DATA

Table 5b Character data input decoding, East European languages (SAA5246P/H)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	1	1	1	1	1		1		0	0	1	1	1	1
b_6	0	0	1	1	0	0	1	1	1		1		0	0	0	0	1	1
b_5	0	1	0	1	0	1	0	0	1		0		0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓ / row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha–numerics black	graphics black															
0 0 0 1	1	alpha–numerics red	graphics red															
0 0 1 0	2	alpha–numerics green	graphics green															
0 0 1 1	3	alpha–numerics yellow	graphics yellow															
0 1 0 0	4	alpha–numerics blue	graphics blue															
0 1 0 1	5	alpha–numerics magenta	graphics magenta															
0 1 1 0	6	alpha–numerics cyan	graphics cyan															
0 1 1 1	7	alpha–** numerics white	graphics white															
1 0 0 0	8	flash	conceal display															
1 0 0 1	9	** steady	** contiguous graphics															
1 0 1 0	10	** end box	separated graphics															
1 0 1 1	11	start box	* ESC															
1 1 0 0	12	** normal height	black ** background															
1 1 0 1	13	double height	new background															
1 1 1 0	14	* SO	hold graphics															
1 1 1 1	15	* SI	** release graphics															

7Z22497.5

Version number 00001 (see Register 11B).

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins.

Table 5c Character data input decoding, West European and Turkish languages (SAA5246P/T)

BITS b_8	0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b_7	0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b_6	0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b_5	0	1	0	1	1	1	0	1	0		1		0	1	0	1	0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	row 0 alpha - numerics black	graphics black																
0 0 0 1	1 alpha - numerics red	graphics red																
0 0 1 0	2 alpha - numerics green	graphics green																
0 0 1 1	3 alpha - numerics yellow	graphics yellow																
0 1 0 0	4 alpha - numerics blue	graphics blue																
0 1 0 1	5 alpha - numerics magenta	graphics magenta																
0 1 1 0	6 alpha - numerics cyan	graphics cyan																
0 1 1 1	7 alpha - numerics white **	graphics white																
1 0 0 0	8 flash	conceal display																
1 0 0 1	9 steady **	contiguous graphics **																
1 0 1 0	10 end box **	separated graphics																
1 0 1 1	11 start box	ESC *																
1 1 0 0	12 normal height **	black back - ground **																
1 1 0 1	13 double height	new back - ground																
1 1 1 0	14 SO *	hold graphics																
1 1 1 1	15 SI *	release graphics **																

MBA431

Version number 00010 (see Register 11B).

* These control characters are reserved for compatibility with other data codes.

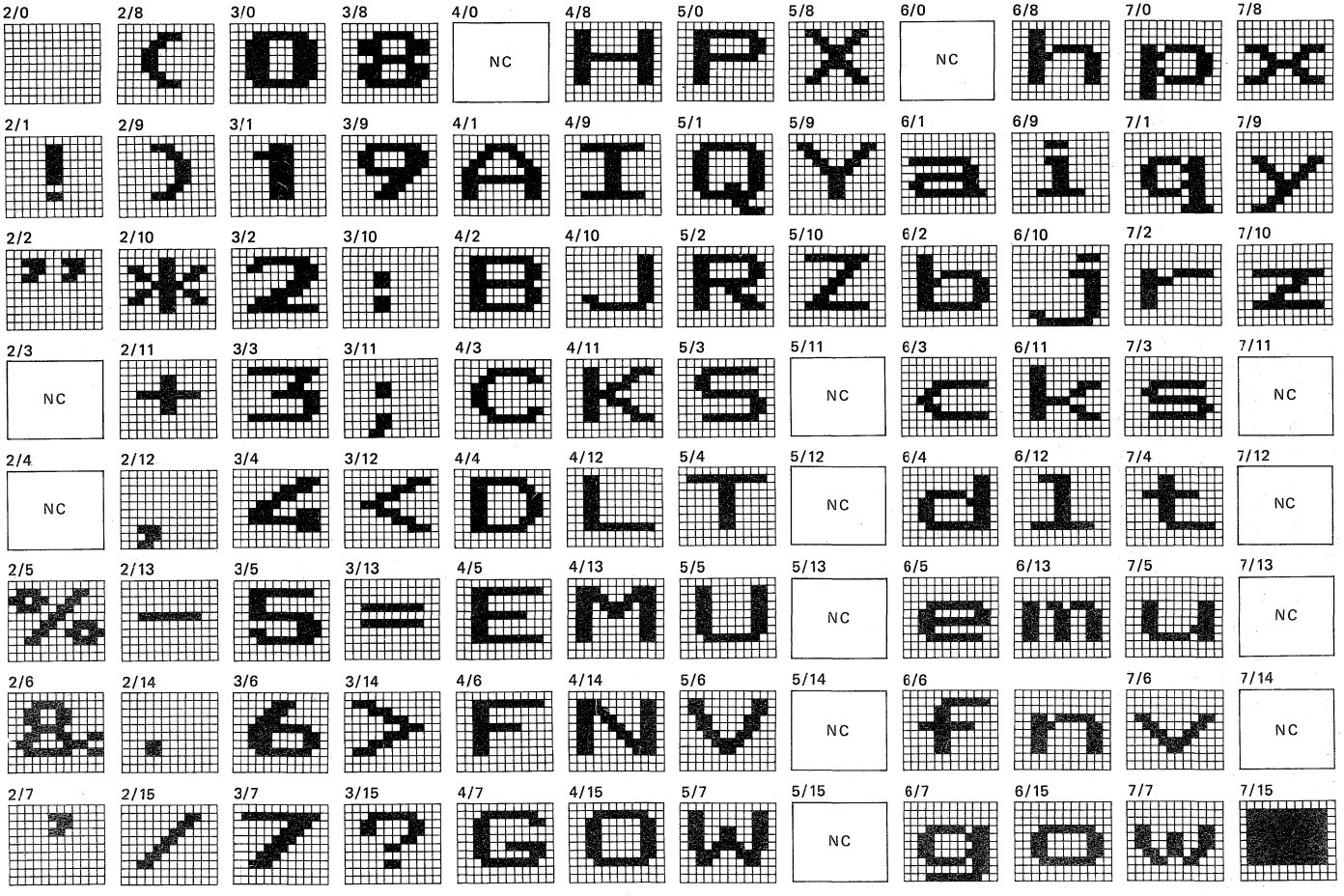
** These control characters are presumed before each row begins.

DEVELOPMENT DATA

Notes to Table 5

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Columns may be referred to by column and row, for example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □.
5. The SAA5246 national option characters are illustrated by Table 7.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5.
7. With bit 8 = 0, national characters will be decoded according to the setting of control bits C12 to C14 (see Table 7).
8. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 6 SAA5246 basic character matrix



7Z91405

Where: NC = national option character position.

Table 7a SAA5246P/E/M2 national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Table 7b SAA5246P/H national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
POLISH	0	0	0	#	ń	ą	Ż	Ś	Ł	ć	ó	ę	ż	ś	ł	ź
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	½	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECHOSLOVAK	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

7Z22658.1

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to German.

Table 7c SAA5246P/T national option character set

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	Ţ	ğ	İ	Ş	ö	Ç	ü	Ğ	ı	ş	ö	ç	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

MBA430

(1) Where PHCB are the Page Header Control bits. Other combinations of PHCB default to English.

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

INTERFACE FOR DATA ACQUISITION AND CONTROL (for multi-standard teletext systems)

GENERAL DESCRIPTION

The SAA5250 is a CMOS Interface for Data Acquisition and Control (CIDAC) designed for use in conjunction with the Video Input Processor (SAA5230) in a multi-standard teletext decoder. The device retrieves data from a user selected channel (channel demultiplexer), as well as providing control signals and consecutive addressing space necessary to drive a 2 K bytes buffer memory.

The system operates in accordance with the following transmission standards:

- French Didon Antiope specification D2 A4-2 (DIDON)
- North American Broadcast Teletext specification (NABTS)
- U.K. teletext (CEEFAX)

Features

- 7,5 MHz maximum conversion rate
- Three prefixes; DIDON, NABTS and U.K. teletext (CEEFAX)
- Mode without prefix
- Internal calculation of the validation (VAL) and colour burst blanking (CBB) signals, if programmed
- Programmable framing code and channel numbers
- Error parity calculation or not (odd parity)
- Hamming processing of the prefix byte
- Full channel or VBI reception
- Slow/fast mode (detection of page flags or not)
- Maximum/default format up to 63 bytes
- Addressing space of 2 K bytes of the static memory
- Multiplexed address/data information is compatible with Motorola or Intel microcontrollers
- CIDAC is 'MOTEL' compatible

PACKAGE OUTLINES

SAA5250P: 40-lead DIL; plastic (SOT129).
SAA5250T: 40-lead mini-pack; plastic (VSO40; SOT158).

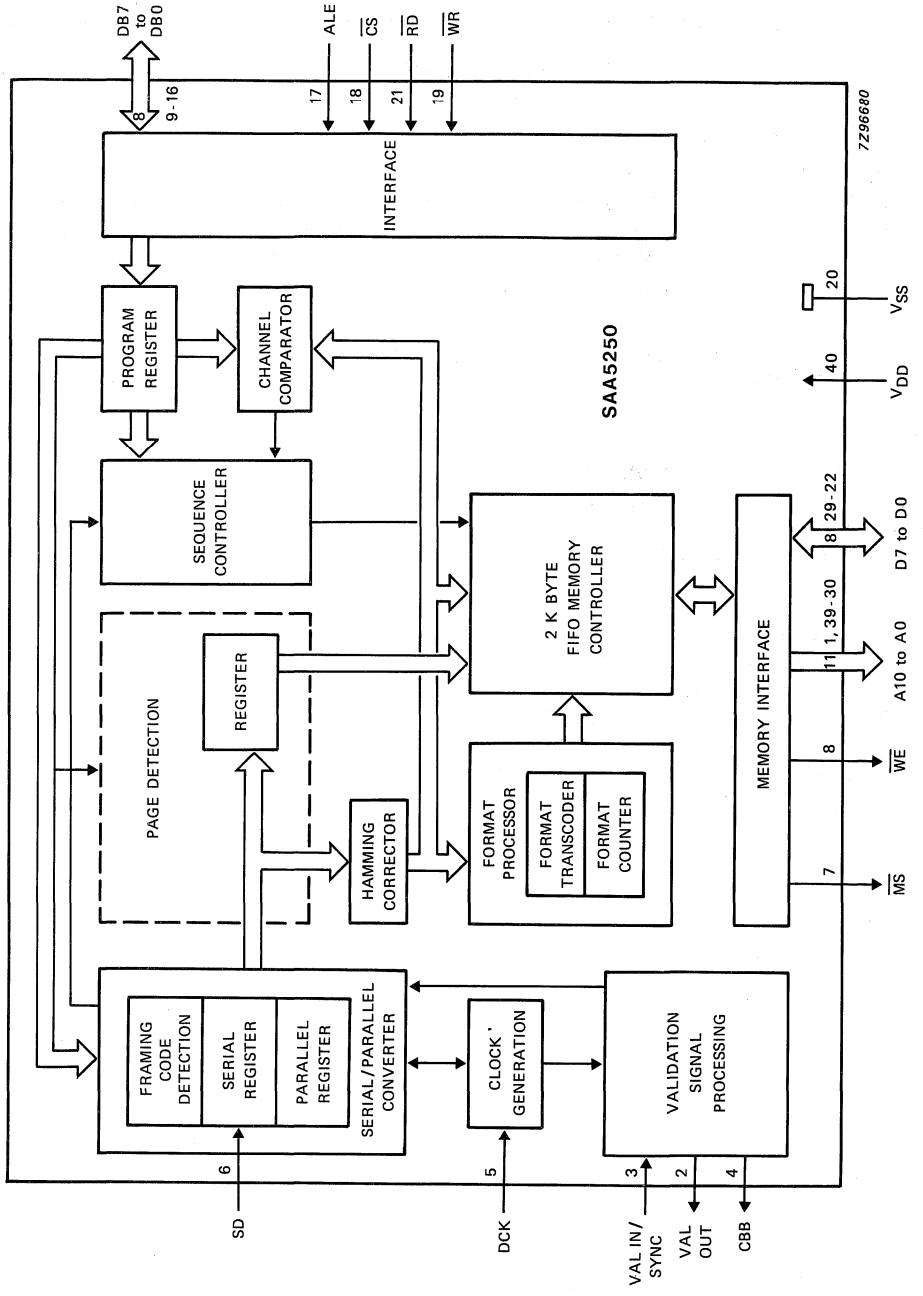


Fig. 1 Block diagram.

DEVELOPMENT DATA

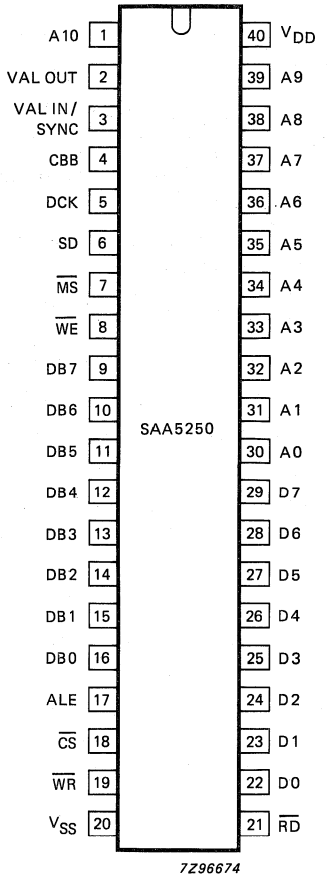


Fig. 2 Pinning diagram.

PINNING FUNCTION

mnemonic	pin no.	function
A10 and A0 to A9	1 and 30 to 39	Memory address outputs used by CIDAC to address a 2 K byte buffer memory
VAL OUT	2	Validation output signal used to control the location of the window for the framing code
VAL IN/SYNC	3	Validation input signal (line signal) used to give or calculate a window for the framing code detection
CBB	4	Colour burst blanking output signal used by the SAA5230 as a data slicer reset pulse
DCK	5	Data clock input, in synchronization with the serial data signal
SD	6	Serial data input, arriving from the demodulator
$\overline{MS}$	7	Chip enable output signal for buffer memory selection
$\overline{WE}$	8	Write command output for the buffer memory
DB7 to DB0	9 to 16	8-bit three state input/output data/address bus used to transfer commands, data and status between the CIDAC registers and the CPU
ALE	17	Demultiplexing input signal for the CPU data bus
$\overline{CE}$	18	Chip enable input for the SAA5250
$\overline{WR}$	19	Write command input (when LOW)
V_{SS}	20	ground
$\overline{RD}$	21	Read command input (when LOW)
D0 to D7	22 to 29	8-bit three state input/output data bus used to transfer data between CIDAC and the buffer memory
V_{DD}	40	+5 V power supply

FUNCTIONAL DESCRIPTION

Microcontroller interface

The microcontroller interface communicates with the CPU via the handshake signals DB7 – DB0, ALE, CS, $\overline{RD}$, $\overline{WR}$. The microcontroller interface produces control commands as well as programming the registers to write their contents or read incoming status/data information from the buffer memory. The details of the codes used to address the registers are given in Table 2.

The CIDAC is 'MOTEL' compatible (MOTEL compatible means it is compatible with standard **Mo**torola or **Intel** microcontrollers). It automatically recognizes the microcontroller type (such as the 6801 or 8501) by using the ALE signal to latch the state of the $\overline{RD}$ input. No external logic is required.

Table 1 Recognition signals

CIDAC	8049/8051 timing 1	6801/6805 timing 2
ALE $\overline{RD}$ $\overline{WR}$	ALE $\overline{RD}$ $\overline{WR}$	AS DS, E, $\Phi 2$ R/$\overline{W}$

Table 2 CIDAC register addressing

codes						
R	W	CS	DB2	DB1	DB0	function
1	0	0	0	0	0	write register R0
1	0	0	0	0	1	write register R1
1	0	0	0	1	0	write register R2
1	0	0	0	1	1	write register R3
1	0	0	1	0	0	write register R4
1	0	0	1	0	1	write register R5
1	0	0	1	1	0	write command register R6 (initialization command)
1	0	0	1	1	1	write register R7
0	1	0	0	0	0	read status
0	1	0	0	0	1	read data register
0	1	0	0	1	0	test (not used)
0	1	0	0	1	1	test (not used)

DEVELOPMENT DATA

Register organization

R0 register

Table 3 R0 Register contents

R04 slow/fast mode	R03 parity	R02 to R00 used prefixes
0 = slow mode 1 = fast mode	0 = no parity control 1 = odd parity	000 = DIDON long 001 = DIDON medium 010 = DIDON short 011 = not used 100 = U.K. teletext 101 = NABTS 110, 111 } without prefix

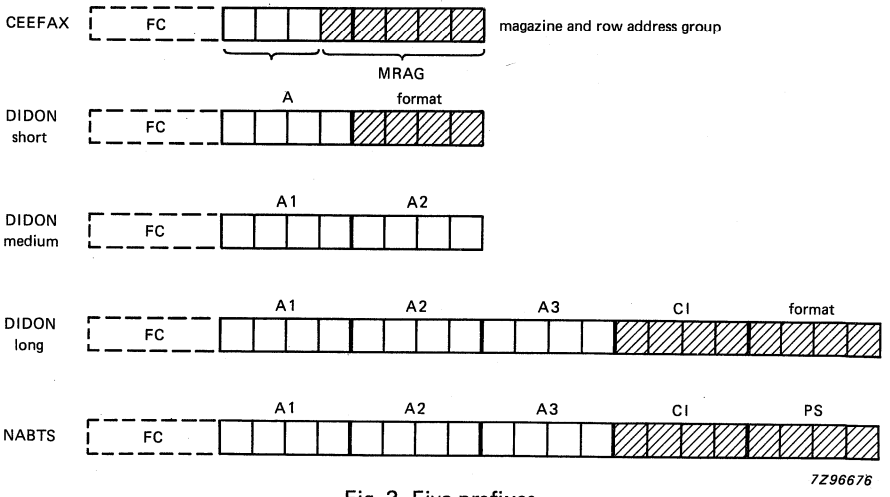


Fig. 3 Five prefixes.

All of the bytes (see Fig. 3) are Hamming protected. The hatched bytes are always stored in the memory in order to be processed by the CPU (see section 'Prefix processing'). In the mode without prefix all of the bytes which follow the framing code are stored in the memory until the end of the data packet, the format is then determined by the contents of the R3 register.

If R03 = 0; no parity control is carried out and the 8-bits of the incoming data bytes are stored in the fifo memory.

If R03 = 1; the 8th bit of the bytes following the prefix (data bytes) represents the result of the odd parity control.

If R04 = 0; the device operates in the slow mode. The CIDAC retrieves data from the user selected magazine (see section 'R1 and R2') and without searching for a start to a page stores the data into the FIFO memory.

If R04 = 1; the device operates in the fast mode. Prior to writing into the FIFO memory, the CIDAC searches for a start to a page which is variable due to the different prefixes:

- DIDON (long, medium and short): using the redundant bytes, SOH RS, X RS and SOH X (where X is a bit affected by a parity error)
- NABTS, the least significant bit of the PS byte is set to 1
- U.K. teletext, ROW = 0

R1 register

Table 4 R1 Register contents

R17 VAL IN/SYNC	R16 to R14 format table	R13 to R10 channel numbers (first digit)
1 = VAL 0 = SYNC	000 = list 1 001 = list 2 010 = list 3 011 = list 4 1XX = maximum/default value used (R3)	first digit hexadecimal value

Note

X = don't care

If VAL IN/SYNC = 1; the line signal immediately produces a validation signal for the framing code detection.

If VAL OUT = 0; the line signal is used as a starting signal for an internally processed validation signal (see Fig. 15). The framing code window width is fixed at 13 clock periods and the delay is determined by the contents of the R5 register (R56 to R50).

At any moment the user is able to ensure that the framing code window is correctly located. This is accomplished by the VAL OUT pin reflecting the internal validation signal. A CBB signal with programmable width (see section 'R7 register') can also be generated, this is used as a data slicer reset pulse by the SAA5230. The line signal is used as the starting point of the internal CBB signal width fixed by the contents of the R7 register.

If R16 = 0; then bits R15 and R14 provide the format table number using DIDON long and short prefixes (see Table 6).

If R16 = 1; then the format is determined by the contents of the R3 register.

The bits R13 to R10 represent the first channel number to be checked in the prefix. In U.K. teletext mode only 3 bits are required, so R13 = X.

Table 5 Format table

format byte B8, B6, B4 and B2	list 1	list 2	list 3	list 4
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	5	6	7
0101	8	9	10	11
0110	12	13	14	15
0111	16	17	18	19
1000	20	21	22	23
1001	24	25	26	27
1010	28	29	30	31
1011	32	33	34	35
1100	36	37	38	39
1101	40	41	42	43
1110	44	45	46	47
1111	48	49	50	51

Note

B8 = MSB and B2 = LSB.

R2 register

Table 6 R2 Register contents

R27 to R24	R23 to R20
channel number, third digit	channel number, second digit
(hexadecimal value, third digit)	(hexadecimal value, second digit)

Note

R27 and R23 = MSB and R24 and R20 = LSB

The R2 register provides the other two parts of the channel number (depending on the prefix) that require checking.

R3 register

Table 7 R3 register contents

R35 to R30 6-bit format maximum/default value
000000 = 0 000001 = 1 – – – 111111 = 63

This 6-bit byte gives:

- In the DIDON long and short mode, a maximum format in case of corrupted transmission (multiple errors on the Hamming corrector)
- A possible 63-bit format for all types of prefix

R4 register

Table 8 R4 register contents

R47 to R40
8-bit register used for storing the framing code value which will be compared with the third byte of each data line

R5 register

Table 9 R5 register contents

R57 negative/positive	R56 to R50 synchronization delay
0 = negative edge for sync signal 1 = positive edge for sync signal	7-bit sync delay, giving a maximum delay of $(2^7 - 1) \times 10^6$ µs/F (Hz)

Note

F = data clock acquisition frequency (DCK).

Using R57 it is possible to start the internal synchronization delay (t_{DVAL}) on the positive or negative edge.

DEVELOPMENT DATA

R6 write command register

This is a fictitious register. Only the address code (see Table 2) is required to reset the CIDAC. See Table 11 for the status of the FIFO memory on receipt of this command.

R7 register

Table 10 R7 register contents

R75 to R70
6-bit register used to give a maximum colour burst blanking signal of: $(2^6 - 1) \times 10^6 \mu s/F$ (Hz)

Note

F = data clock acquisition frequency.

Fifo status register (read R0 register)

Table 11 Fifo register contents

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 1, data not present in the read data register	DB0 = 0 memory not full

Once the relevant prefix and the right working modes have been given by the corresponding registers, a write command to the R6 register enables the CIDAC to accept and process serial data.

Channel comparator

This is a four bit comparator which compares the three user hexadecimal defined values in R1 and R2 to the corresponding bytes of the prefix coming from the Hamming corrector. If the three bytes match, the internal process of the prefix continues. If they do not match the CIDAC returns to a wait state until the next broadcast data package is received.

FIFO memory controller

The FIFO memory contains all the necessary functions required for the control of the 11-bit address memory (2 K byte). The functions contained in the FIFO memory are as follows:

- write address register (11-bits)
- read address register (11-bits)
- memory pointer (11-bits)
- address multiplexer (11-bits)
- write data register (8-bits)
- read data register (8-bits)
- data multiplexer
- control logic

The FIFO memory provides the memory interface with the following:

- 11-bit address bus (A10 to A0)
- 8-bit data bus (D7 to D0)
- two control signals, memory select ($\overline{MS}$) and write enable ($\overline{WE}$)

Operation

The CIDAC uses the same clock signal for data acquisition and internal processing, this allows the CIDAC to have a write and a read cycle during each character period (see Fig. 13). The first half of the character period is a write cycle and the second half is a read cycle. Consequently, for an 8 MHz bit rate the maximum memory cycle time is 500 ns.

When the first data byte is written into the FIFO memory, thus transferred into the read register, the FIFO memory enters the status shown in Table 12.

Table 12 FIFO status

DB2 to DB0		
DB2 = 1 memory empty	DB1 = 0 data available	DB0 = 0 memory not full

When the FIFO memory is full two events occur:

- the write address register points to the next address after the last written address
- when new data is to be written, the memory select signal output ceases

Memory interface

The memory interface contains all the buffers for the memory signals mentioned in the section 'FIFO memory controller'.

Page detection

This part of the CIDAC contains a parallel register with logic which detects (only in fast mode) a start of a page or data group (see section 'R0 register').

Hamming correction (see Tables 13 and 14)

The Hamming correction provides (see section 'Prefix processing'):

- hexadecimal value of the Hamming code
- accept/reject code signal
- parity information

Table 13 Hamming correction (coding)

Hexadecimal notation	B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	1
3	0	1	0	1	1	1	1	0
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	0	1	1
6	0	0	1	1	1	0	0	0
7	0	0	1	0	1	1	1	1
8	1	1	0	1	0	0	0	0
9	1	1	0	0	0	1	1	1
A	1	0	0	0	1	1	0	0
B	1	0	0	1	1	0	1	1
C	1	0	1	0	0	0	0	1
D	1	0	1	1	0	1	1	0
E	1	1	1	1	1	1	0	1
F	1	1	1	0	1	0	1	0

Note

$B7 = B8 \oplus B6 \oplus \overline{B4}$
$B5 = B6 \oplus \overline{B4} \oplus \overline{B2}$
$B3 = \overline{B4} \oplus \overline{B2} \oplus B8$
$B1 = \overline{B2} \oplus B8 \oplus B6$

$\oplus$ = exclusive OR gate function
B8, B6, B4 and B2 = data bits
B7, B5, B3 and B1 = redundancy bits

Table 14 Hamming correction (decoding)

A	B	C	D	interpretation	information
1	1	1	1	no error	accepted
0	0	1	0	error on B8	corrected
1	1	1	0	error on B7	accepted
0	1	0	0	error on B6	corrected
1	1	0	0	error on B5	accepted
1	0	0	0	error on B4	corrected
1	0	1	0	error on B3	accepted
0	0	0	0	error on B2	corrected
0	1	1	0	error on B1	accepted
A.B.C = 0			1	multiple errors	rejected

Note

$A = B8 \oplus B6 \oplus B2 \oplus B1$
$B = B8 \oplus B4 \oplus B3 \oplus B2$
$C = B6 \oplus B5 \oplus B4 \oplus B2$
$D = B8 \oplus B7 \oplus B6 \oplus B5 \oplus B4 \oplus B3 \oplus B2 \oplus B1$

$\oplus$ = exclusive OR gate function

Format processing

The format processing consists of two parts:

part 1

A format transcoder produces a 6-bit code (up to 63) and uses the following as inputs:

- DIDON long and short prefixes;
  hamming corrected code (4-bits)
  accept/reject code condition
  table number (see section 'R1 register', bits R15 and R14)
- Other prefixes (R16 = 1)
- 6-bit maximum/default format (see section 'R3 register')

part 2

A format counter operating at the character clock frequency which receives the 6-bit code from the format transcoder and is used to check the data packet length following the prefix.

Serial/parallel converter

The serial/parallel converter consists of three parts:

- An 8-bit shift register which receives the SD input and operates at the bit frequency (DCK).
- An 8-bit parallel register used for storage.
- A framing code detection circuit. This logic circuit compares the 8-bits of the R4 register with that of the serial register. If seven bits out of eight match (in coincidence with a validation window), it produces a start signal for a new teletext data line to the sequence controller.

Clock generation

The clock generator does the following:

- acts as a buffer for the DCK clock
- generates the character clock

As soon as a framing code has been detected, a divide by 8 counter is initialized and the character clock is started. The clock drives the following:

- sequence controller
- parallel registers
- format counter

Processing of VAL and CBB signals

The circuit has one input (VAL IN/SYNC) and two outputs (VAL OUT and CBB). The circuit consists of:

- 7-bit counter operating at DCK frequency which produces the framing code validation pulse delay
- 7-bit comparator which compares the contents of the R5 register (bits R56 to R50) to the bit counter
- a 6-bit counter operating at DCK frequency which produces the CBB pulse width
- 6-bit comparator which compares the contents of the R7 register (bits R75 to R70) to the bit counter
- control logic required to provide the start condition for the VAL signal and the CBB pulse width (on the negative or positive edge of the sync signal)

The CBB signal usefulness occurs when the associated video processor:

- has no sandcastle pulse to send back to the demodulator
- carries out the synchronization of the time base clock. In this event the CBB acts as a data slicer reset pulse

The VAL OUT is a control signal which reflects the internal framing code window.

Prefix processing (see Table 21)

Figs 4 to 9 show the acquisition flow charts for each prefix type coded in the R0 register (bits R02 to R00).

As soon as an initialization command is received by the CIDAC, a write command to the R6 register (only the address is significant), is ready to receive data from a dedicated channel number and store the data in the FIFO memory (explained in the following paragraphs, each paragraph being dedicated to an individual type of prefix).

DIDON long (see Fig. 4)

In this mode, the continuity index, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 15 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 16 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

Note

A/R = 0, if rejected
A/R = 1, if accepted
X = don't care

DIDON mediun (see Fig. 5)

Only data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

DIDON short (see Fig. 6)

In this mode, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 17 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

NABTS (see Fig. 7)

In this mode, the continuity index, packet structure and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 18 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 19 Packet structure processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	PS3	PS2	PS1	PS0

U.K. teletext (see Fig. 8)

In this mode, the magazine and row address group (two bytes) and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a flag detection.)

Table 20 Magazine and row address group processing results

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	RW4	RW3	RW2	RW1	RW0

Without prefix

All the data following the framing code are stored in the FIFO memory.

Table 21 Prefix processing

prefixes	construction of prefixes	bytes stored in FIFO memory during slow mode	bytes stored in FIFO memory during fast mode
DIDON long	A1, A2, A3, CI, F and D	CI, F and D	CI*, F* and D*
DIDON medium	A1, A2 and D	D	D*
DIDON short	A1, F and D	F and D	F* and D*
NABTS	A1, A2, A3 CI, PS and D	CI, PS and D	CI*, PS* and D*
U.K. teletext	MRAG and D	MRAG and D	MRAG* and D*
without prefix		all bytes of the data packet following the framing code are written into the FIFO memory	

Note

* = after page/flag detection
A1, A2, A3 are channel numbers
CI = continuity index
F = format
PS = packet structure
D = data
MRAG = magazine and row address group

DEVELOPMENT DATA

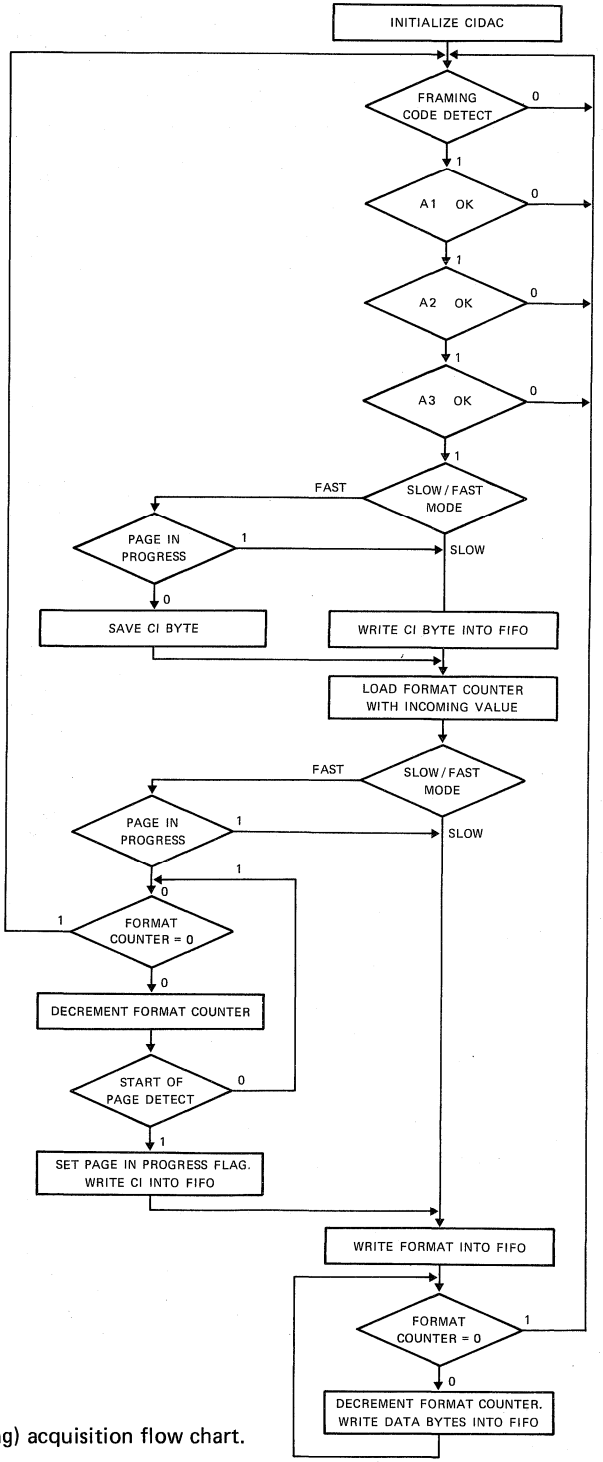


Fig. 4 DIDON (long) acquisition flow chart.

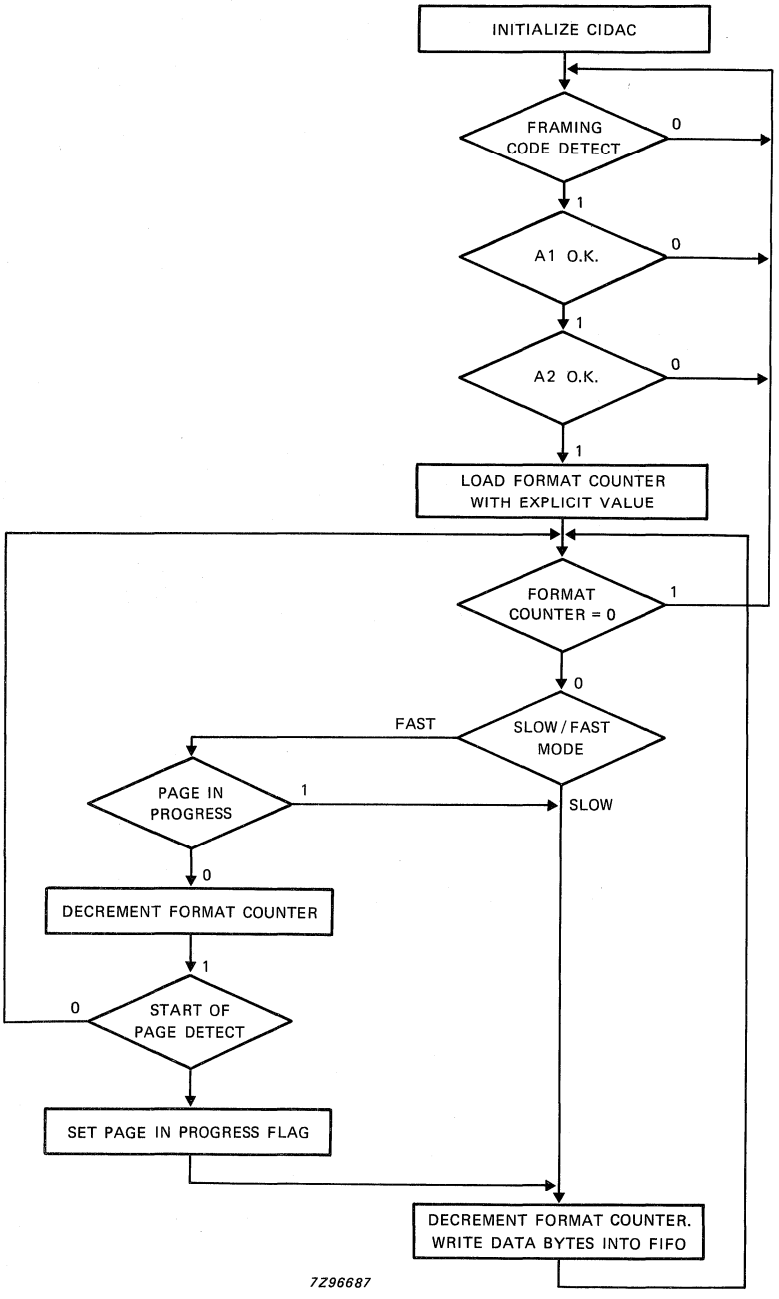


Fig. 5 DIDON (medium) acquisition flow chart.

DEVELOPMENT DATA

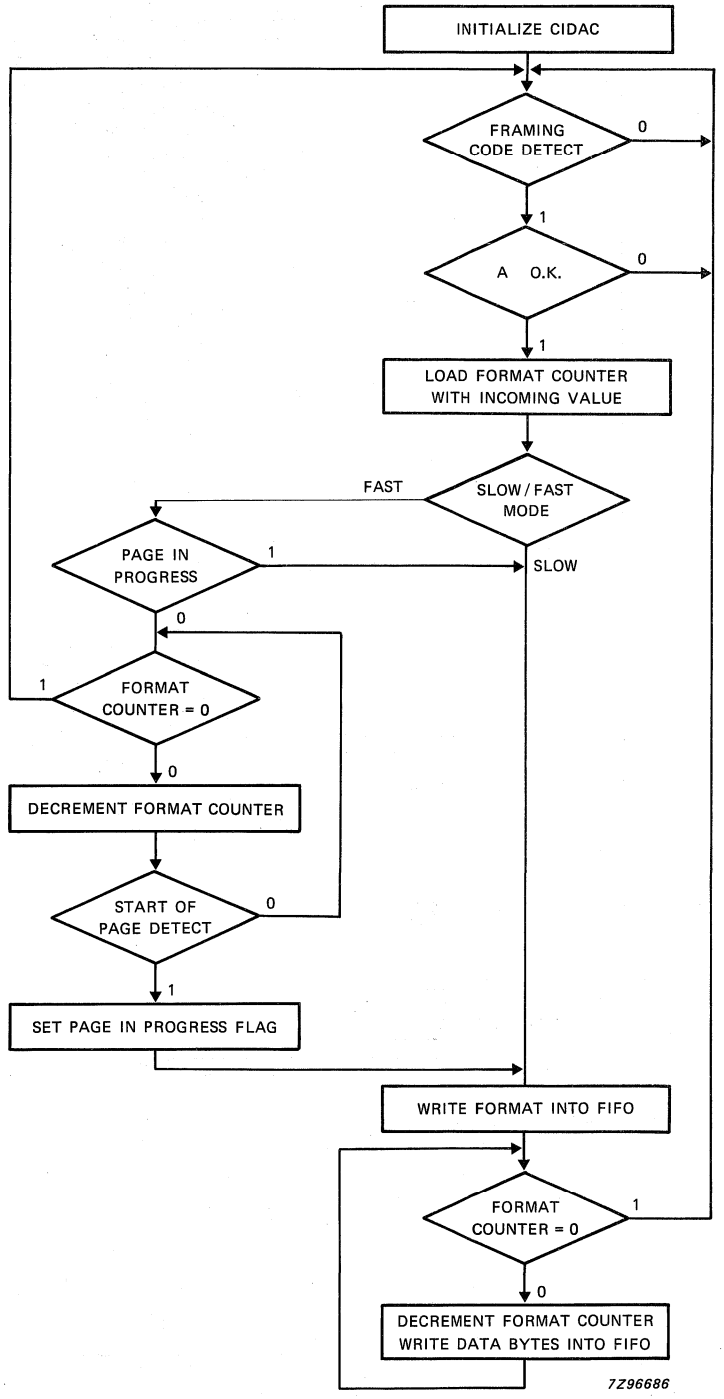


Fig. 6 DIDON (short) acquisition flow chart.

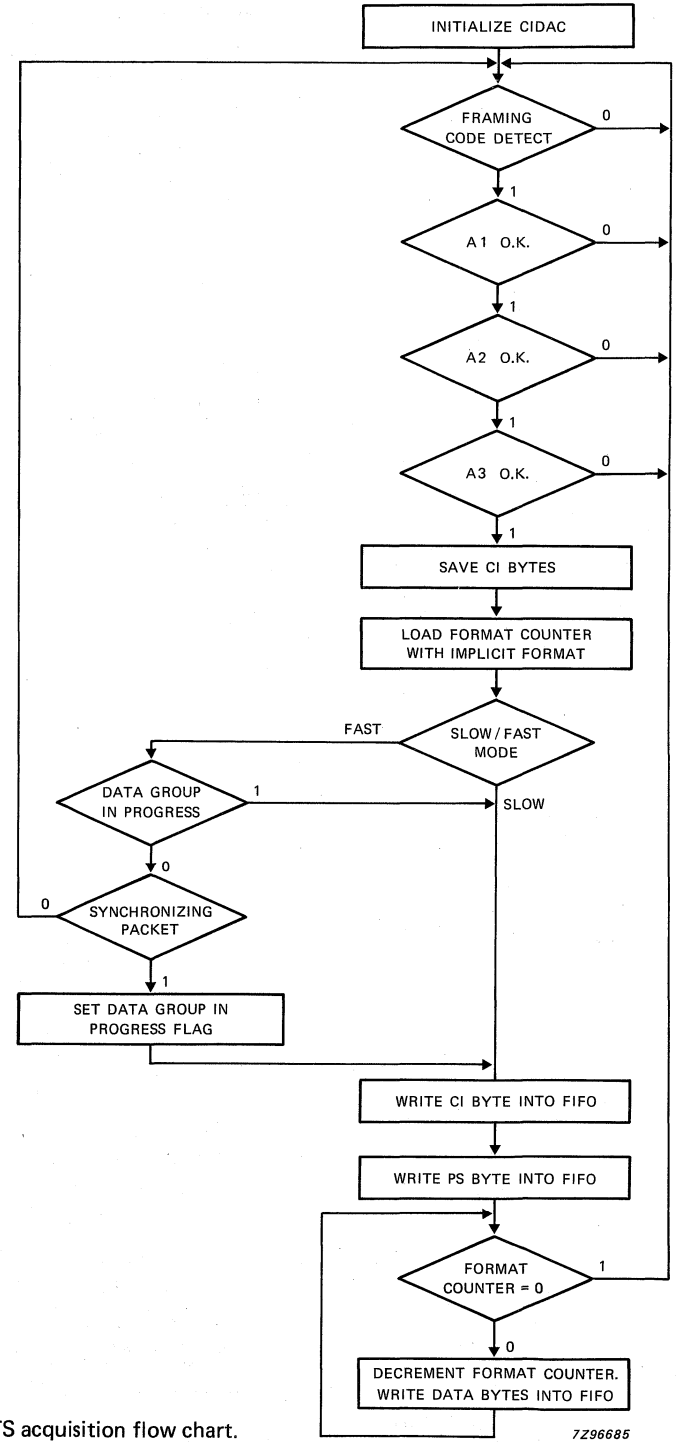


Fig. 7 NABTS acquisition flow chart.

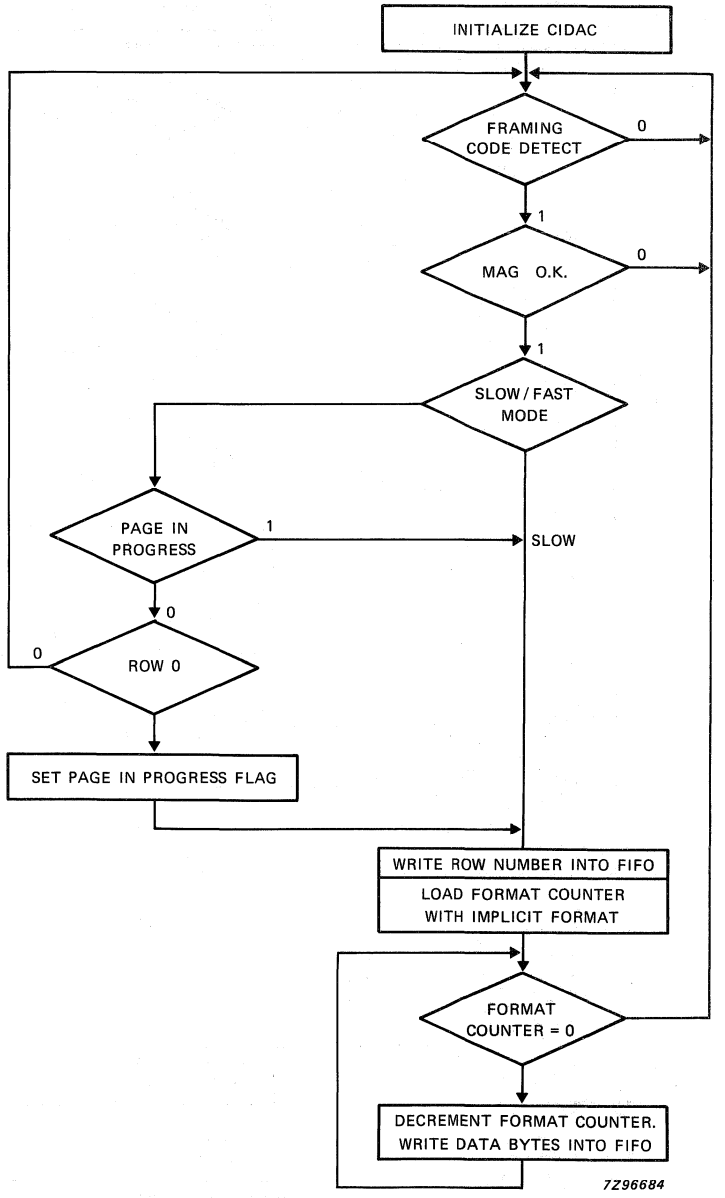


Fig. 8 U.K. teletext acquisition flow chart.

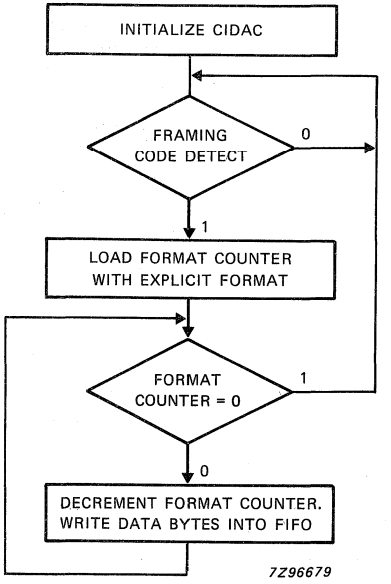


Fig. 9 Without prefix acquisition chart.

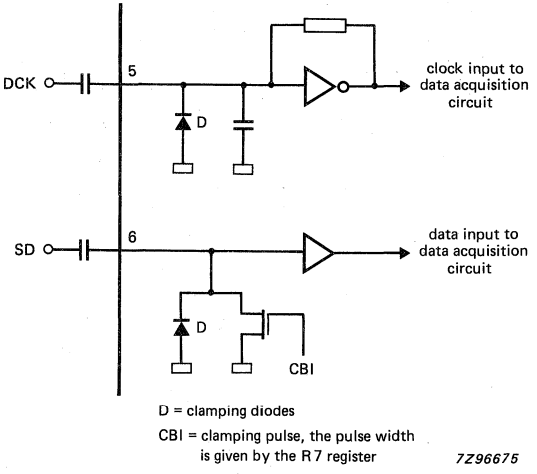


Fig. 10 SD and DCK input circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,3	6,5	V
Input voltage range		V_I	−0,3	V_{DD}+0,3	V
Total power dissipation		P_{tot}	−	400	mW
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−20	+125	°C

D.C. CHARACTERISTICS (except SD and DCK)

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	5,0	5,5	V
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−	−	0,8	V
Input leakage current		I_I	−	−	1,0	μA
Output voltage HIGH	I_{load} = 1 mA	V_{OH}	V_{DD}−0,4	−	−	V
Output voltage LOW	I_{load} = 4 mA, at pins 9 to 16 and 22 to 29	V_{OL}	−	−	0,4	V
	I_{load} = 1 mA all other outputs	V_{OL}	−	−	0,4	V
Power dissipation		P	−	5	−	mW
Input capacitance		C_I	−	−	7,5	pF

DEVELOPMENT DATA

SD and DCK D.C. CHARACTERISTICS (see Fig. 10)

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
DCK						
Input voltage range (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input current	V_I = 0 to V_{DD}	I_I	5	–	200	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF
SD						
D.C. input voltage range HIGH	note 1	V_{IH}	2,0	–	–	V
D.C. input voltage range LOW	note 2	V_{IL}	–	–	0,8	V
A.C. input voltage (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input leakage current	V_I = 0 to V_{DD}	I_I	–	–	10	μA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF

A.C. CHARACTERISTICS

V_{DD} = 5 V ±10%; Reference levels for all inputs and outputs, V_{IH} = 2 V; V_{IL} = 0,8 V; V_{OH} = 2,4 V; V_{OL} = 0,4 V; C_L = 50 pF on DB7 to DB0; T_{amb} = 0 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Microcontroller interface	Figs 11 and 12					
Cycle time		t_{CY}	400	–	–	ns
Address pulse width		t_{LHLL}	50	–	–	ns
$\overline{RD}$ HIGH or $\overline{WR}$ to ALE HIGH	Fig. 11	t_{AHRD}	0	–	–	ns
DS LOW to AS HIGH	Fig. 12	t_{AHRD}	0	–	–	ns
ALE LOW to $\overline{RD}$ LOW or $\overline{WR}$ LOW	Fig. 11	t_{ALRD}	30	–	–	ns
AS LOW to DS HIGH	Fig. 12	t_{ALRD}	30	–	–	ns
Write pulse width		t_{WL}	120	–	–	ns
Address and chip select set-up time		t_{ASL}	10	–	–	ns
Address and chip select hold time		t_{AHL}	20	–	–	ns
Read to data out period		t_{RD}	–	–	130	ns
Data hold after $\overline{RD}$		t_{DR}	10	–	100	ns
R/$\overline{W}$ to DS set-up time	Fig. 12	t_{RWS}	40	–	–	ns
R/$\overline{W}$ to DS hold time	Fig. 12	t_{RWH}	10	–	–	ns
Data set-up time	write cycle	t_{DW}	50	–	–	ns
Data hold time	write cycle	t_{WD}	10	–	–	ns
Read pulse width	note 3	t_{RL}	150 or DCK + 50	–	–	ns

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Memory interface	Fig. 13					
$\overline{WE}$ LOW to DCK falling edge		t_{WEL}	10	–	80	ns
$\overline{WE}$ HIGH to DCK falling edge		t_{WEH}	10	–	80	ns
$\overline{MS}$ LOW to DCK rising edge		t_{MSL}	10	–	80	ns
$\overline{MS}$ HIGH to DCK rising edge		t_{MSH}	10	–	85	ns
Address output from DCK rising edge		t_{AV}	10	–	120	ns
Data output from $\overline{WE}$ falling edge		t_{DWL}	0	–	10	ns
Data hold from $\overline{WE}$ rising edge		t_{DWH}	0	–	–	ns
Address set-up time to data	note 4	t_{AD}	–	–	3 x DCK – 110	ns
$\overline{WE}$ pulse width	note 5	t_{WEW}	3 x DCK	–	–	ns
$\overline{MS}$ pulse width	note 6	t_{MSW}	2 x DCK	–	–	ns
Demodulator interface (see SD and DCK D.C. CHARACTERISTICS)	Fig. 14					
DCK LOW	conversion rate < 7,5 MHz	t_{DCKL}	55	–	–	ns
DCK HIGH	conversion rate < 7,5 MHz	t_{DCKH}	55	–	–	ns
Serial data set-up time		t_{SSD}	0	–	–	ns
Serial data hold time		t_{HSD}	30	–	–	ns
Validation signal set-up time		t_{SVALI}	50	–	–	ns
Validation signal hold time		t_{HVALI}	50	–	–	ns
Other I/O signals	Fig. 15					
User definable width as a multiple of DCK period		t_{WCBB}	0	–	63	DCK
Validation signal width	note 7	t_{WVAL}	X	12	X	DCK
User definable delay as a multiple of DCK period		t_{DVAL}	0	–	127	DCK

Notes to the characteristics

1. Unless R7 = 00 the value given is unacceptable.
2. When CBI signal is maintained at 0 V (R7 = 00) and if SD input signal is correctly referenced to ground, no coupling capacitor is required.
3. DCK + 50 is the DCK period plus 50 ns.
4. 3 x DCK − 110 is 3 x DCK period − 110 ns.
5. 3 x DCK is 3 x DCK period.
6. 2 x DCK is 2 x DCK period.
7. X = irrelevant.

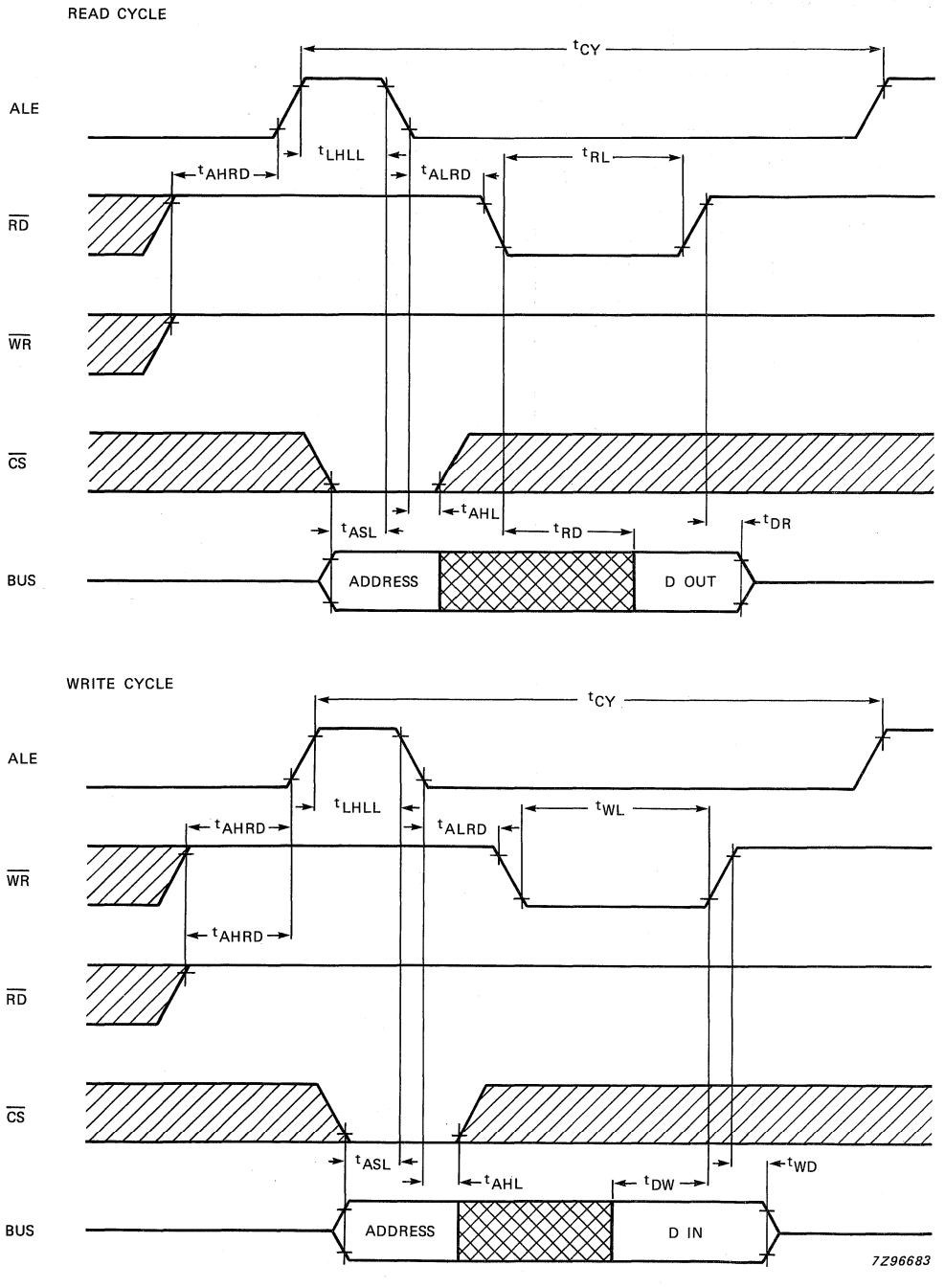
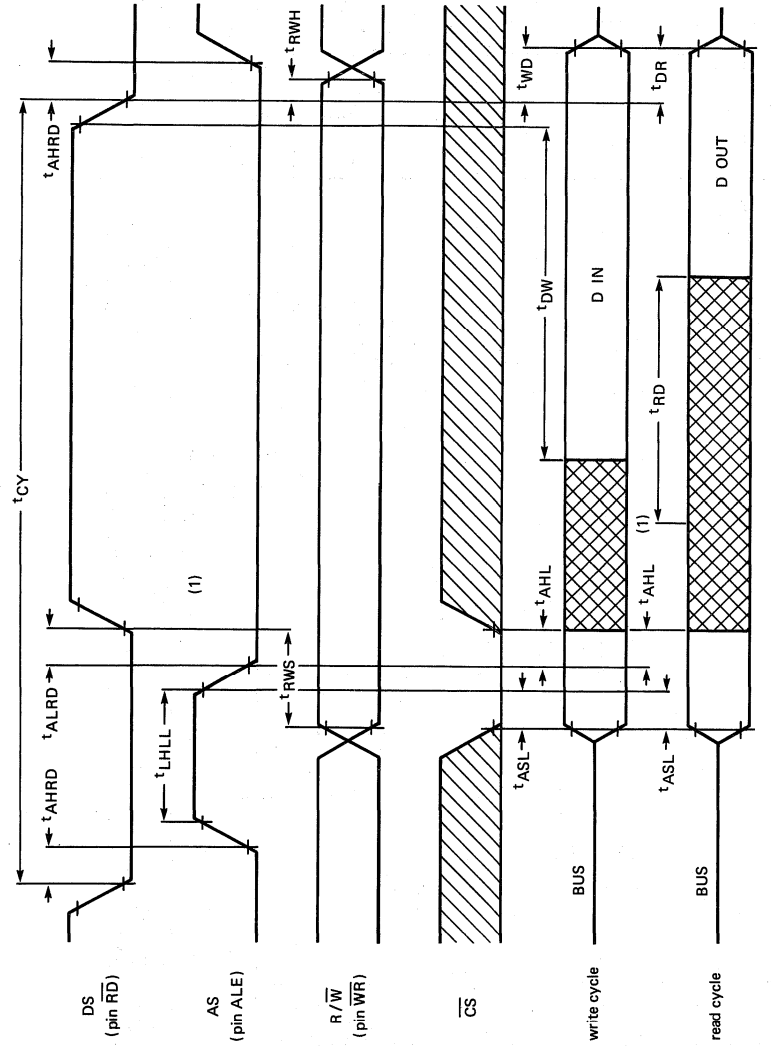


Fig. 11 Timing diagram for microcontroller interface (Intel).

DEVELOPMENT DATA



(1) ALE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and DB7 to DB0

Fig. 12 Timing diagram for microcontroller interface (Motorola).

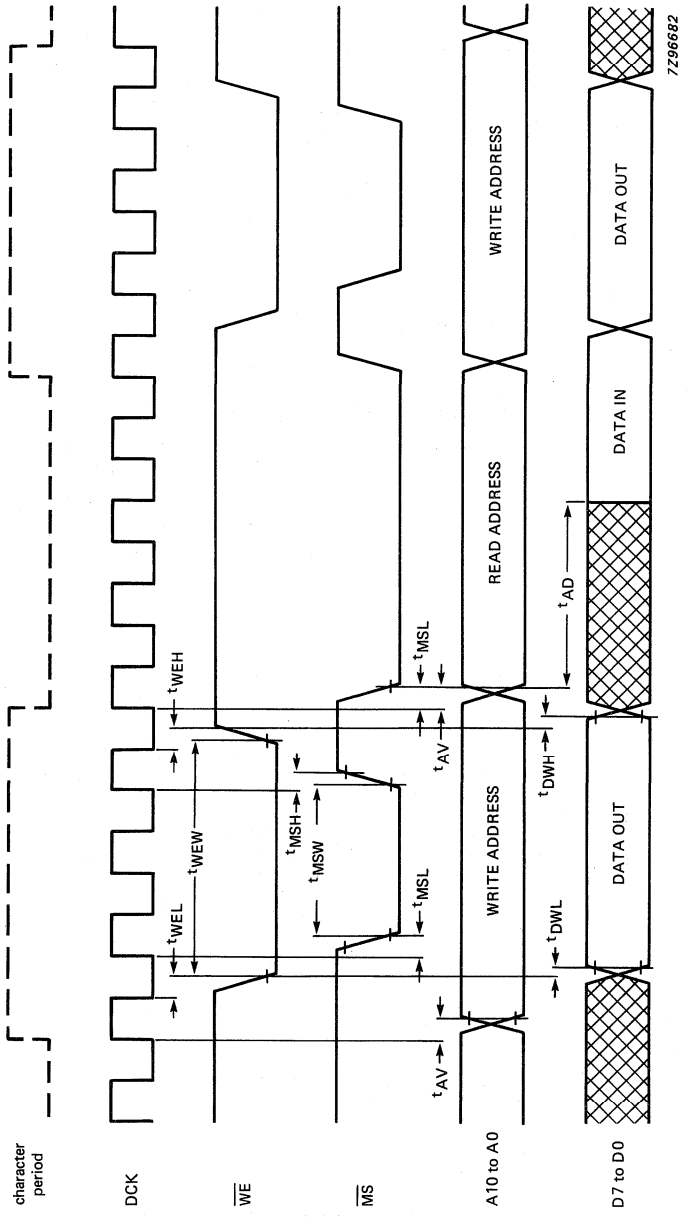


Fig. 13 Timing diagram for memory interface.

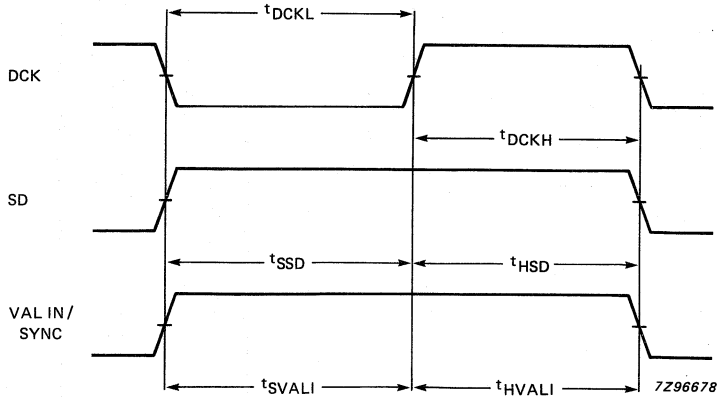


Fig. 14 Timing diagram for demodulator interface.

DEVELOPMENT DATA

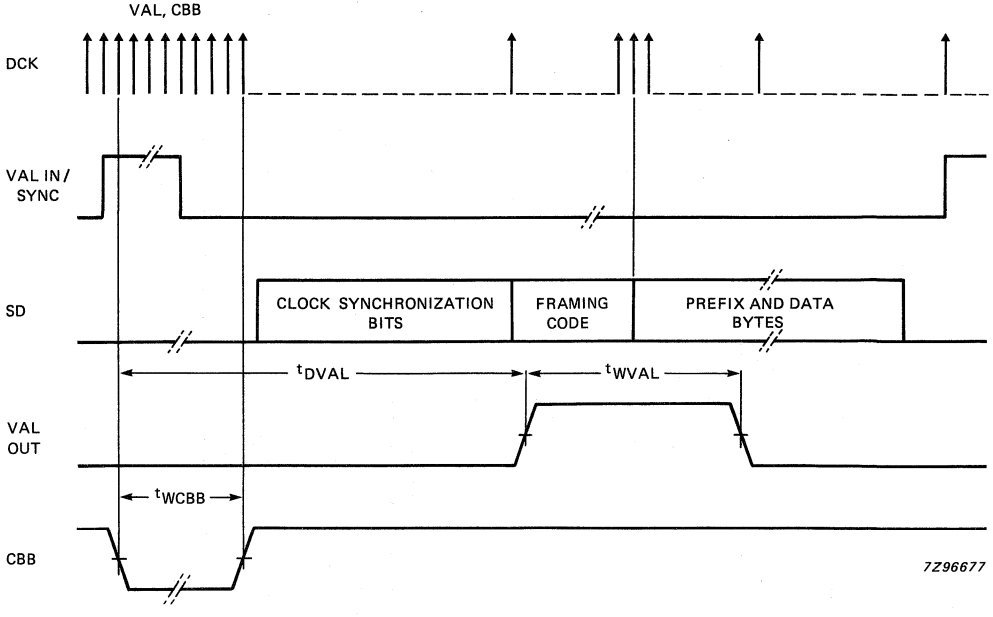


Fig. 15 Timing diagram for all other I/O signals.

EUROM 50 Hz

GENERAL DESCRIPTION

The SAA5351 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

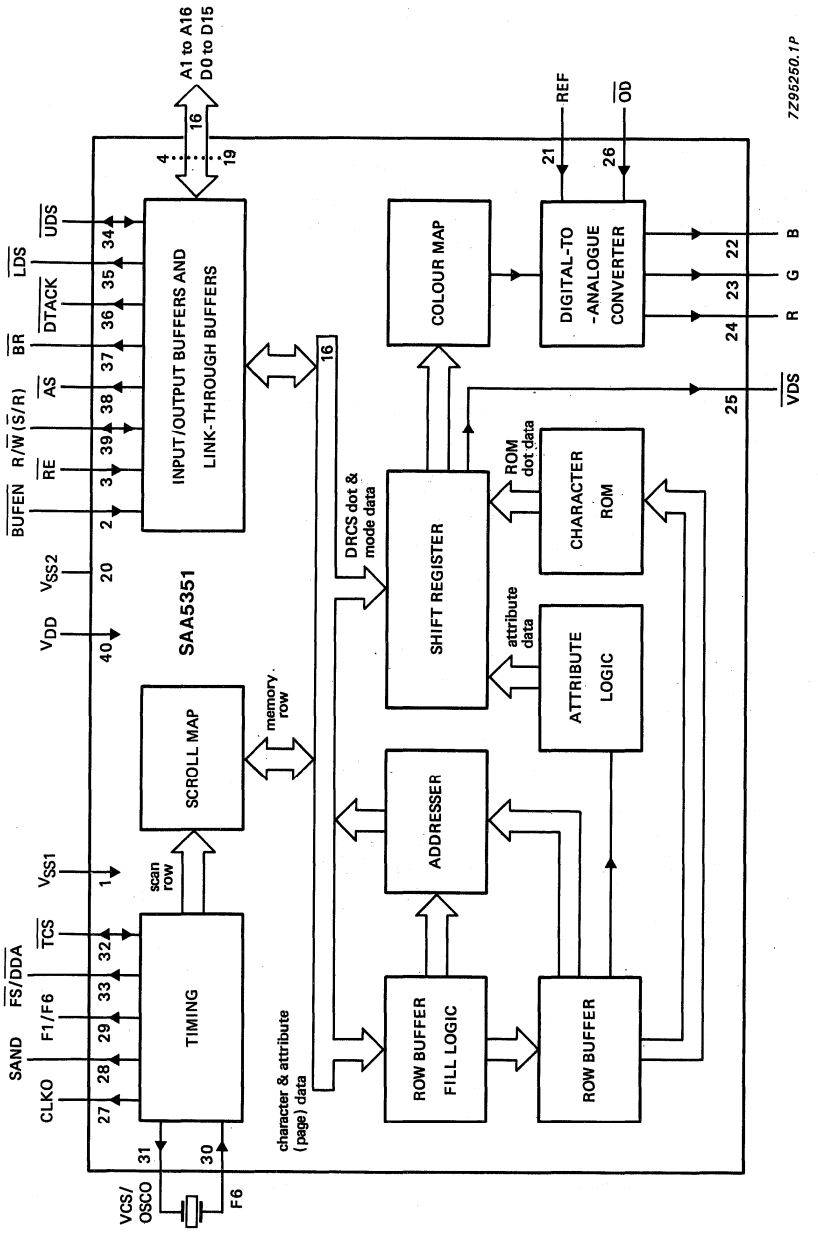


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	V_{SS1}	Ground 0 V.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS2}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	$R/\overline{W}$ ($\overline{S}/R$)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+5 V).

PINNING (continued)

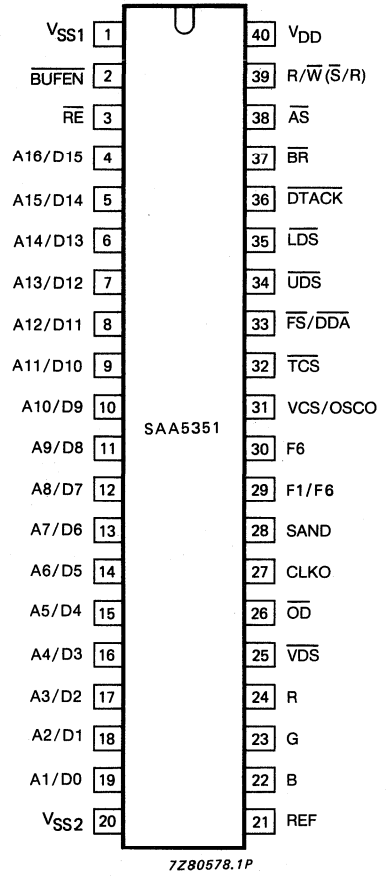


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	390	mA
INPUTS					
F6					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	2,0	7,0	V
Input leakage current at V_I = 0 to $V_{CC\,max}$; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input leakage current at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{IL}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance (note 1)	C_L	–	–	130	pF
F1/F6, $\overline{DDA}$/$\overline{FS}$					
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{LDS}$, $\overline{AS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{DTACK}$, $\overline{BR}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA (note 10)	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA
CLOCKO					
Output voltage HIGH	V_{OH}	2,0		V_{DD}	V
Output voltage LOW	V_{OL}	0		0,8	V
Load capacitance (note 1)	C_L	–		50	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW	V_{OL}	0	–	0,8	V
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
INPUTS/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Output leakage current (output OFF) at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Output leakage current at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 to 100 μA	V_{OH}	2,0	–	6,0	V
Output voltage LOW at V_{OL} = 3,2 mA	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	50	pF
A1/D0 to A16/D15					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Output leakage current V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{UDS}$; R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Output leakage current at V_I = 0 to V_{DD} + 0,3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_{IN}	–	–	10	pF
Output voltage HIGH (I_{OH} = −200 μA)	V_{OH}	2,0	–	V_{DD}	V
Output voltage LOW (I_{OH} = 3,2 mA)	V_{OL}	0	–	0,8	V
Load capacitance (note 1)	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Values guaranteed at 0,8 V and 2,0 V levels F6 input frequency at 6 MHz					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	60	ns
F1 HIGH time (note 5)	t_{F1H}	400	500	580	ns
F1 LOW time (note 5)	t_{F1L}	400	500	580	ns
F6 HIGH time	t_{F6H}	40	83	120	ns
F6 LOW time	t_{F6L}	40	83	120	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 1, 6, 7 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time (note 9)	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	290	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	280	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers					
(notes 6, 7 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM					
(Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 8)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise (notes 1, 6 and 7)	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. All pins are tested with a 150 pF load capacitor.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V.
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V.
5. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
6. Reference levels = 0,8 to 2,0 V.
7. F6 input at 6 MHz.
8. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.
9. This timing may be infringed at the beginning and end of the memory access window.
10. Output voltage guaranteed when programmed for bottom level.

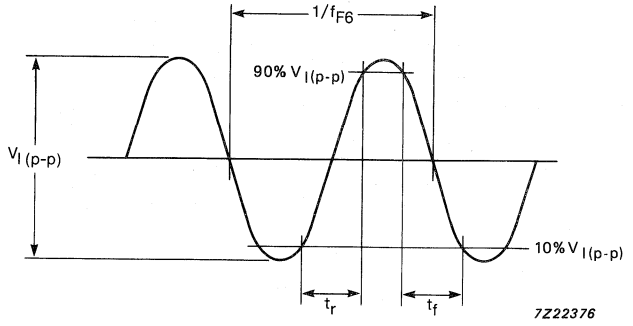
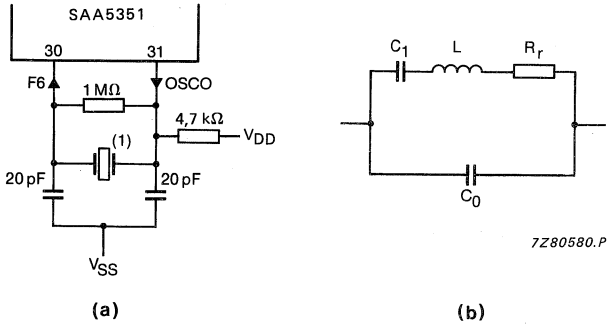


Fig. 3 F6 input waveform.



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5351 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

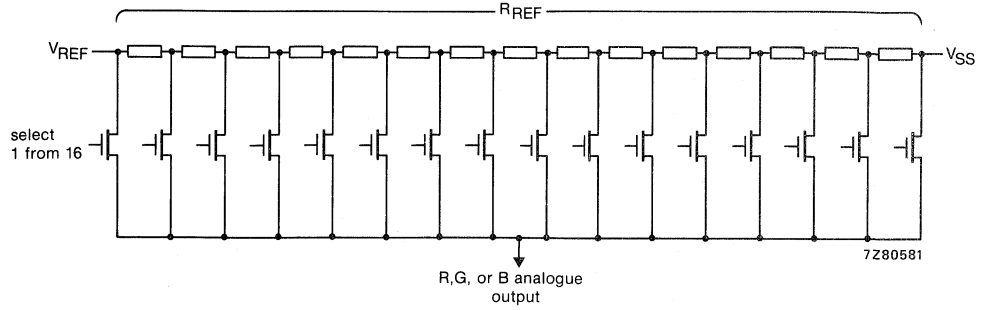


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

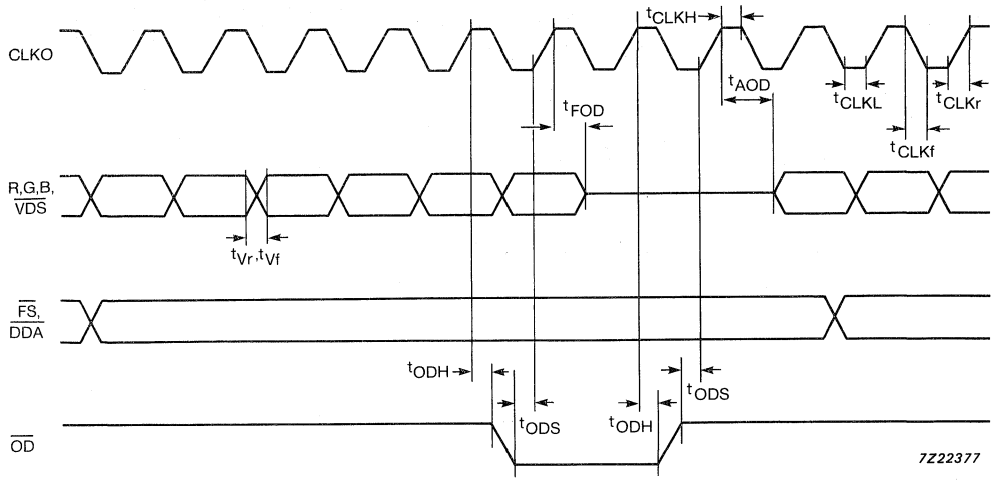


Fig. 6 Video timing.

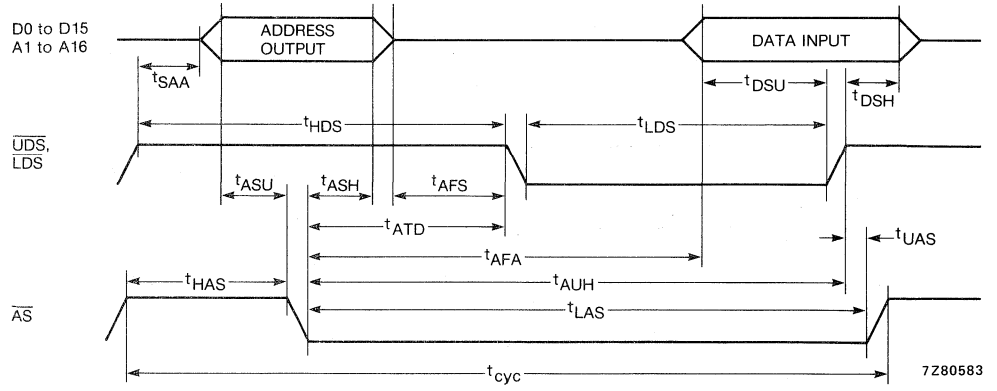


Fig. 7 Memory access timing.

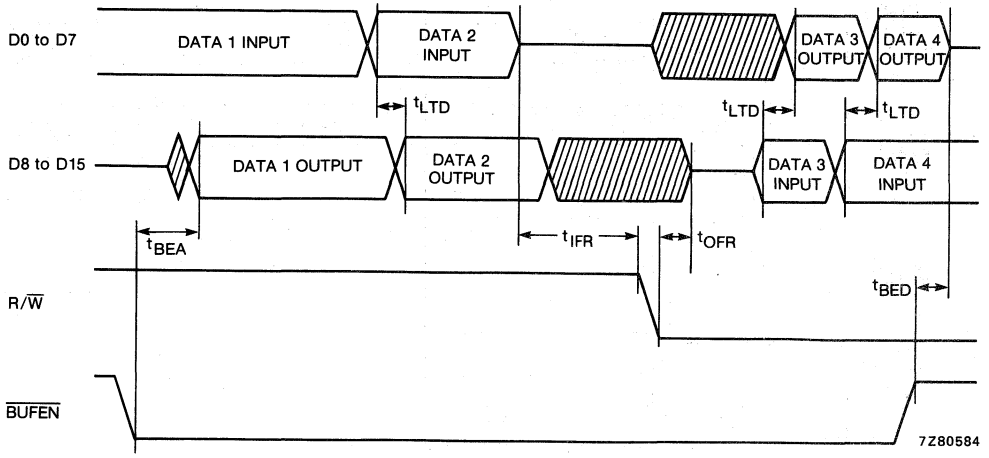


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

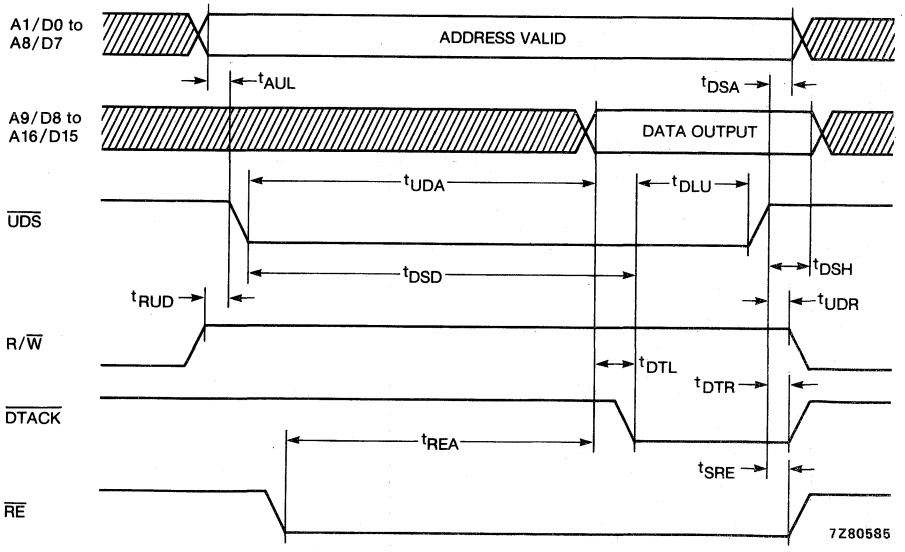


Fig. 9 Timing of microprocessor read from EUROM.

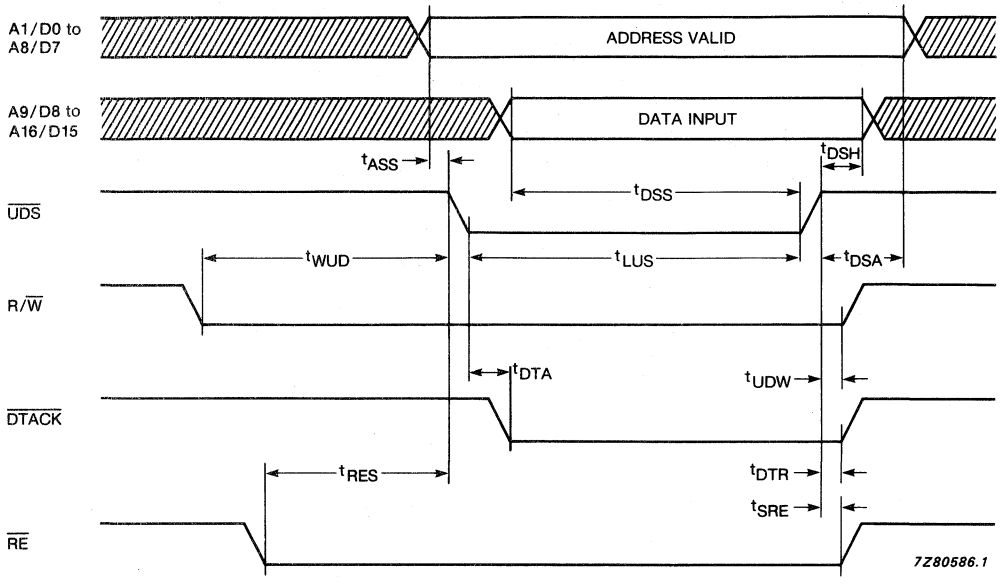


Fig. 10 Timing of microprocessor write to EUROM.

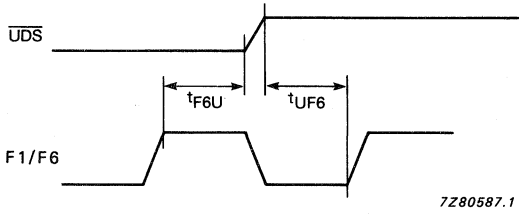


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

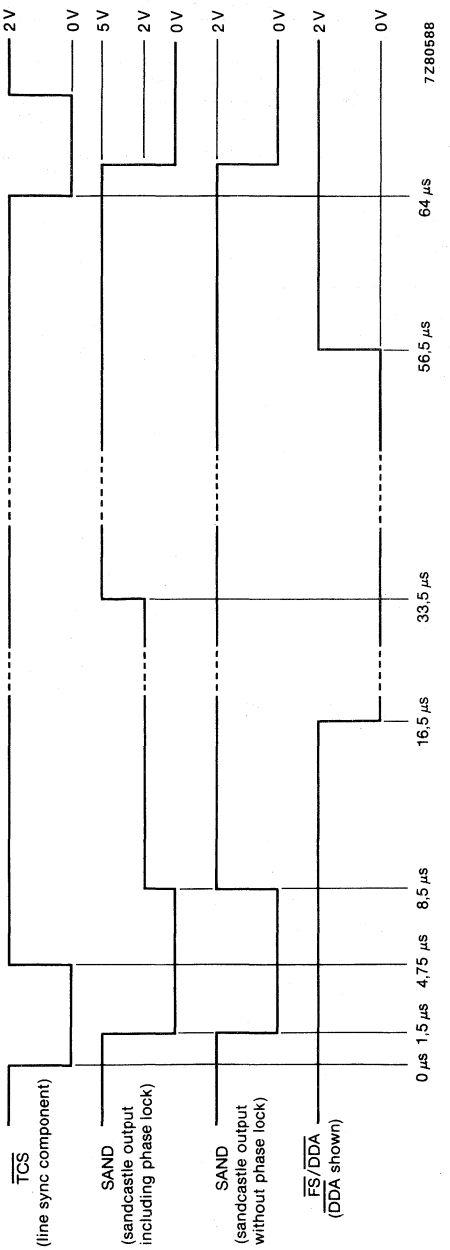


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6 MHz.

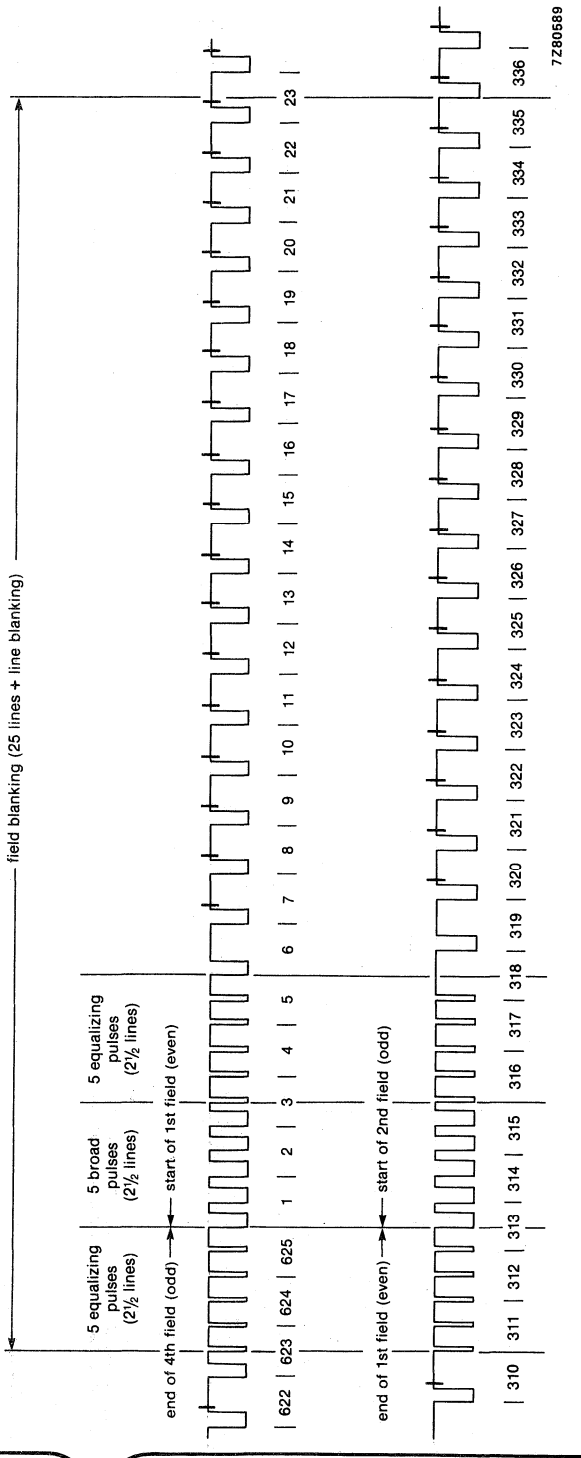


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,75 μs; equalizing pulse widths = 2,25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

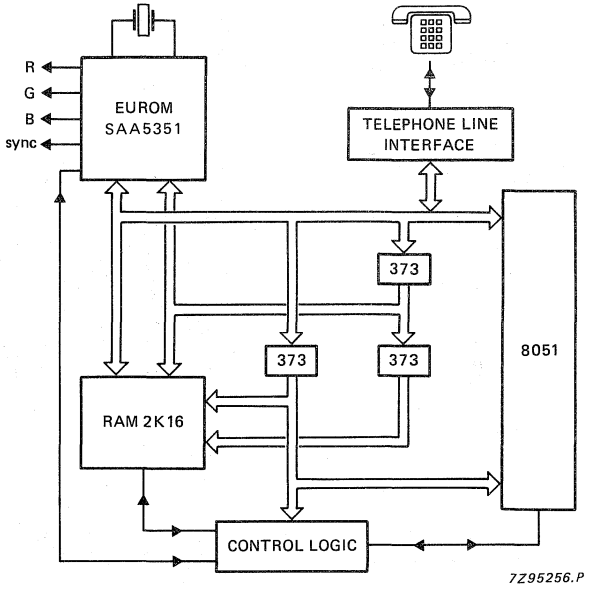


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

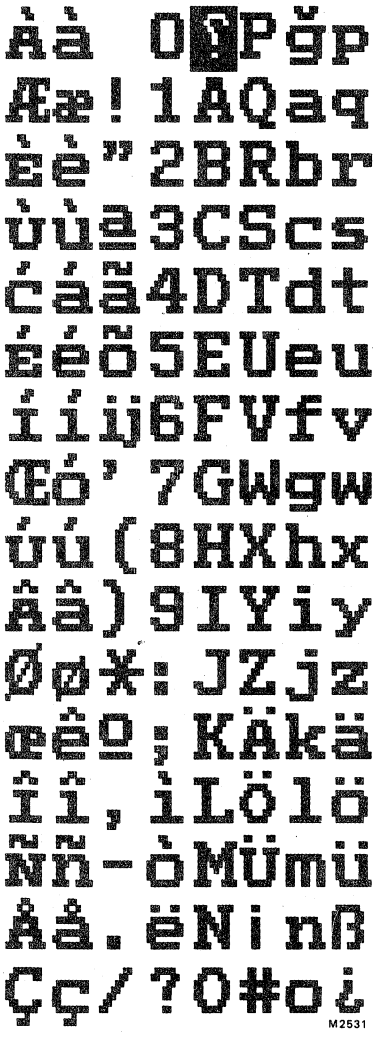
The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz (pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

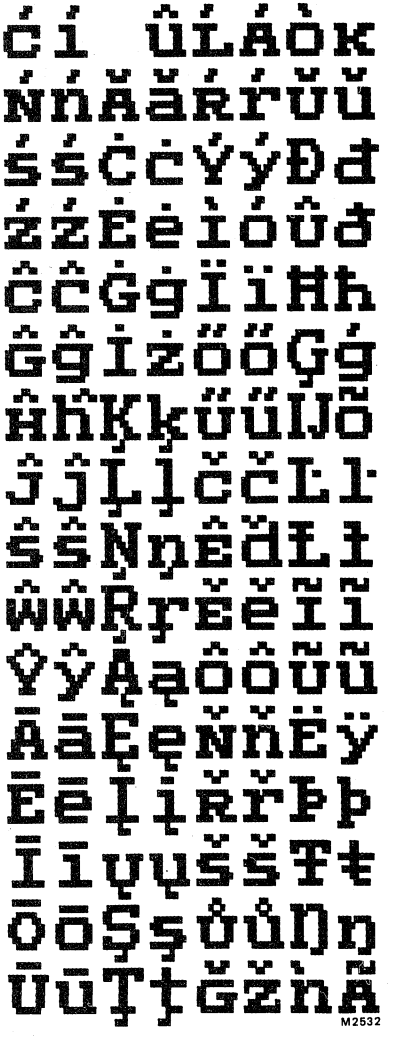
APPLICATION INFORMATION (continued)

Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.

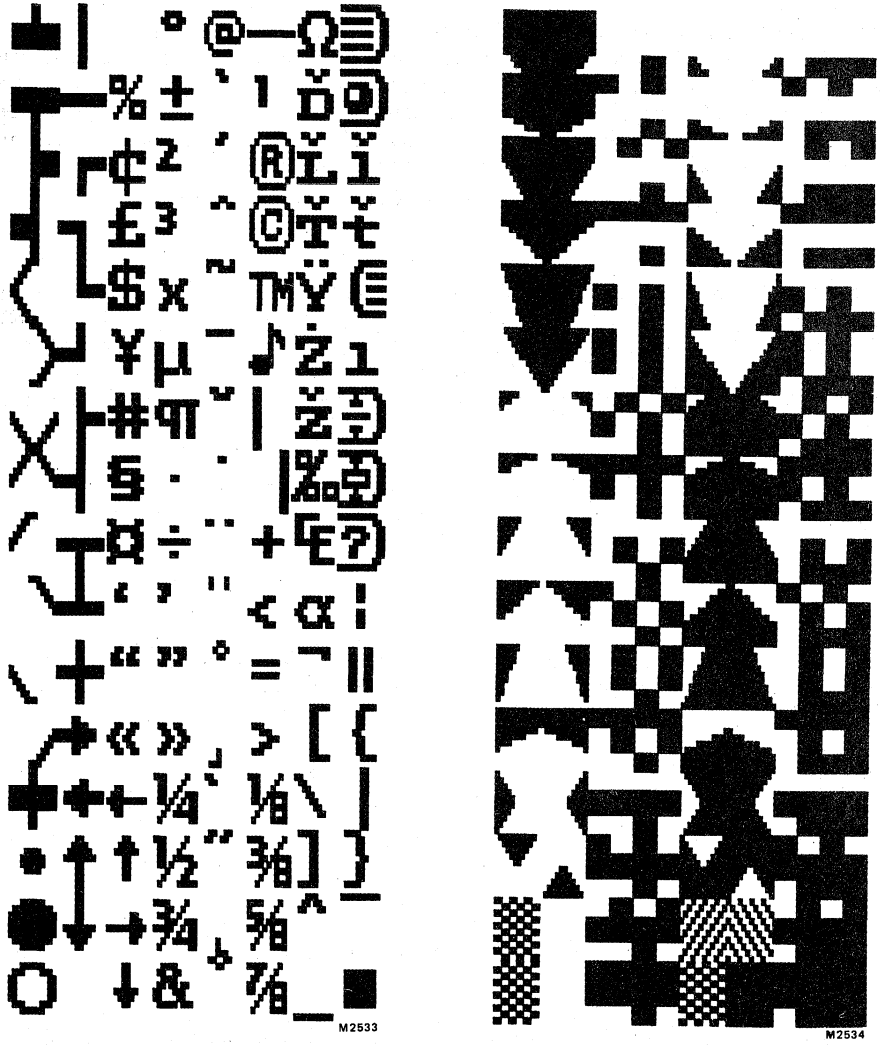


(a)



(b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a) (b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

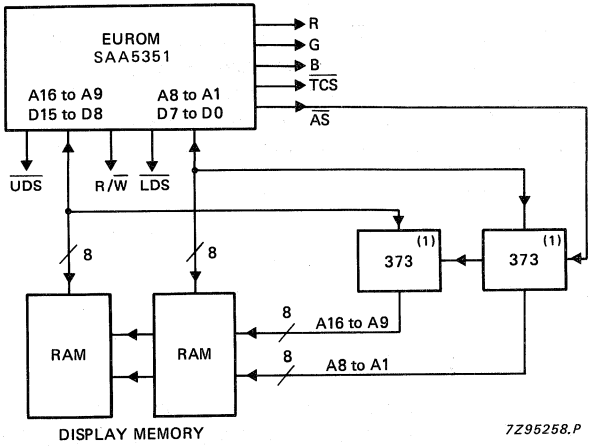
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

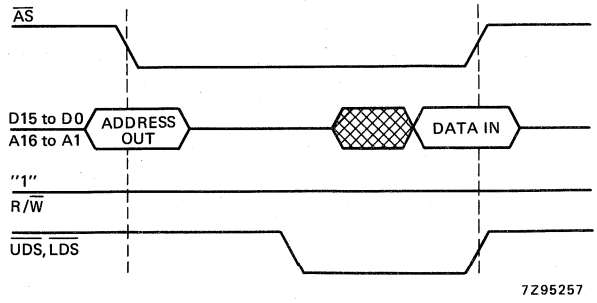


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

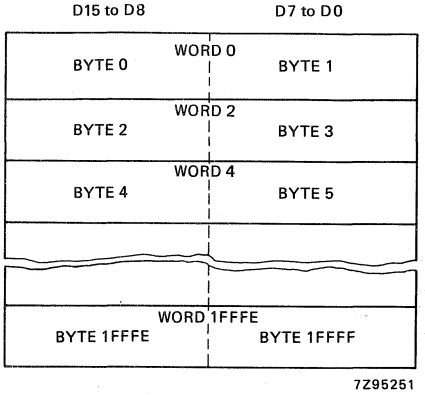


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

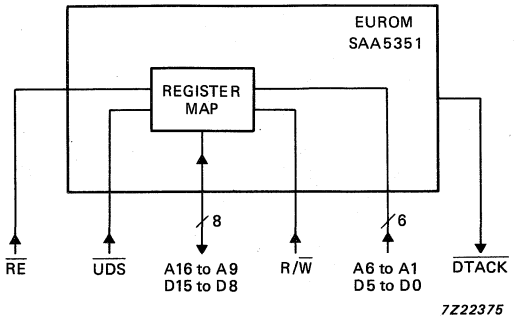


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

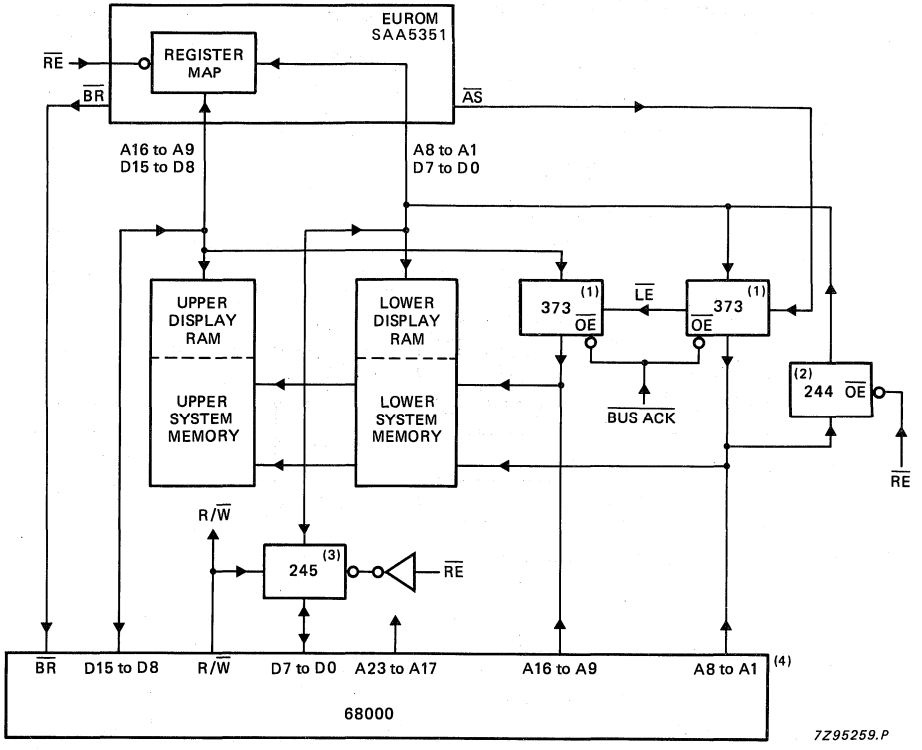
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

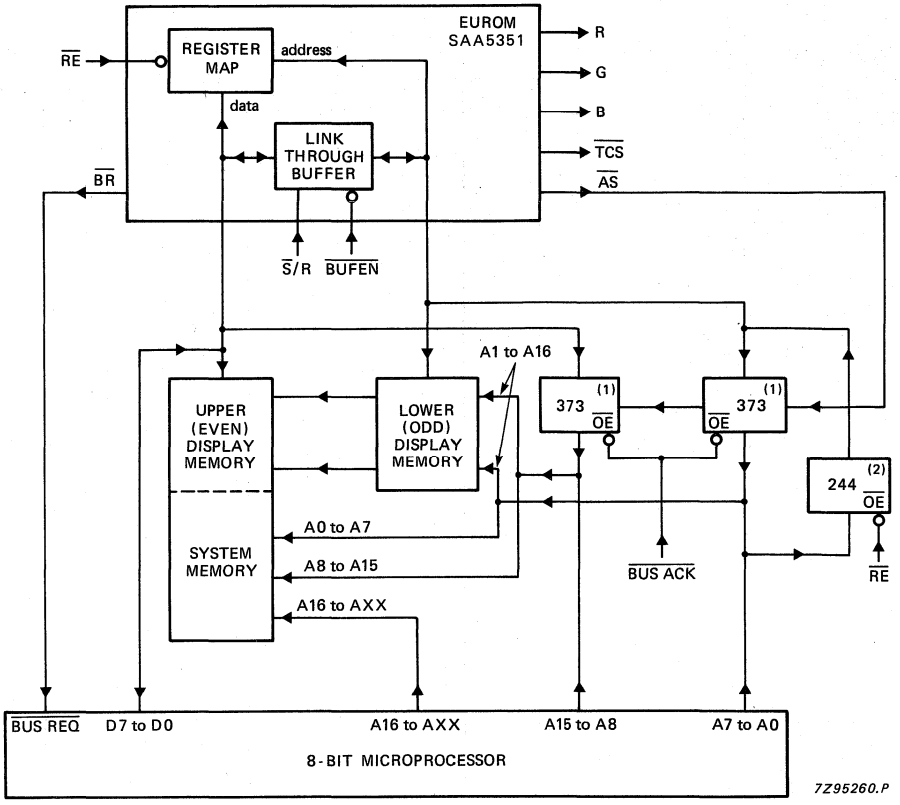
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



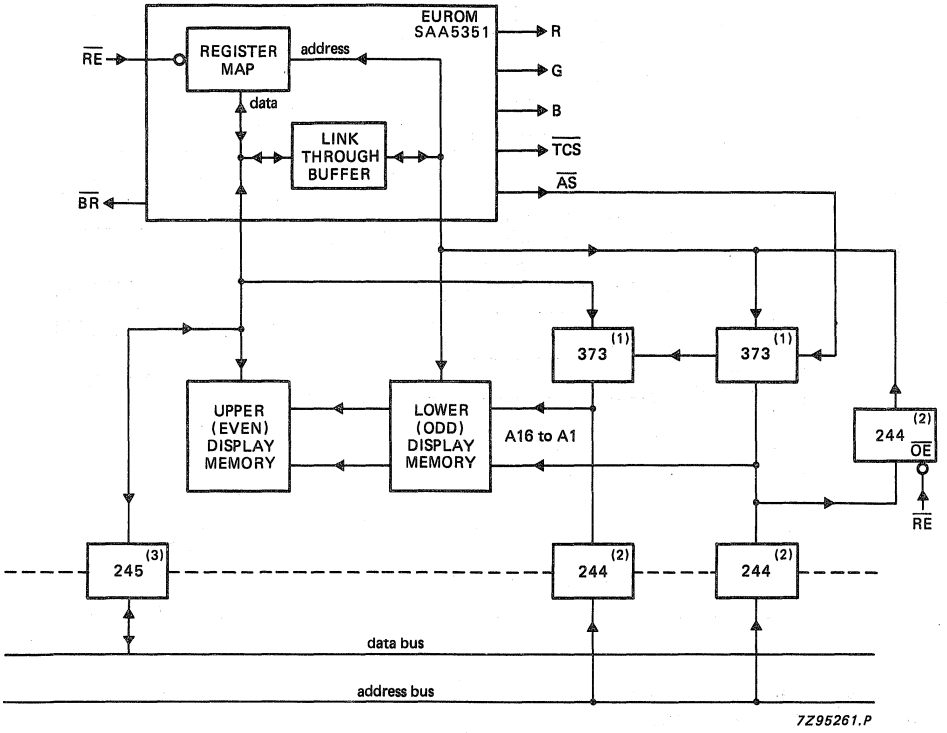
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

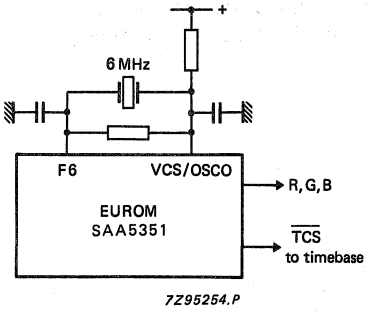


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

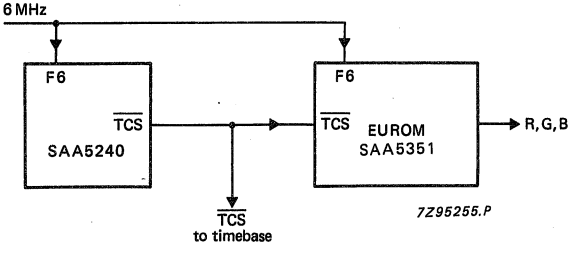


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5231 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

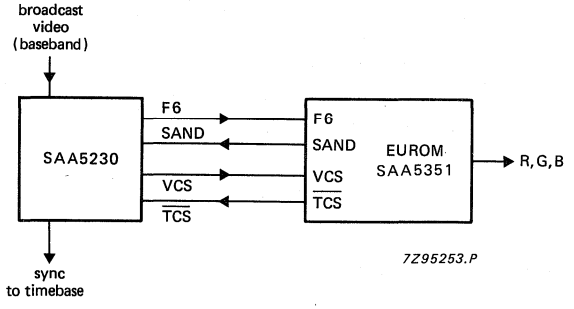


Fig. 26 Phase-locked slave (indirect sync) mode.

SINGLE-CHIP COLOUR CRT CONTROLLER (FTFROM)

GENERAL DESCRIPTION

The SAA5355 FTFROM (Five-Two-Five-ROM) is a single-chip VLSI NMOS crt controller capable of handling the display functions required for a 525-line, level-3 videotex decoder. Only minimal hardware is required to produce a videotex terminal using FTFROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- 32 on-screen colours redefinable from a palette of 4096
- Three on-chip digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. FTFROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6,041957 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing with composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

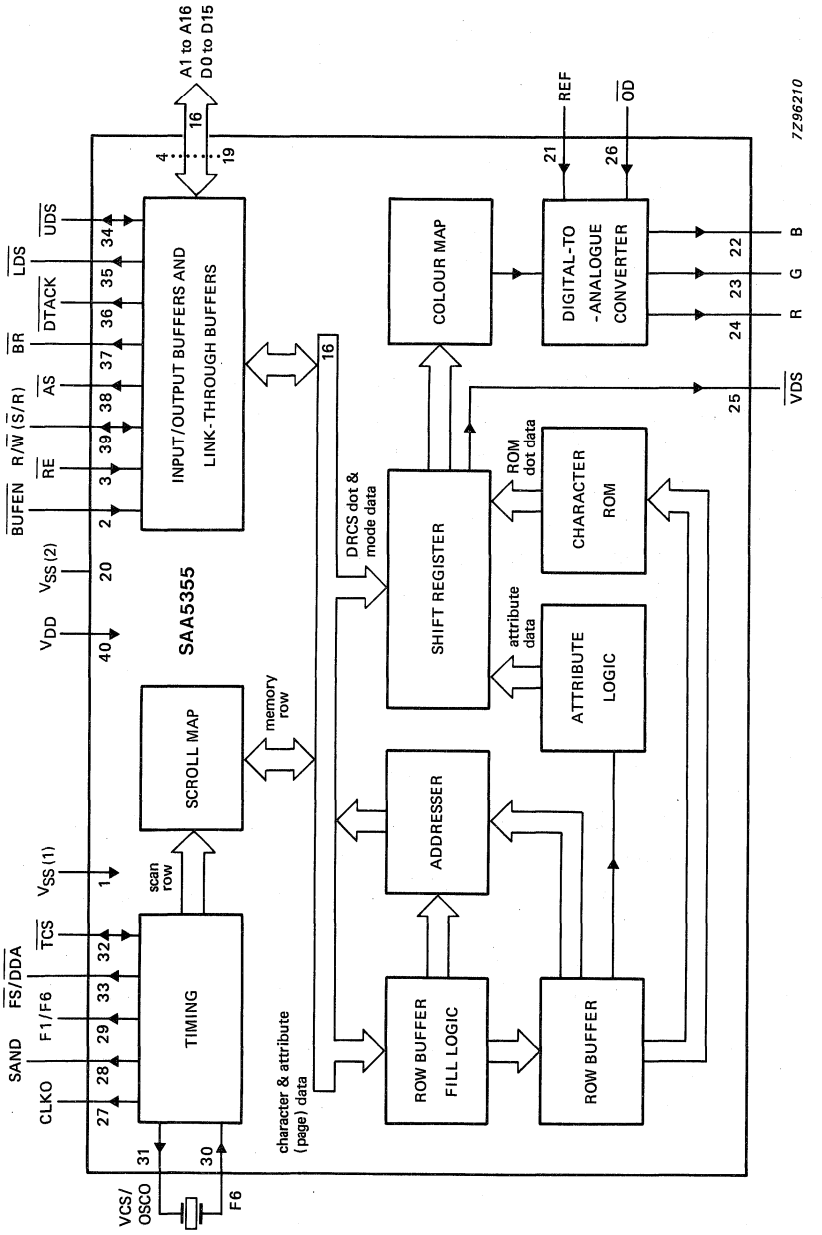


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	$V_{SS(1)}$	Ground (0 V).
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	$V_{SS(2)}$	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3563, TDA3562A).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/F6	1,00699 MHz or 6,041957 MHz output.
30	F6	6,041957 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	$R/\overline{W}$ ($\overline{S}/R$)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

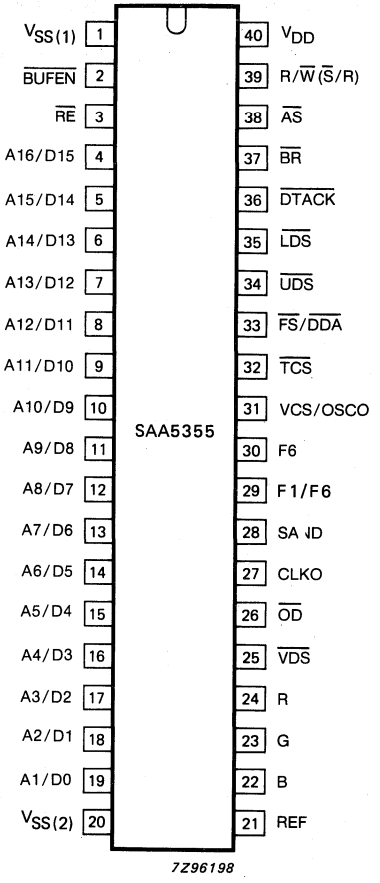


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0,3 to + 7,5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0,3 to + 7,5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0,3 to + 10,0 V
Maximum input voltage (REF)	V_{REF}	−0,3 to + 3,0 V
Maximum output voltage	V_{Omax}	−0,3 to + 7,5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4,75	5,0	5,25	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0,2	–	3,5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7,1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	*	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at V_I = 0 to V_{DD}+0,3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2,7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

DEVELOPMENT DATA

* Value under investigation.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4,2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1,3	2,0	2,7	V
Output voltage low level at I_O = 0,2 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	130	pF
F1/F6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2,7 V	V_{OH}	2,4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0,3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0,4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0,2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2,4	–	6,0	V
Output voltage LOW at $V_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input current at $V_I = 0$ to $V_{DD}+0,3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3,2$ mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	200	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING (note 4)					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5,9	–	6,1	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$ $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 5, 6 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	25	–	–	ns
CLKO LOW time	t_{CLKL}	15	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{UOD}	0	–	60	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{DCH}	10	–	60	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 7)	t_{F1H}	–	500	–	ns
F1 LOW time (note 7)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	275	ns
Link-through buffers (notes 8, 9 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from FTFROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	40	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	250	–	350	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to FTFROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	75	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. All timings are related to a 6,00 MHz clock.
5. CLKO, R, G, B, F1/F6, $\overline{VDS}$: C_L = 25 pF.
   $\overline{FS}$/$\overline{DDA}$: C_L = 50 pF
6. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0,8 to 2,0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2,7 V
7. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
8. C_L = 150 pF.
9. Reference levels = 0,8 to 2,0 V.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will than depend on the internal synchronization time.

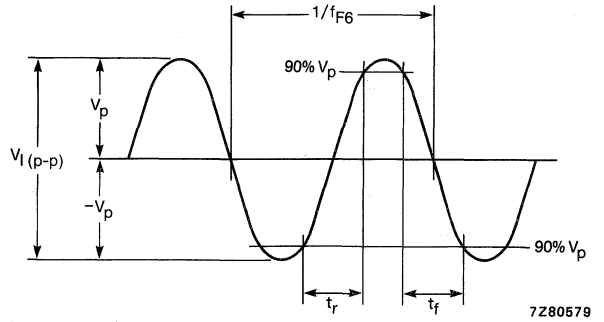
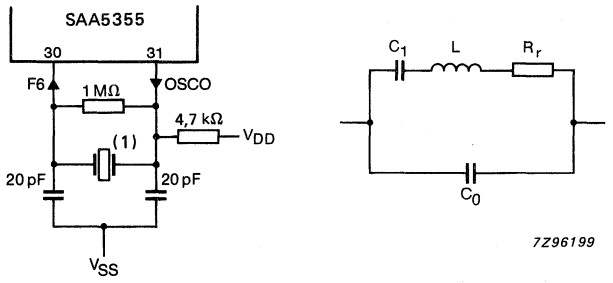


Fig. 3 F6 input waveform.



(1) for 525-line operation, frequency = 6,041957 MHz.

Fig. 4(a) Oscillator circuit for SAA5355 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

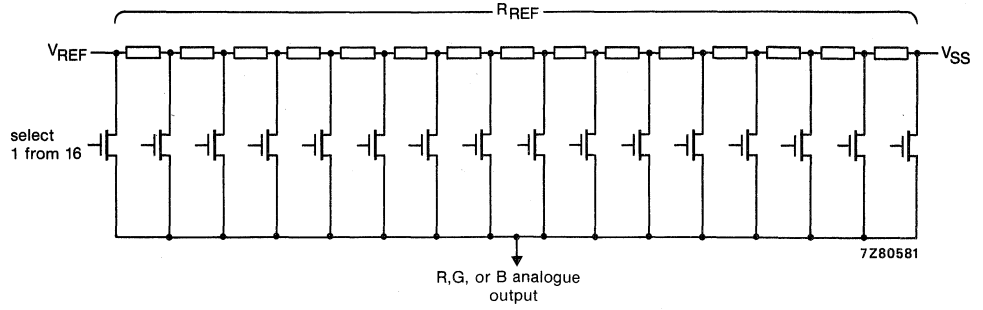


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

DEVELOPMENT DATA

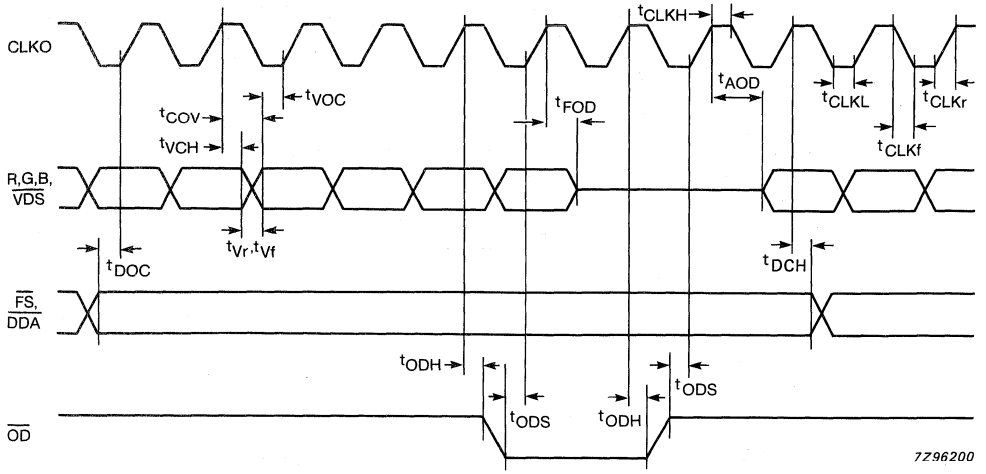


Fig. 6 Video timing.

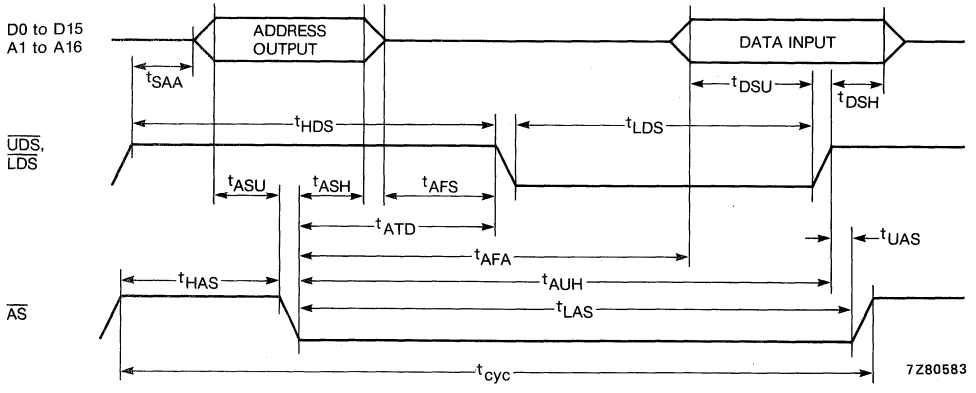


Fig. 7 Memory access timing.

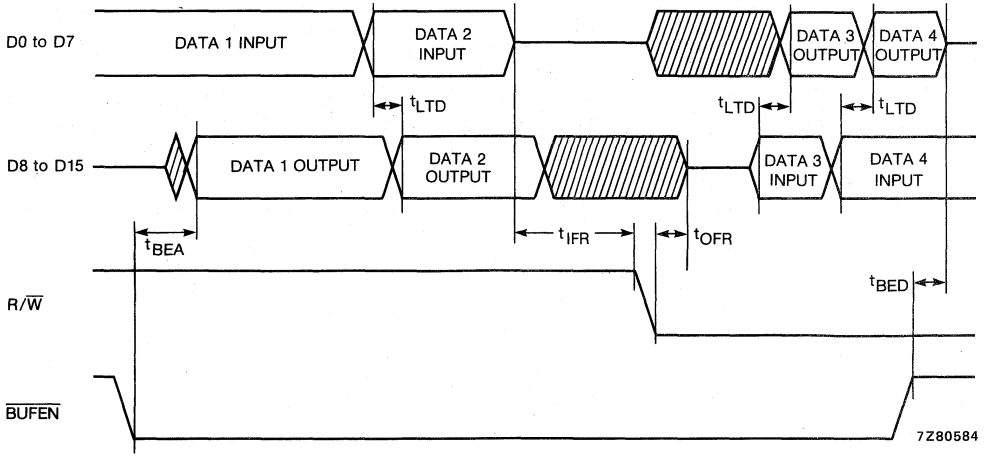


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

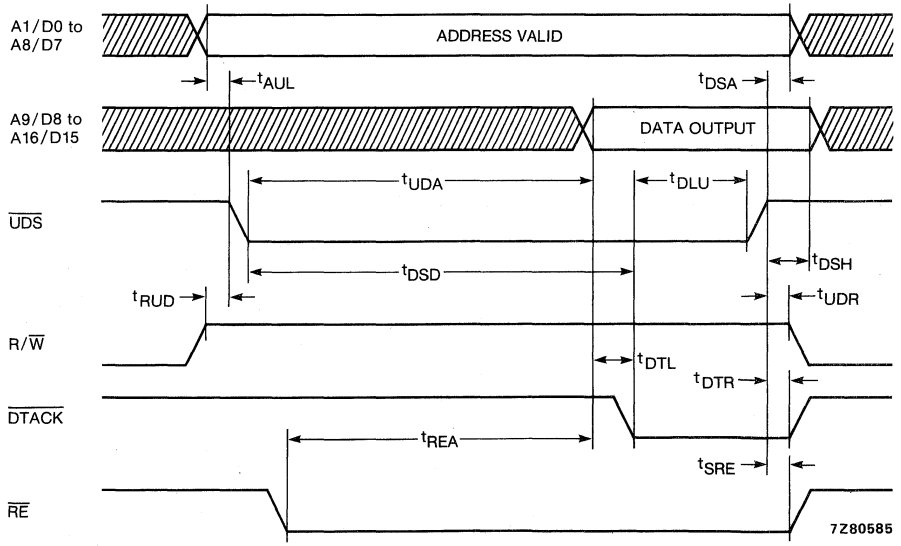


Fig. 9 Timing of microprocessor read from FTFROM.

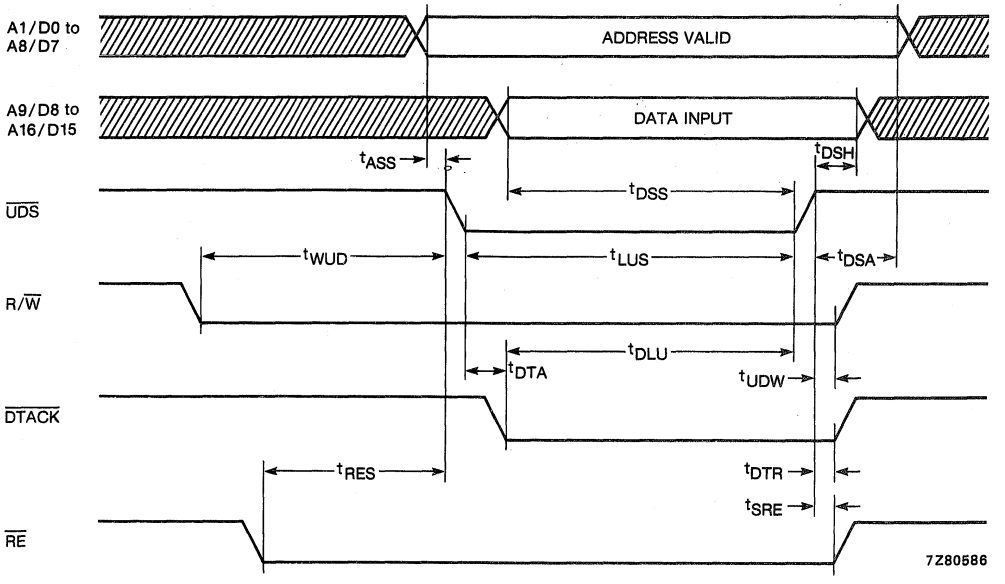


Fig. 10 Timing of microprocessor write to FTFROM.

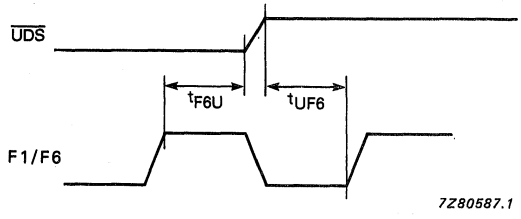


Fig. 11 Timing of F1/F6 to memory access cycle.

DEVELOPMENT DATA

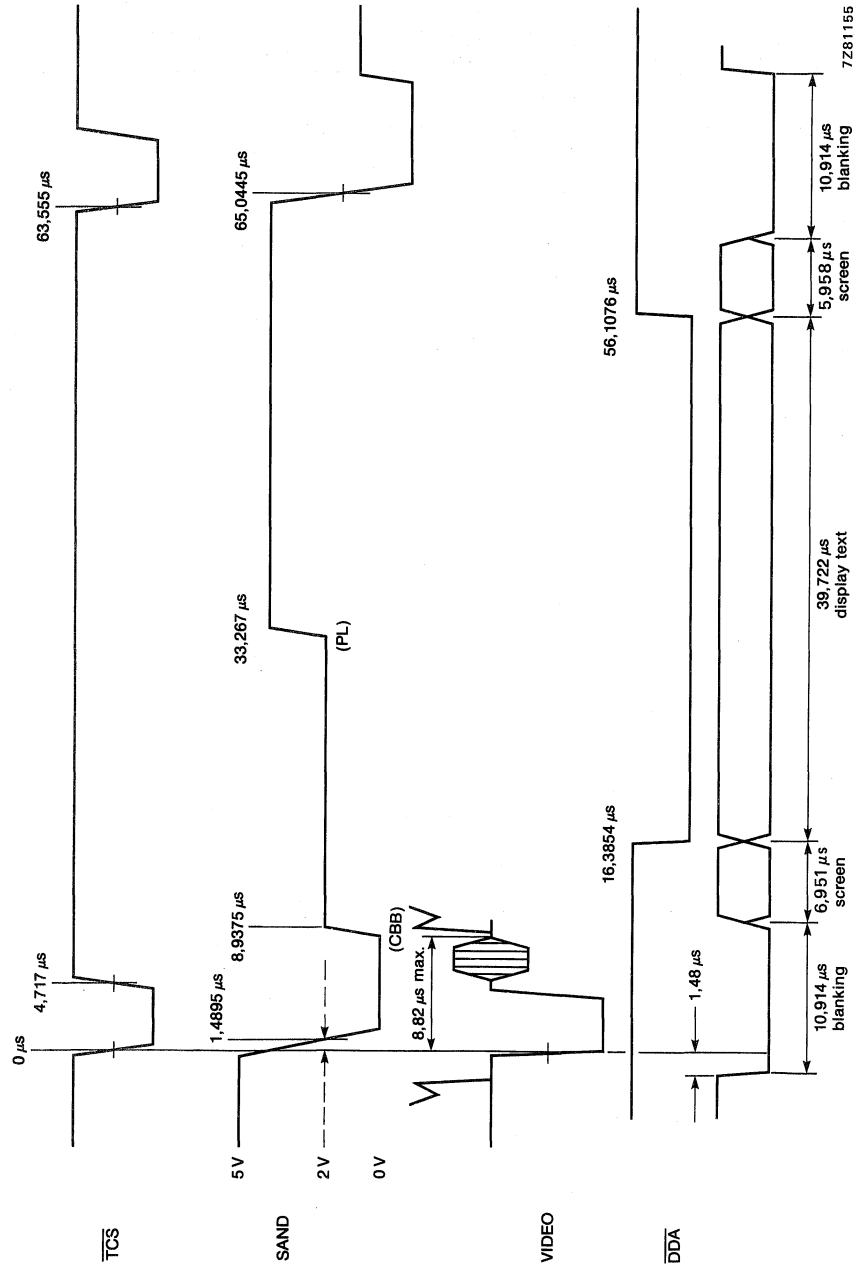


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume $f_{F6} = 6{,}041957$ MHz.

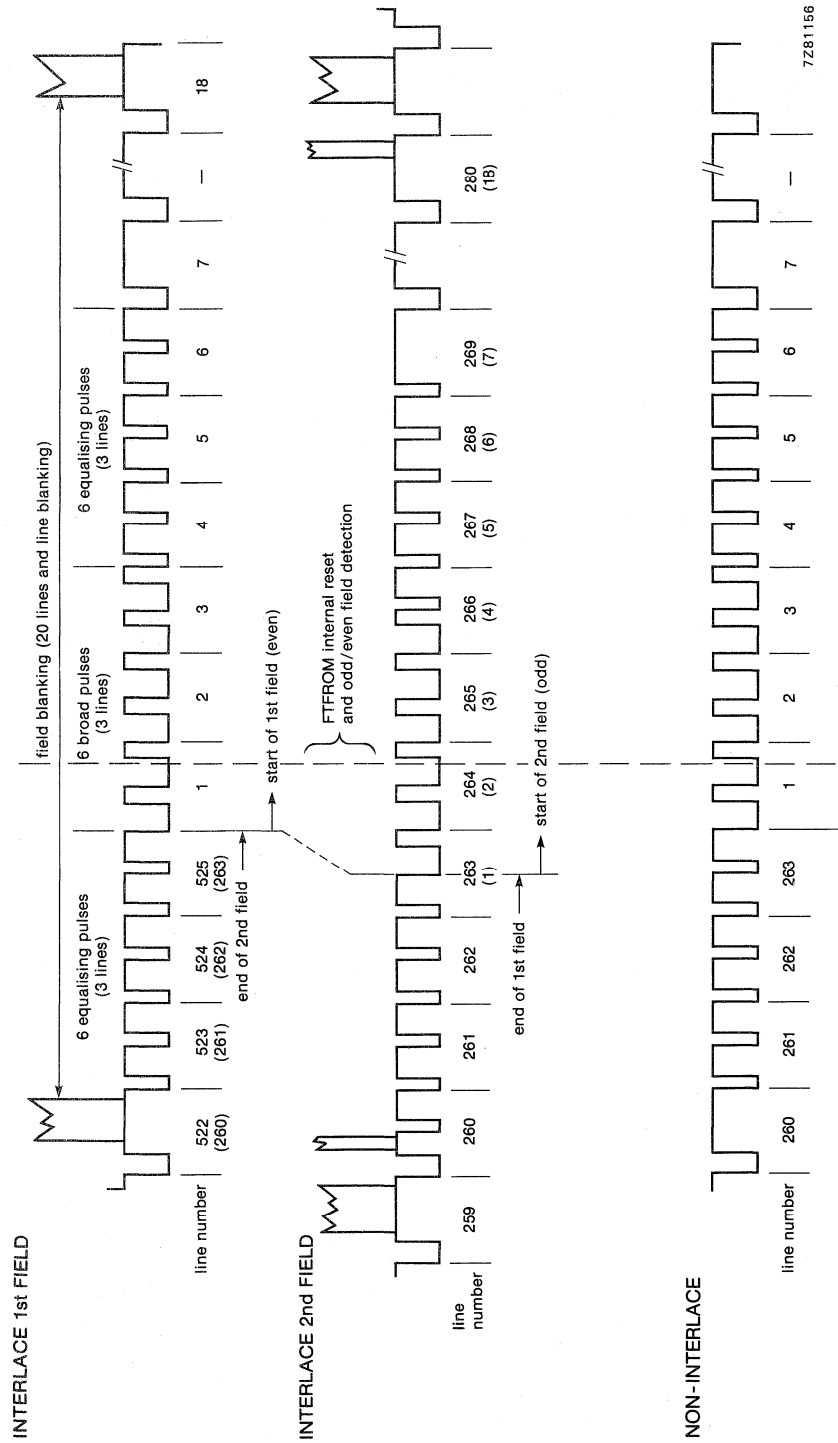


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4,717 μs; equalizing pulse widths = 2,23 μs.

DEVELOPMENT DATA

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

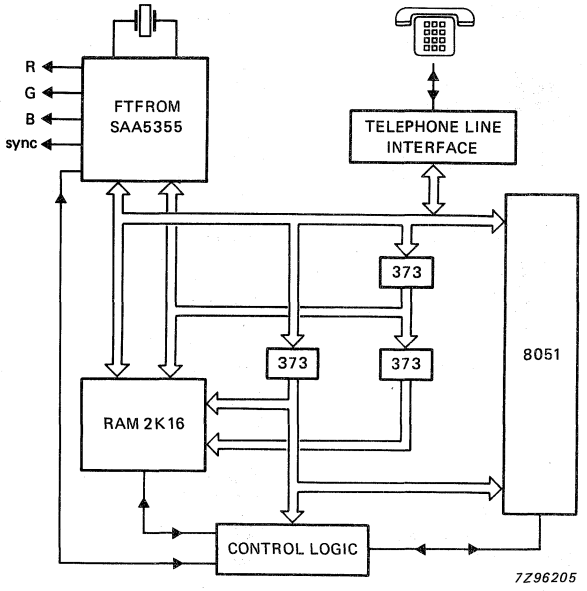


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

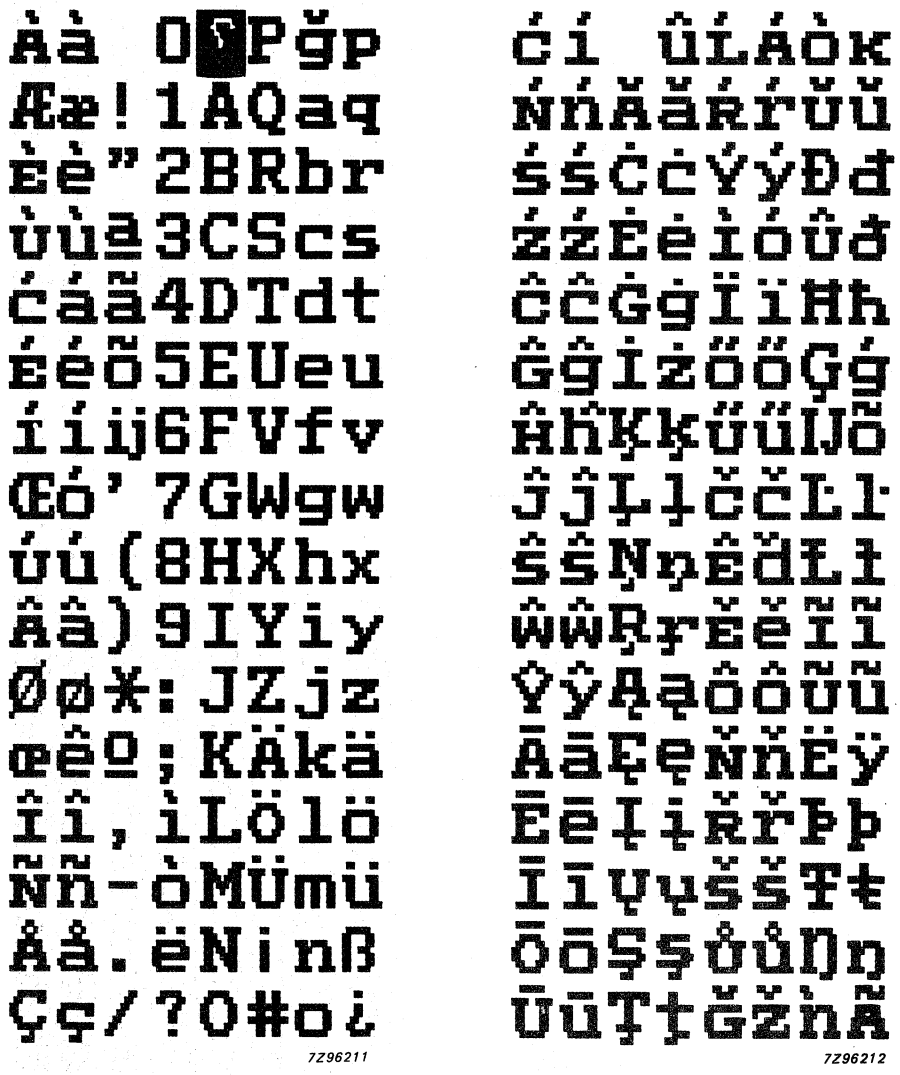
The timing chain operates from an external 6,041957 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 20/21 rows per page and 10 video lines per row. FTFROM will also operate with 25 rows per page and 9 video lines per row.

The display is generated to the normal 525-line/59,94 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at approximately 1 MHz or 6 MHz (pin 29) is available for driving other devices, and a clock output (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

APPLICATION INFORMATION (continued)

Character generation

FTFROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The fixed character tables (Tables 0 to 3), shown in Figs 15 and 16, are applicable to 10-lines-per-row applications. For 9 lines per row applications, the characters will be as shown but with the last line removed from alpha characters and line 5 (labelling 0 to 9) removed from mosaic and line drawing characters.



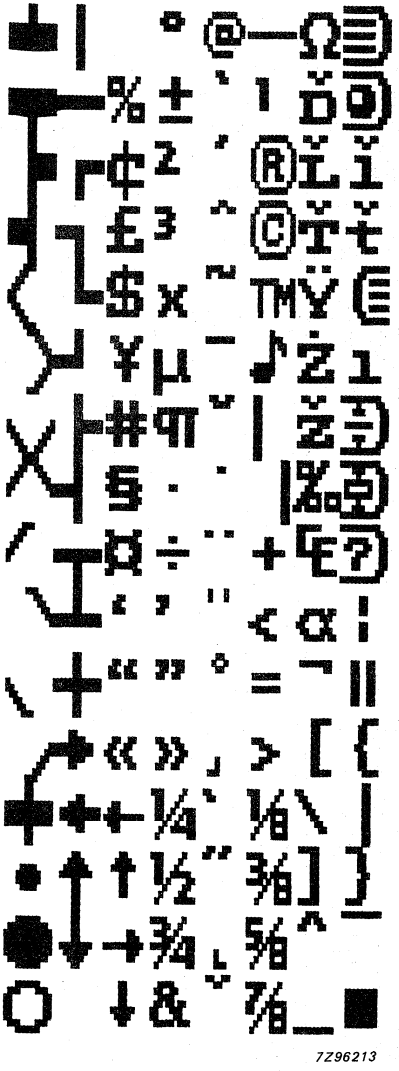
7Z96211

(a)

7Z96212

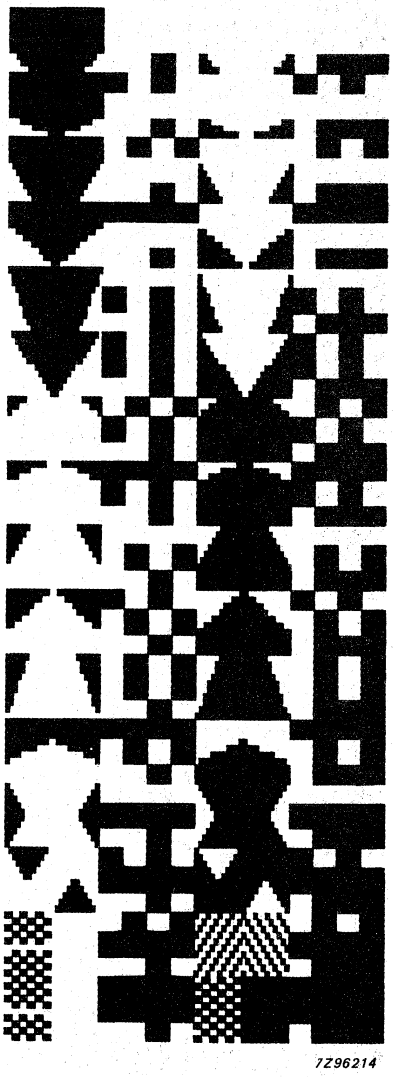
(b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



7Z96213

(a)



7Z96214

(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

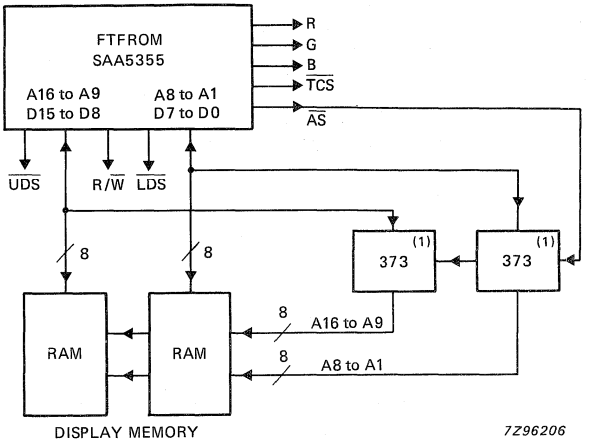
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- FTFROM fetches data from the display memory
- The microprocessor reads from, or writes to, FTFROM's internal register map
- The microprocessor accesses the display memory

FTFROM access to display memory (Figs 17 and 18)

FTFROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 496,5 ns (F6 = 6,041957 MHz). The address strobe ($\overline{AS}$) signal from FTFROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although FTFROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

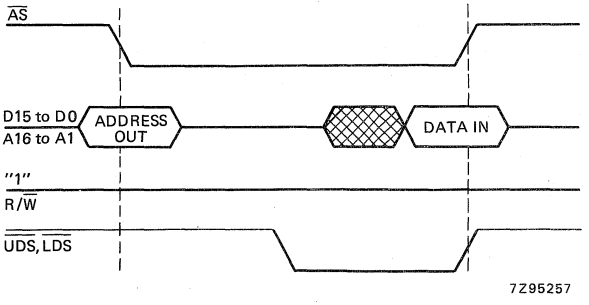


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

FTFROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

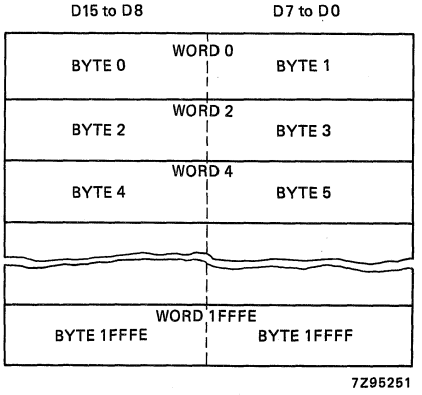


Fig. 19 Display memory word/byte organization.

Warning time

As FTFROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by FTFROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and FTFROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that FTFROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of FTFROM's bus activity is programmable to be between 0 and 22,84 μs.

Microprocessor access to register map

FTFROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

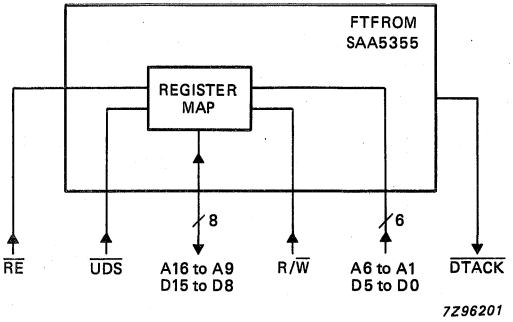


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to FTFROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

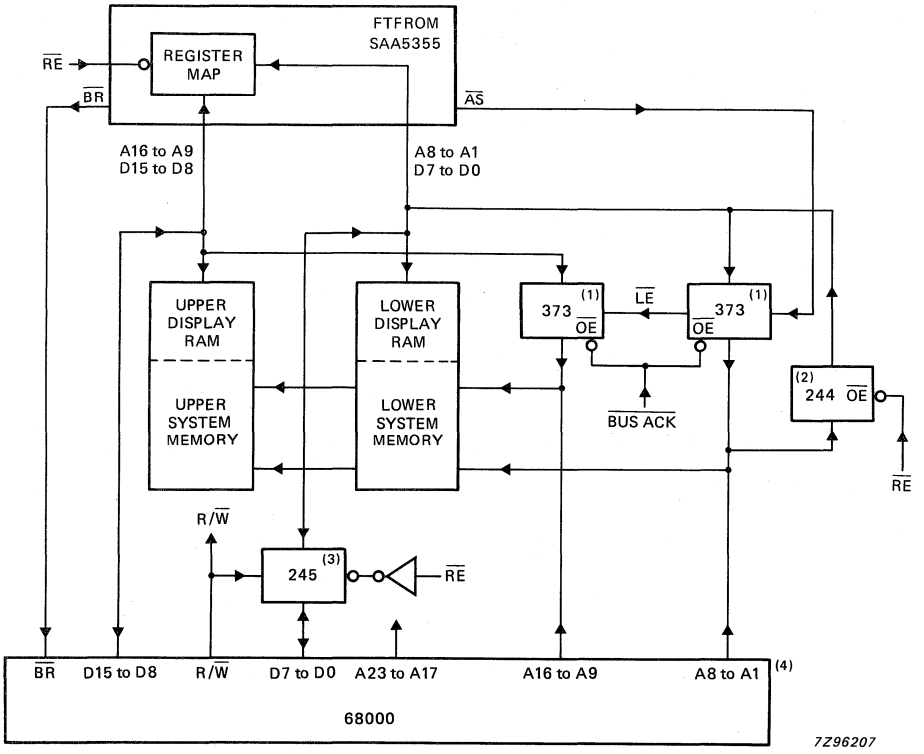
The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by FTFROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of FTFROM's scroll map contents at a location in its main memory.

8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, FTFROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by FTFROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

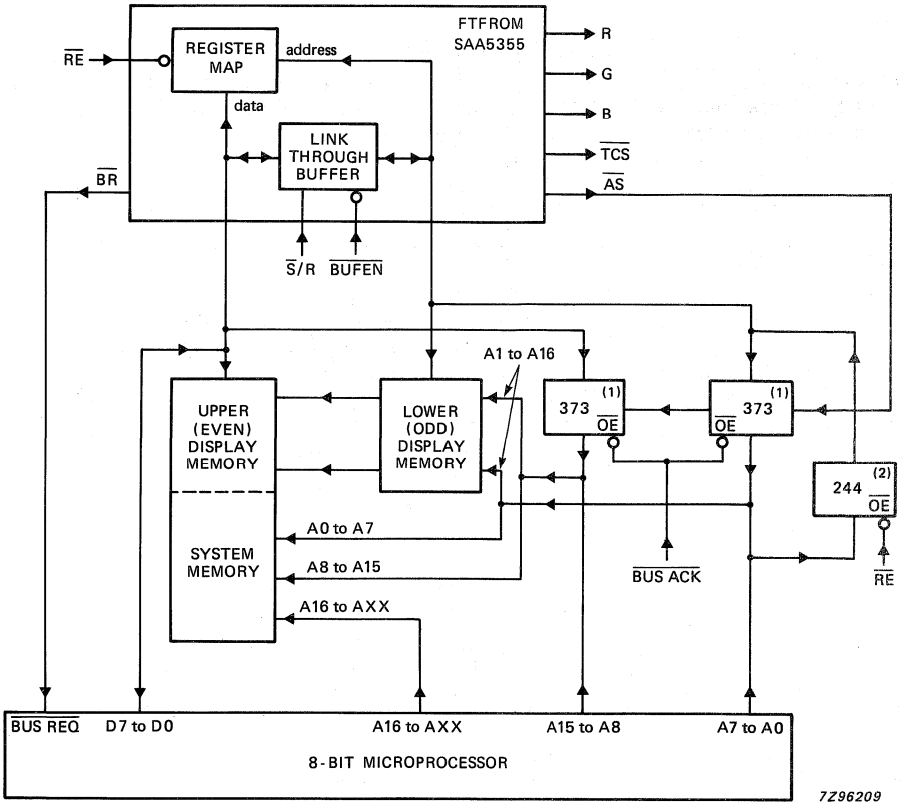
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



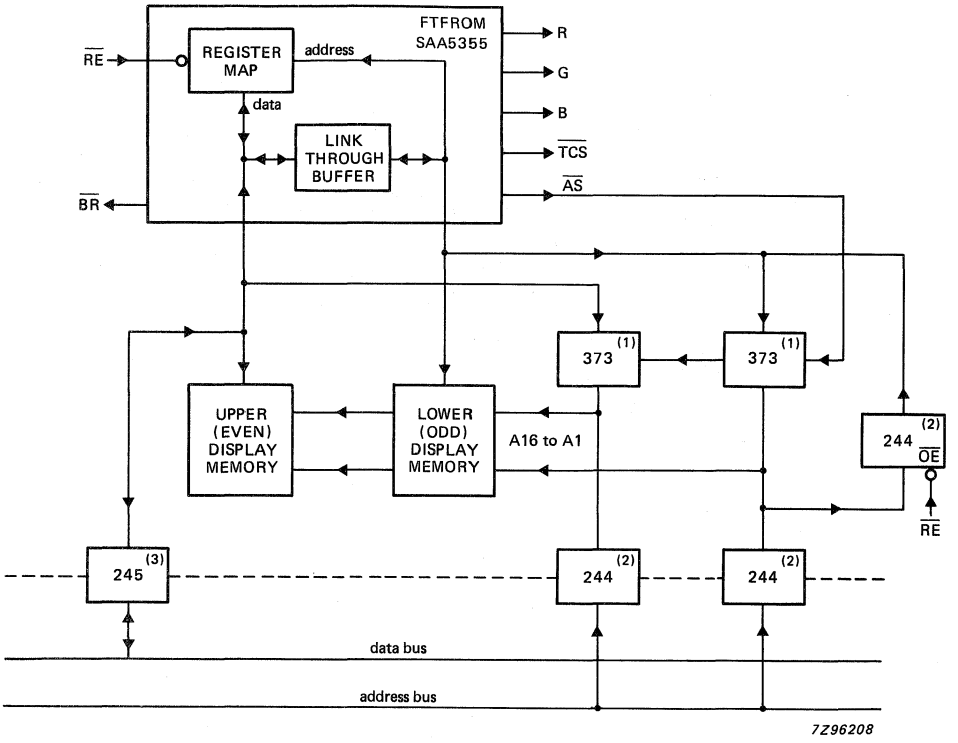
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect FTFROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses FTFROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) FTFROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6,041957 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

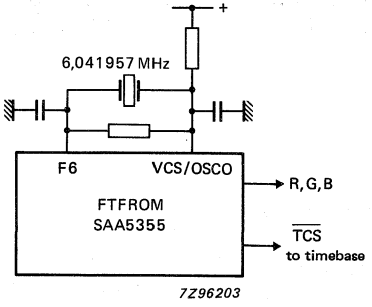


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode FTFROM synchronizes directly to another device as shown in Fig. 25. FTFROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using FTFROM's internal field sync separator.

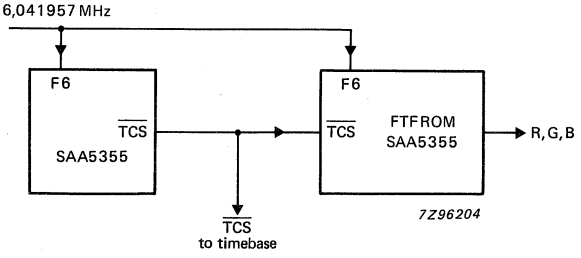


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When FTFROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to FTFROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from FTFROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

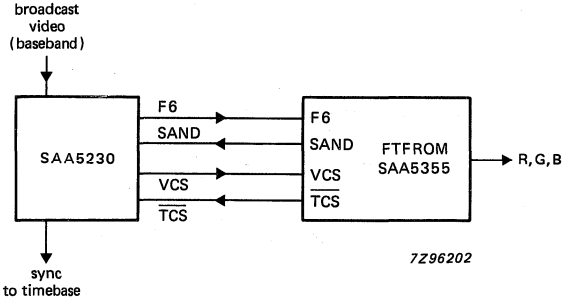


Fig. 26 Phase-locked slave (indirect sync) mode.

EUROM 60 Hz

GENERAL DESCRIPTION

The SAA5361 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM (4096 locations) and three on-chip digital-to-analogue converters allow 32 colours on-screen
- On-chip digital-to-analogue converters are non-linear to compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 7.2 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

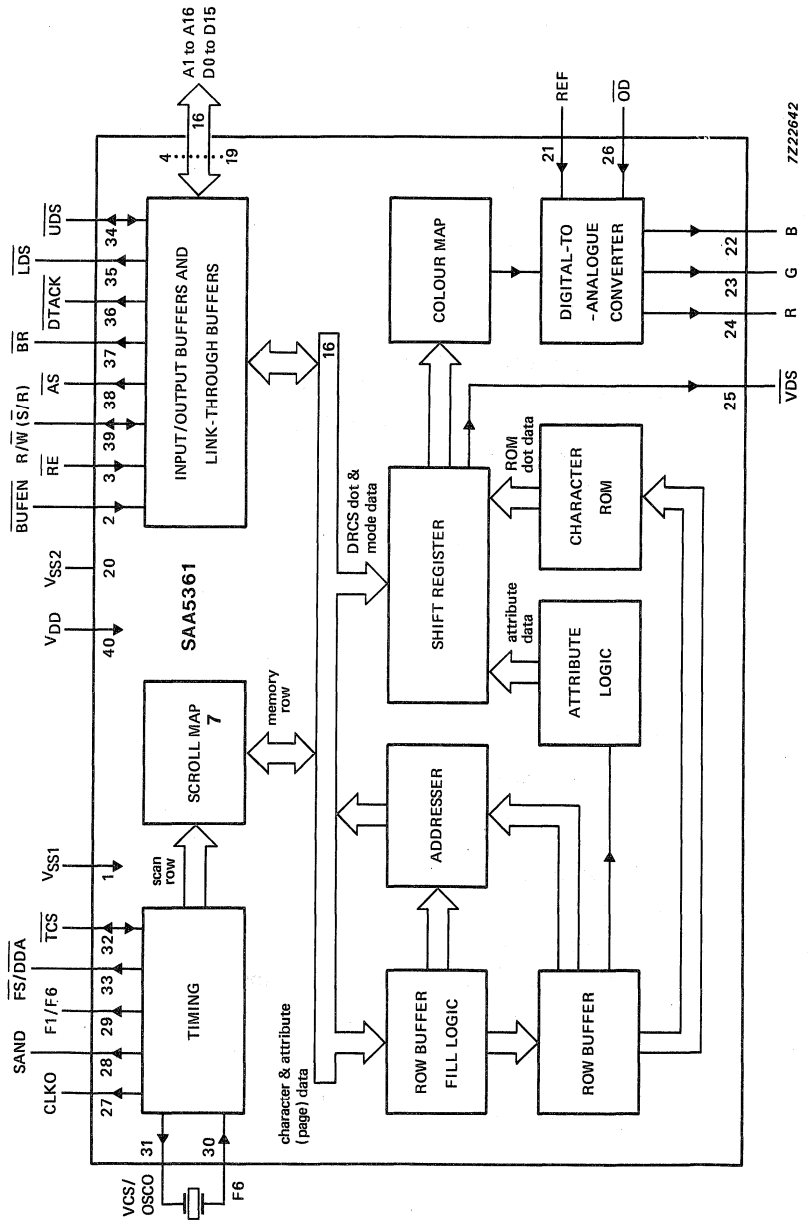


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

1	V_{SS1}	Ground 0 V.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS2}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs.
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	14.4 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback to other circuit, when display must be locked to a VLP. The phase-lock part of the sandcastle waveform can be disabled.
29	F1/F6	1.2 MHz or 7.2 MHz output.
30	F6	7.2 MHz clock input. Internal AC coupling is provided.
31	VCS/OSCO	Video composite sync input for phase reference of vertical display timing when locking to a video source or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}/\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	$\overline{DTACK}$	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	$R/\overline{W}$ ($\overline{S}/R$)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

PINNING (continued)

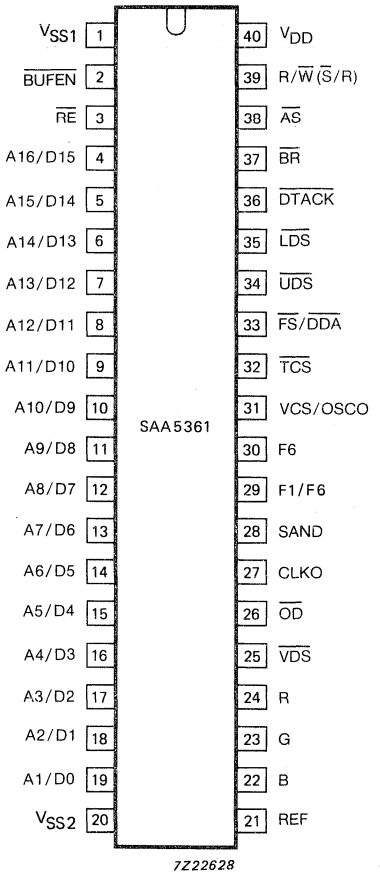


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0.3 to +7.5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0.3 to +7.5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0.3 to +10.0 V
Maximum input voltage (REF)	V_{REF}	−0.3 to +3.0 V
Maximum output voltage	V_{Omax}	−0.3 to +7.5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	0 to +60 °C
Storage temperature range	T_{stg}	−55 to +125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 5%; V_{SS} = 0 V; T_{amb} = 0 to +60 °C, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4.75	5.0	5.25	V
Supply current (pin 40)	I_{DD}	–	–	390	mA
INPUTS					
F6					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.5	3.0	7.0	V
Input leakage current at V_I = 0 to $V_{CC\,max}$; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7.1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.5	V
Input leakage current at V_I = 0 to V_{DD}+ 0.3 V; T_{amb} = 25 °C	I_{IL}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2.7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −10 μA	V_{OH}	4.2	–	V_{DD}	V
Output voltage intermediate level at I_O = −10 to + 10 μA	V_{OI}	1.3	–	2.7	V
Output voltage low level at I_O = 0.2 mA	V_{OL}	0	–	0.2	V
Load capacitance (note 1)	C_L	–	–	130	pF
F1/F6, $\overline{DDA}$/$\overline{FS}$					
Output voltage HIGH	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{LDS}$, $\overline{AS}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{DTACK}$, $\overline{BR}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2.7 V	V_{OH}	2.4	–	–	V
Output voltage LOW at I_{OL} = 2 mA (note 10)	V_{OL}	–	–	0.4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0.3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA
CLOCKO					
Output voltage HIGH	V_{OH}	2.0		V_{DD}	V
Output voltage LOW	V_{OL}	0		0.8	V
Load capacitance (note 1)	C_L	–		50	pF

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW	V_{OL}	0	–	0.8	V
Output leakage current (OFF state) at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
INPUTS/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Output leakage current (output OFF) at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Load capacitance (note 1)	C_L	–	–	50	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input voltage LOW	V_{IL}	0	–	1.5	V
Output leakage current at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 to 100 μA	V_{OH}	2.0	–	6.0	V
Output voltage LOW at V_{OL} = 3.2 mA	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	50	pF
A1/D0 to A16/D15					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Output leakage current V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance (note 1)	C_L	–	–	200	pF
$\overline{UDS}$; R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Output leakage current at V_I = 0 to V_{DD} + 0.3 V; T_{amb} = 25 °C	I_{LO}	−10	–	+ 10	μA
Input capacitance	C_{IN}	–	–	10	pF
Output voltage HIGH (I_{OH} = −200 μA)	V_{OH}	2.0	–	V_{DD}	V
Output voltage LOW (I_{OH} = 3.2 mA)	V_{OL}	0	–	0.8	V
Load capacitance (note 1)	C_L	–	–	200	pF

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Values guaranteed at 0.8 V and 2.0 V levels F6 input frequency at 7.2 MHz					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	69	ns
Frequency	f_{F6}	–	72	–	MHz
CLKO, F1/F6, R, G, B, $\overline{VDS}$, $\overline{FS}$/DDA, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	20	–	–	ns
CLKO LOW time	t_{CLKL}	12	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	– –	– –	10 10	ns ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	0	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	60	ns
F1 HIGH time (note 5)	t_{F1H}	333	417	500	ns
F1 LOW time (note 5)	t_{F1L}	333	417	500	ns
F6 HIGH time	t_{F6H}	33	69	100	ns
F6 LOW time	t_{F6L}	33	69	100	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING					
(notes 1, 6, 7 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	417	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	65	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	16	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	16	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	42	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	180	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time (note 9)	t_{LDS}	160	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	100	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	240	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	25	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	15	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	225	ns
Link-through buffers (notes 6, 7 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	85	ns
Link-through delay time	t_{LTD}	–	–	70	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	50	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	50	ns
Microprocessor READ from EUROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	0	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	8	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	–	–	260	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 8)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/F6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/F6) rise (notes 1, 6 and 7)	t_{UF6}	20	–	–	ns
F6 (component of F1/F6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS}$/$\overline{DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. All pins are tested with a 150 pF load capacitor.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, F1/F6, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$: reference levels = 0.8 to 2.0 V.
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2.7 V.
5. These times may momentarily be reduced to a nominal 69 ns in slave-sync mode at the moment of re-synchronization.
6. Reference levels = 0.8 to 2.0 V.
7. F6 input at 6 MHz.
8. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time
9. This timing may be infringed at the beginning and end of the memory access window.
10. Output voltage guaranteed when programmed for bottom level.

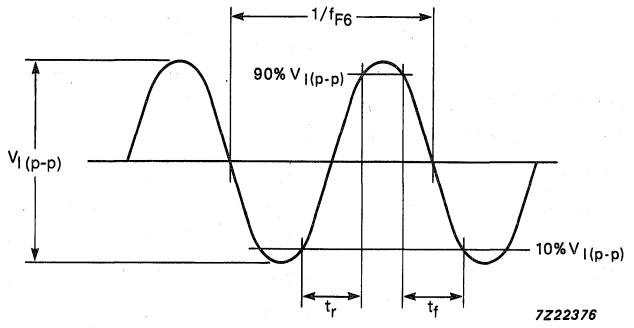


Fig. 3 F6 input waveform.

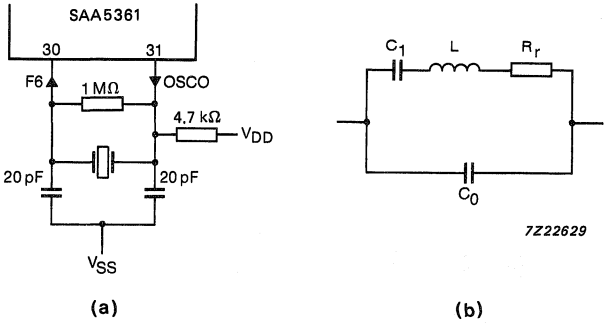


Fig. 4(a) Oscillator circuit for SAA5361 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

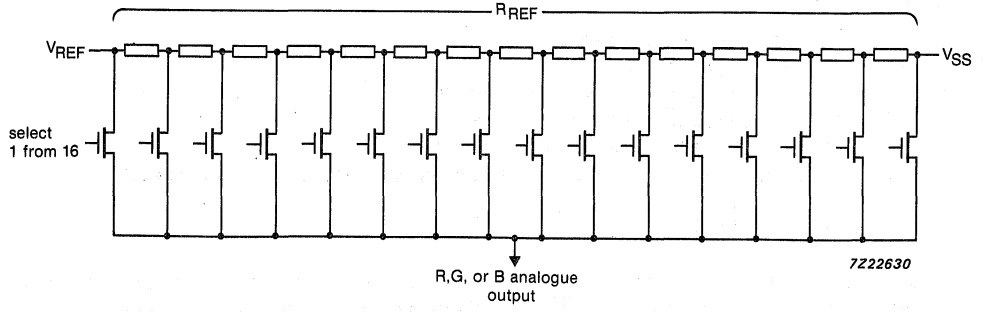


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

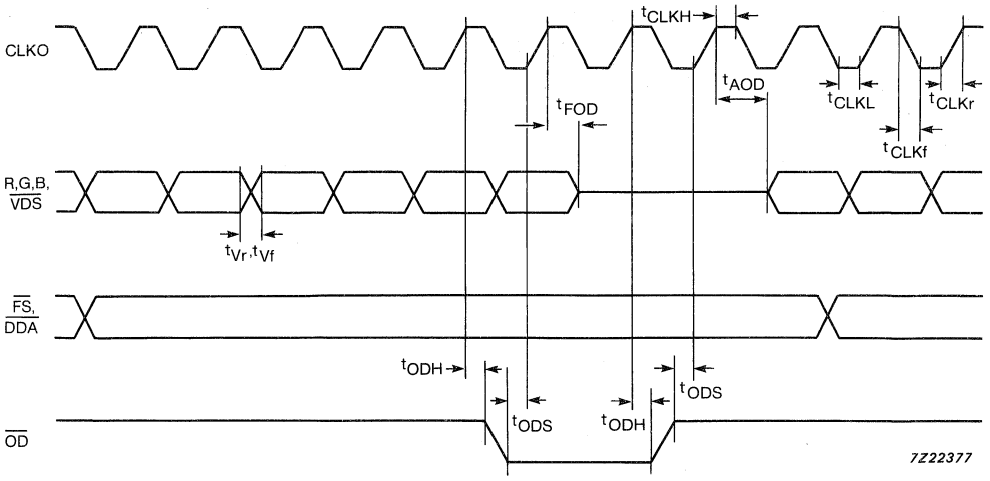


Fig. 6 Video timing.

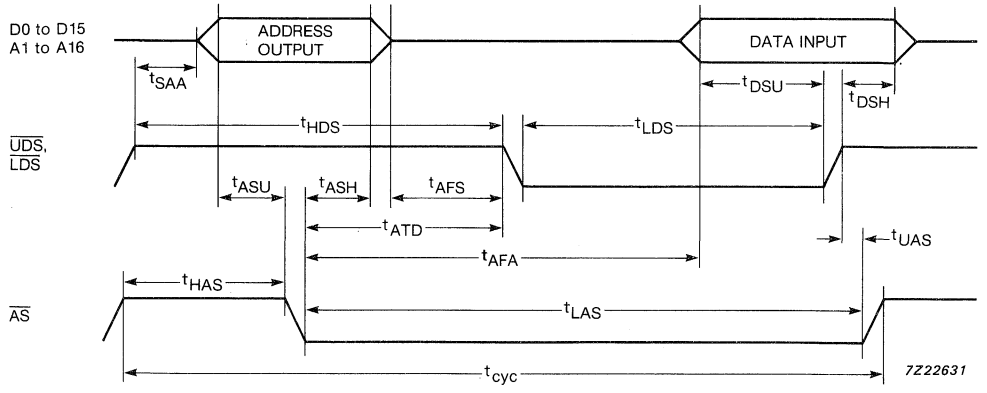


Fig. 7 Memory access timing.

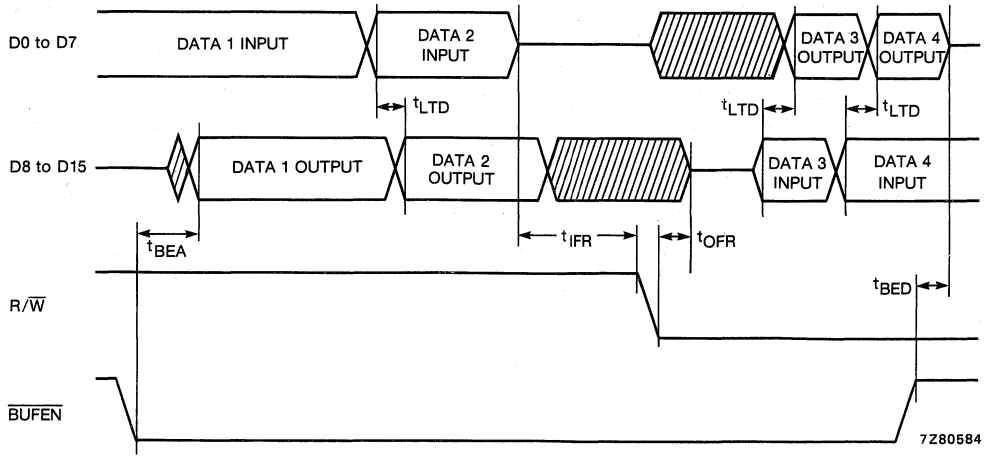


Fig. 8 Timing of link-through buffers.

DEVELOPMENT DATA

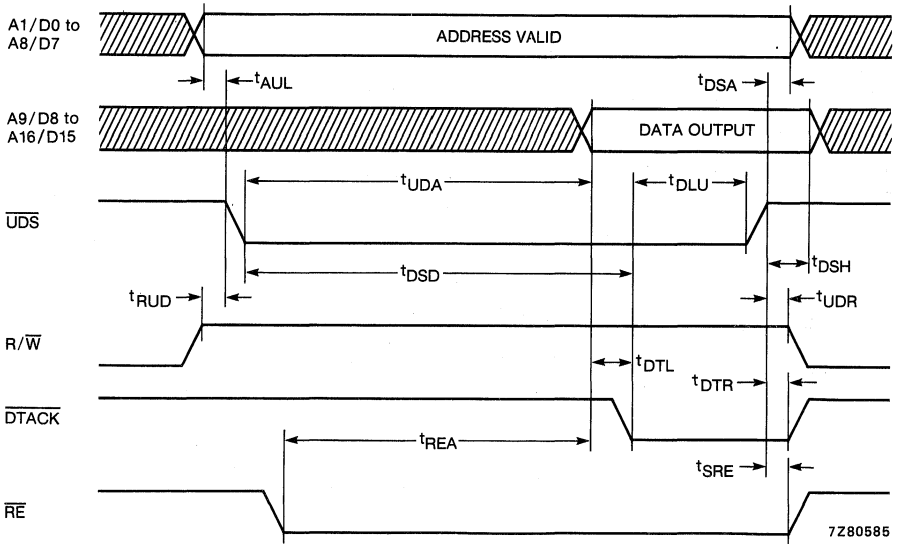


Fig. 9 Timing of microprocessor read from EUROM.

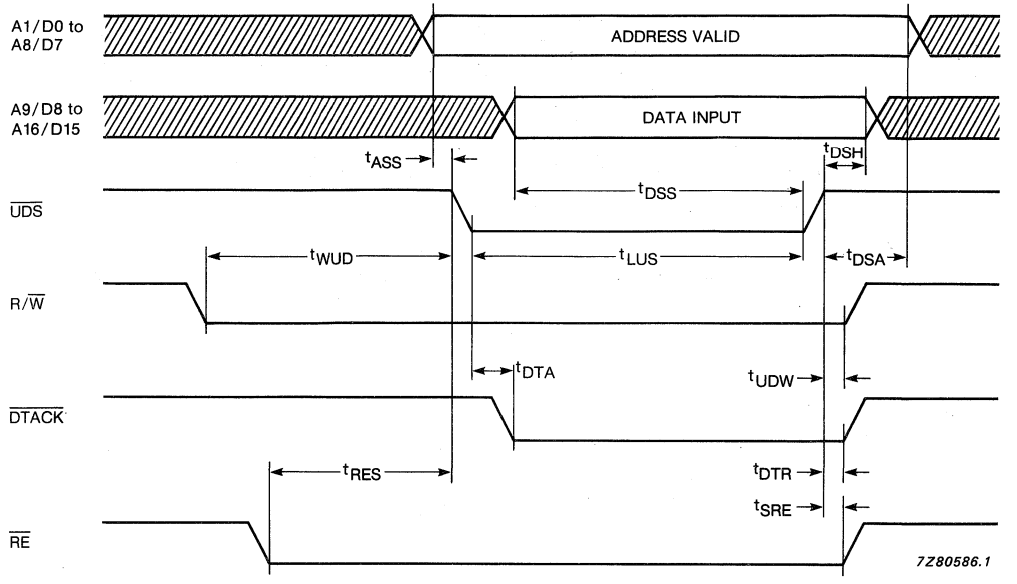


Fig. 10 Timing of microprocessor write to EUROM.

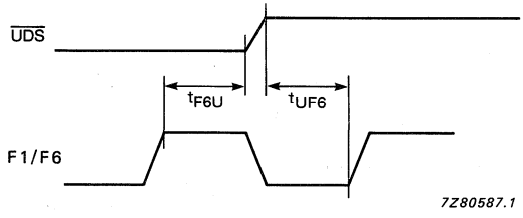


Fig. 11 Timing of F1/F6 to memory access cycle.

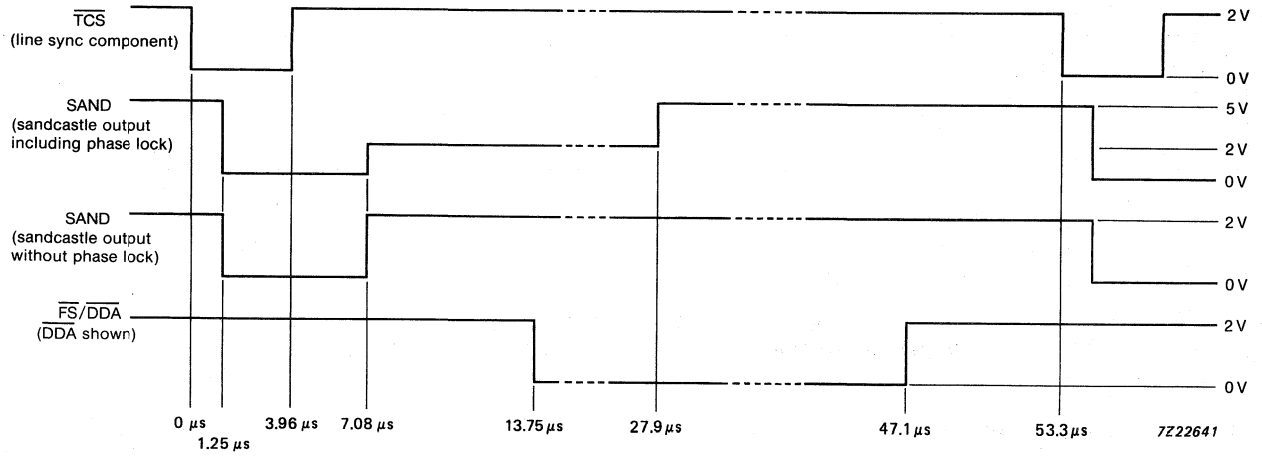


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 7.2 MHz.

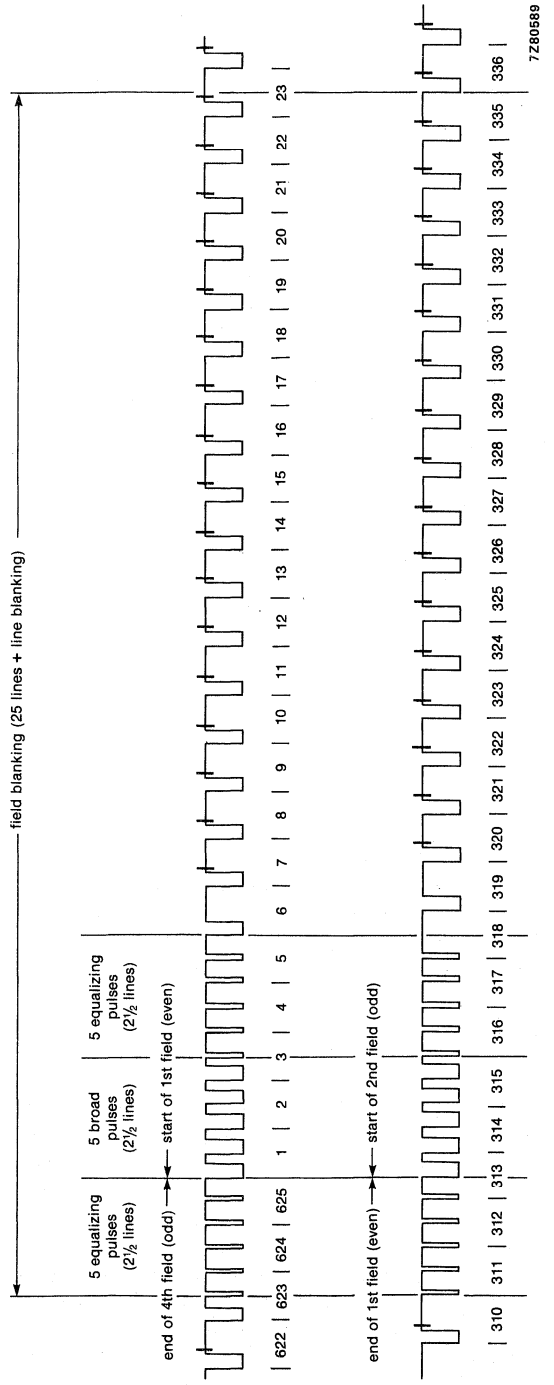


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 3.96 μs; equalizing pulse widths = 7.88 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

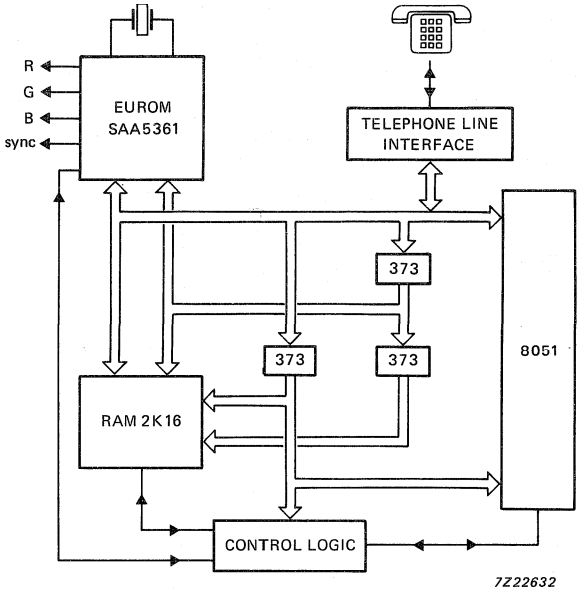


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows – each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 7.2 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

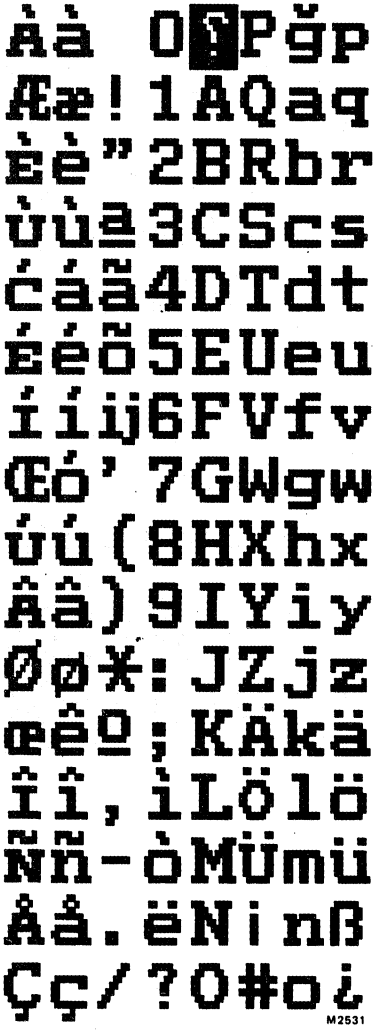
The display is generated to 625-line/60 Hz scanning (interlaced or non-interlaced).
In addition to composite sync (pin 32) for conventional timebases, a clock output at 1.2 MHz or 7.2 MHz (pin 29) is available for driving other videotex devices, and a 14.4 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

DEVELOPMENT DATA

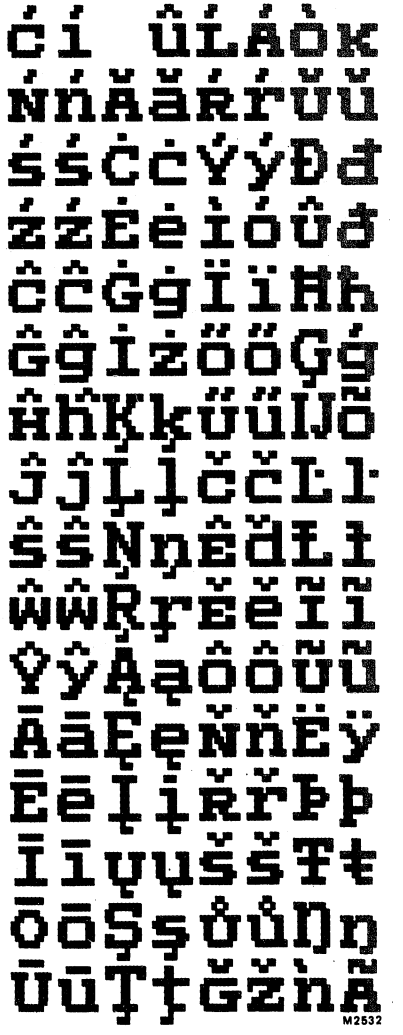
APPLICATION INFORMATION (continued)

Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.



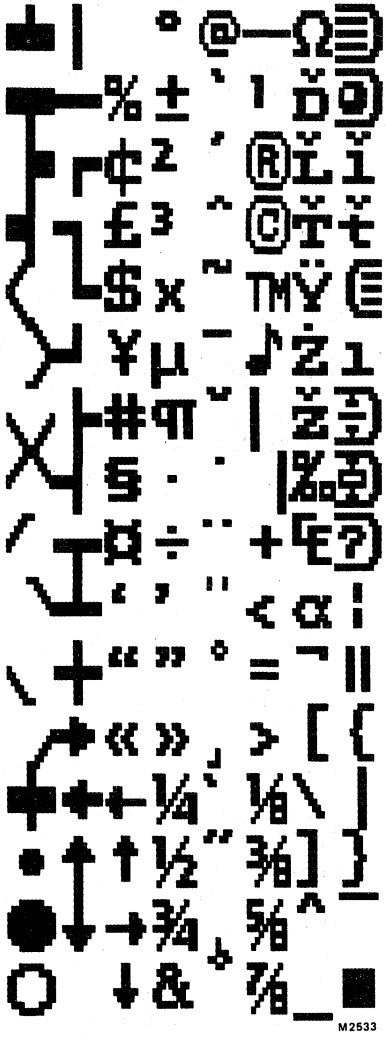
(a)



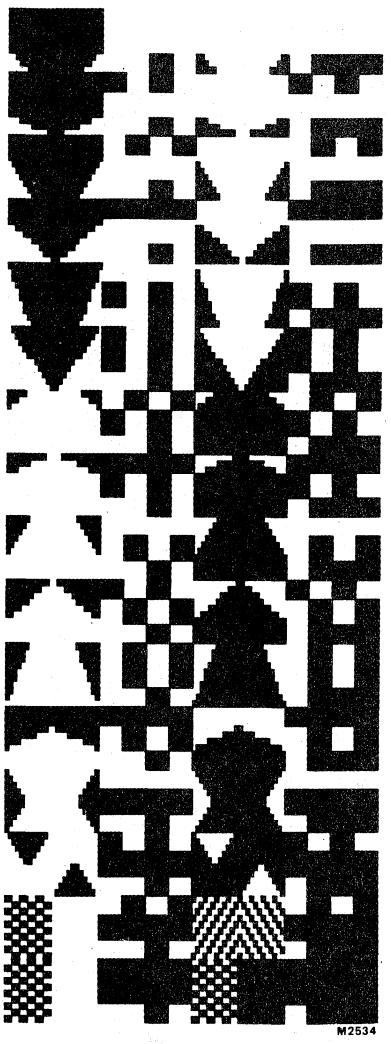
(b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.

DEVELOPMENT DATA



(a)



(b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

APPLICATION INFORMATION (continued)

Character generation (continued)

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

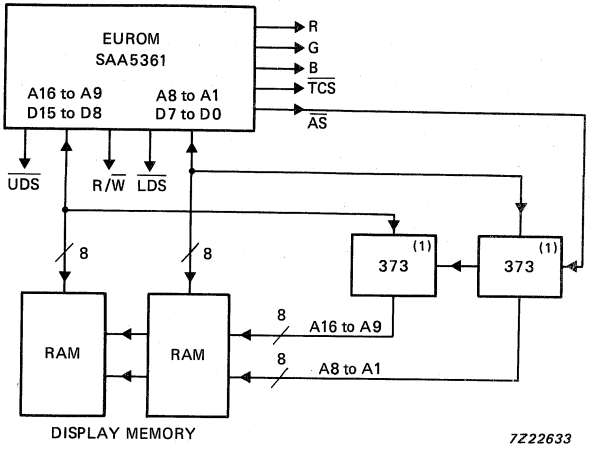
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 417 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

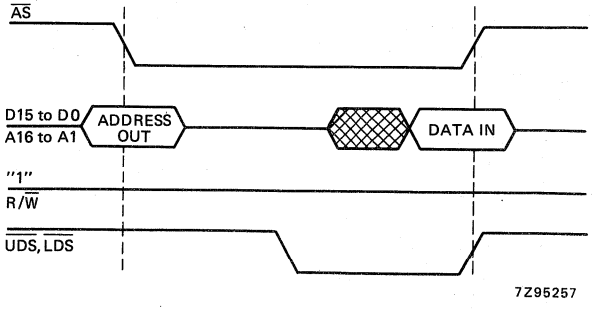


Fig. 18 Bus timing for display memory access.

APPLICATION INFORMATION (continued)

EUROM access to display memory (continued)

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain — there are no odd-numbered word addresses.

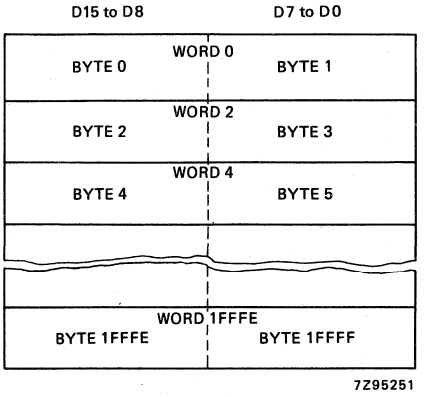


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 19.2 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

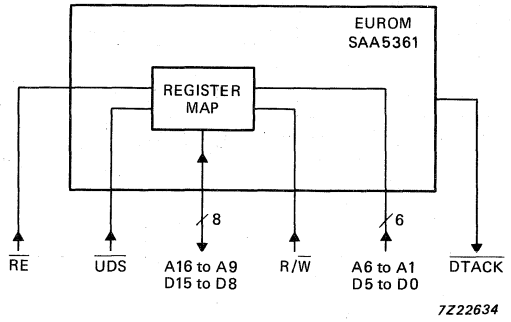


Fig. 20 Microprocessor access to register map.

The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

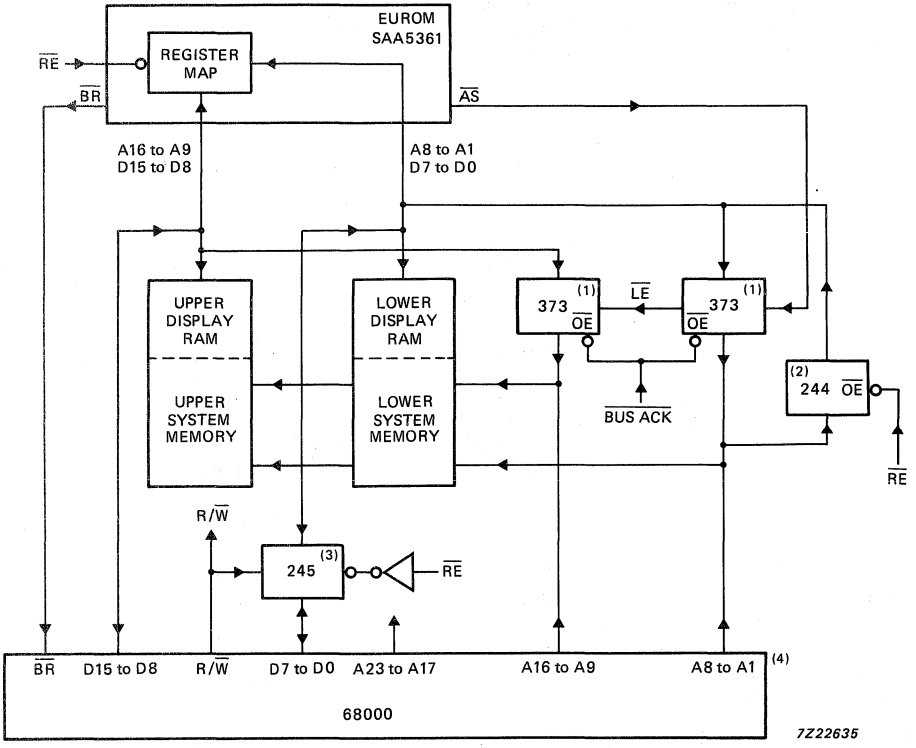
8-bit microprocessors

Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).

DEVELOPMENT DATA

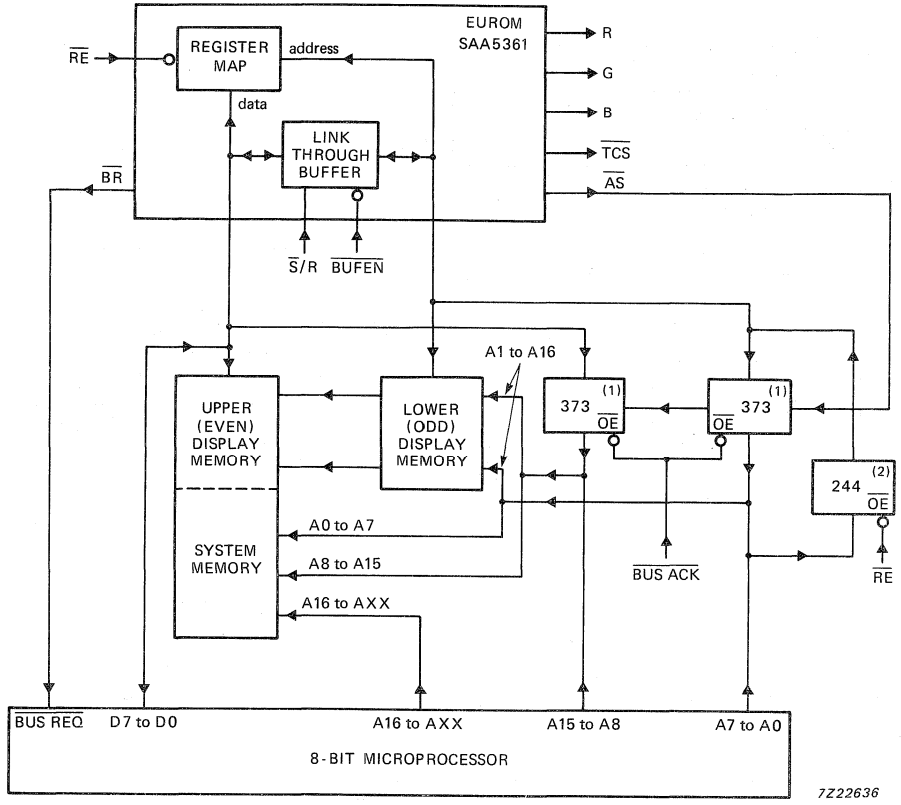
APPLICATION INFORMATION (continued)



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

DEVELOPMENT DATA



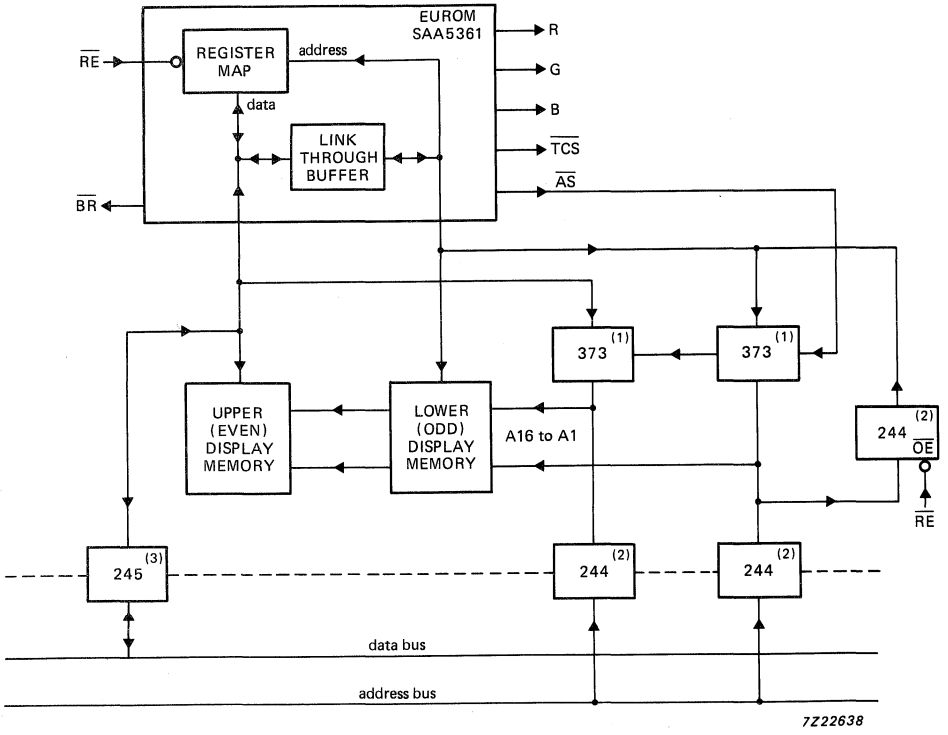
(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

APPLICATION INFORMATION (continued)

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 7.2 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

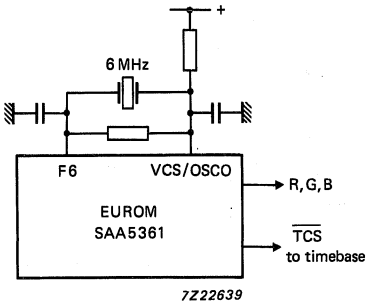


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 208 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

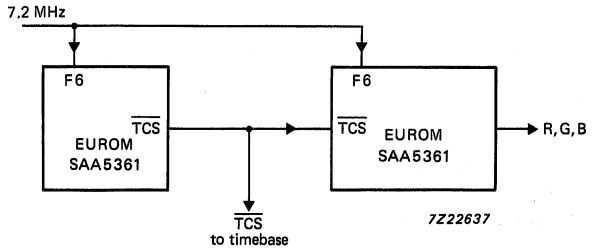


Fig. 25 Simple-slave (direct sync) mode.

APPLICATION INFORMATION (continued)

Synchronization (continued)

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. Part of a VIP2 forms alu. When EUROM is active, its horizontal counter forms part of the phase control loop — a horizontal reference is fed back to the VIP2 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possibilities.

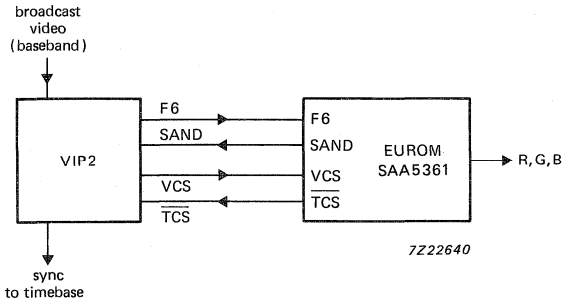


Fig. 26 Phase-locked slave (indirect sync) mode.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	April 1991

SAA7157

Clock signal generation circuit (SCGC) for a digital TV system

FEATURES

- PLL frequency multiplier
- Two different clock frequencies
- Power fail detection circuit

APPLICATIONS

- Digital TV system with line-locked sampling
- Digital TV with feature box and picture memories

GENERAL DESCRIPTION

The SAA7157 is a clock generation circuit (SCGC) which generates all clock signals required for a digital TV system utilizing the SAA715X family of devices. The circuit operates in either the phase-locked-loop mode (PLL) or voltage controlled oscillator mode (VCO).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	-	5.5	V
I_{DD}	digital supply current	10	-	60	mA
I_{DDA}	analog supply current	3	-	*	mA
$P_{tot\ (c)}$	total power consumption	-	-	0.4	W
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157P	20	DIL	plastic	SOT146
SAA7157T	20	SO20	plastic	SOT163A

* Value to be fixed.

Clock signal generation circuit (SCGC) for a digital TV system

SAA7157

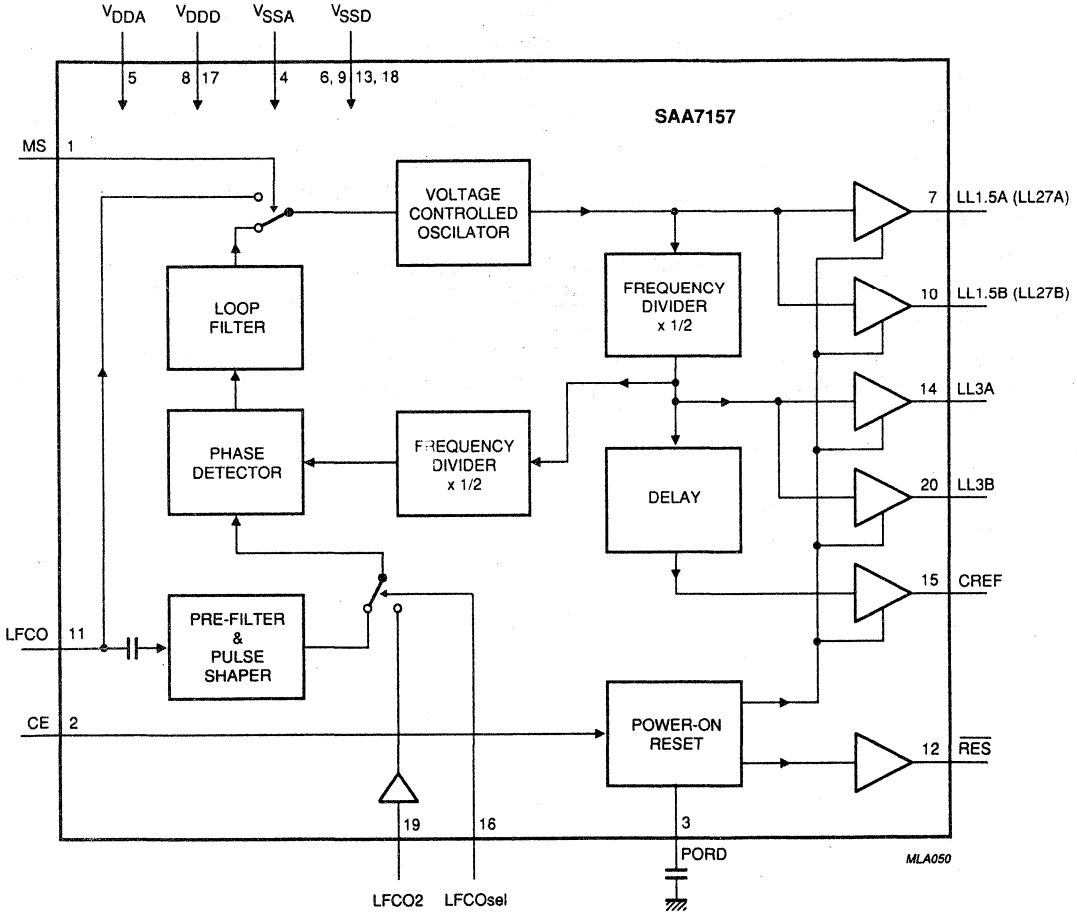


Fig.1 Block diagram.

Clock signal generation circuit (SCGC) for a digital TV system

SAA7157

PIN CONFIGURATION

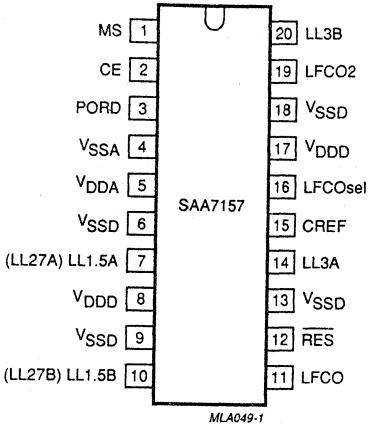


Fig.2 Pin configuration.

Clock signal generation circuit (SCGC) for a digital TV system

SAA7157

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	Mode Select input. Usually this input is LOW and the SCGC generates the different clocks using the LFCO or LFCO2 as reference frequency
CE	2	Chip Enable input. A HIGH level at CE enables the output buffers; a LOW level sets the clock buffers to HIGH and $\overline{RES}$ to LOW. The VCO operates on an internally adjusted frequency
PORD	3	Power-On Reset Delay. An external capacitor at this pin determines the duration of the reset state (see $\overline{RES}$)
V_{SSA}	4	Analog ground
V_{DDA}	5	Analog power supply
V_{SSD}	6	Digital ground
LL1.5A	7	LL1.5A (LL27A) is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
V_{DDD}	8	Digital power supply
V_{SSD}	9	Digital ground
LL1.5B	10	LL1.5B (LL27B) is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
LFCO	11	Line Frequency COntrol input. This signal received from the DMSD, is a multiple of the line frequency (6.75 MHz). It is the reference frequency for all clocks generated by the SCGC
$\overline{RES}$	12	RESET output (active LOW). This output indicates the reset state. After a power-ON or power failure $\overline{RES}$ goes LOW and remains in this state for a period that is determined by the external capacitor connected to pin PORD. If the supply voltage decreases below the operating range (power failure)*, $\overline{RES}$ goes LOW. After the power supply returns within the operating range and the POR delay is completed, $\overline{RES}$ goes HIGH. This signal can be used to reset the entire digital TV system. When CE is LOW, the $\overline{RES}$ output will be set LOW
V_{SSD}	13	Digital ground
LL3A	14	LL3A is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular
CREF	15	CLocK reference signal of digital TV2. This output is a clock qualifier signal of 2 times the LFCO or LFCO2 input frequency for bus clock generation
LFCOsel	16	Line Frequency COntrol select. This input signal selects either the LFCO signal from the DMSD (LFCOsel = LOW) or a TTL-compatible LFCO2 signal (LFCOsel = HIGH)
V_{DDD}	17	Digital power supply
V_{SSD}	18	Digital ground
LFCO2	19	Line Frequency COntrol 2 input. This signal received e.g. from the MAC decoder, is a multiple of the line frequency (6.75 MHz). It is the TTL-compatible reference frequency for all clocks generated by the SCGC
LL3B	20	LL3B is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular

* See section "**APPLICATION INFORMATION**"; Fig.4, reset waveform.

Clock signal generation circuit (SCGC) for a digital TV system

SAA7157

FUNCTIONAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system utilizing the SAA715X and SAA905X families of devices. These consist of the ADC8 (8-bit Analog-to-Digital Converter), DMSD2 (Digital Multi-Standard Decoder) and VEDA (Video Enhancement and Digital-to-Analog converter). Optional extras (Video, Memory, Controller etc.) via external buffers, this is advantageous for a digital video signal processing system based on display standard conversion concepts. The frequency of the reference signal LFCO, a 6.75 MHz triangular waveform from the DMSD or LFCO2, a 6.75 MHz TTL-compatible from the MAC decoder, is multiplied by the PLL to 27 MHz. This clock signal is frequency divided to produce LL1.5A/B (LL27A/B) and LL3A/B (LL13.5A/B) using ratios of 1:1 and 1:2 respectively.

The clock signals of LL1.5 (LL27) and LL3 are rectangular waveforms. The clock outputs of equal frequency may be wired together externally. The clock signal output lines go HIGH during an internal power-ON reset period. This internal reset period ensures that the clock signals are delivered before $\overline{RES}$ goes HIGH.

The $\overline{RES}$ output signal indicates a stable power supply. This output can be used to drive other power-ON reset circuits and provides the SAA7157 with a capability to reset an entire digital video signal processing system. The reset time is determined by the external capacitor connected to pin PORD. It is important that a signal, within the specified ranges, is applied to the LFCO or LFCO2 input before $\overline{RES}$ goes HIGH. The power-ON reset circuit is combined with a power-failure detector.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}/V_{DDA}	supply voltage		−0.5	7.0	V
V_I	input voltage		−0.5	7.0	V
V_O	output voltage	I_{OM} = 20 mA	−0.5	7.0	V
P_{tot}	total power dissipation		-	1.1	W
T_{stg}	storage temperature range		-55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Clock signal generation circuit (SCGC) for a digital TV system

SAA7157

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 6.0$ to 7.2 MHz; $T_{amb} = 0$ to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DDD}	digital supply voltage		4.5	5.5	V
I_{DDD}	digital supply current		10	60	mA
V_{DDA}	analog supply voltage		4.5	5.5	V
I_{DDA}	analog supply current		3	*	mA
Inputs					
MS, CE, LFCO and LFC02					
I_{IL}	input leakage current		-	10	µA
MS, CE, LFCOsel and LFCO2					
C_I	input capacitance		-	5	pF
LFCO					
C_I	input capacitance		-	10	pF
CE, LFCOsel and LFCO2					
V_{IL}	input voltage LOW		0	0.8	V
V_{IH}	input voltage HIGH		2.0	V_{DDD}	V
LFCO2					
f_{LFCO2}	input frequency		6.0	7.2	MHz
LFCO					
V_{LFCO}	input voltage		0	V_{DDA}	V
f_{LFCO}	input frequency		6.0	7.2	MHz
$V_{LFCO(p-p)}$	input signal amplitude (peak-to-peak value)		1.0	V_{DDA}	V
Outputs					
LL1.5A, LL1.5B, LL3A, CREF and LL3B					
V_{OH}	output voltage HIGH	CE = LOW; $I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
RES					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.4	V
t_d	delay time (see Fig.4)	$C_{PORD} = 100$ nF	20	200	ms
CREF					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
C_L	output load capacitance		15	40	pF
t_{HD}	output hold time	note 1	4	-	ns
t_{SU}	output set-up time		12	-	ns

* Value to be fixed.

CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs (continued)					
LL1.5A, (LL27A), LL1.5B, (LL27B), LL3A and LL3B					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
	output frequency				
$f_{LL1.5A}$	LL1.5A		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
fLL1.5B	LL1.5B		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
f_{LL3A}	LL3A		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
f_{LL3B}	LL3B		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
t_r	rise time	0.6 V to 2.6 V	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	5	ns
t_{comp}	composite rise time	note 2	-	8	ns
LL1.5A, LL1.5B, LL3A and LL3B					
	duty factor	notes 1 and 3			
K_{CLK1}	LL1.5A, LL1.5B		0.43	0.57	
K_{CLK3}	LL3A, LL3B		0.43	0.57	

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz, with a 40 pF output load (typically 6.75 MHz); see Fig.3.

2. The composite rise time is the time duration from all clocks = LOW to all clocks = HIGH (within 0.6 V to 2.6 V, includes rise time, skew and jitter). Skew between two LLX clocks will not deviate more than ± 2 ns if output loads are matched within 20%.

3. The duty factor is mean value and defined at 1.5 V.

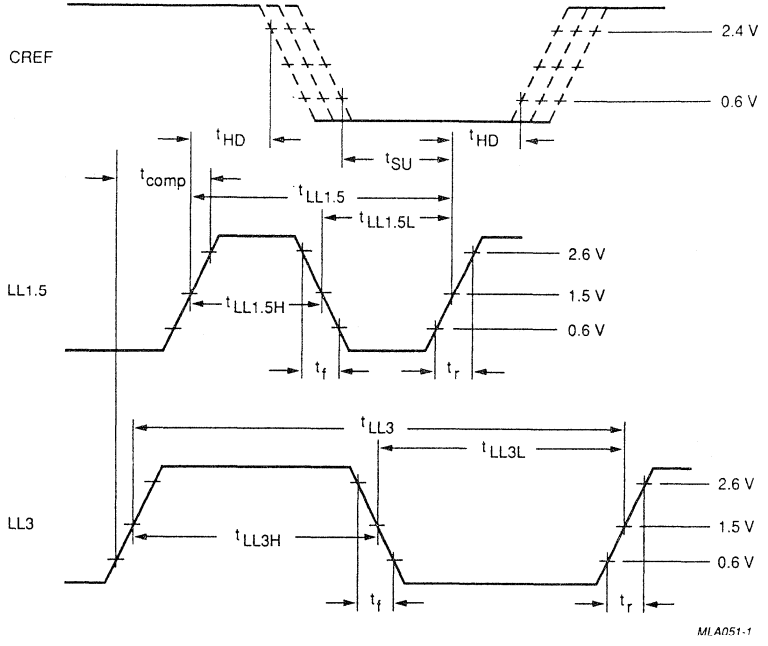


Fig.3 Timing waveform.

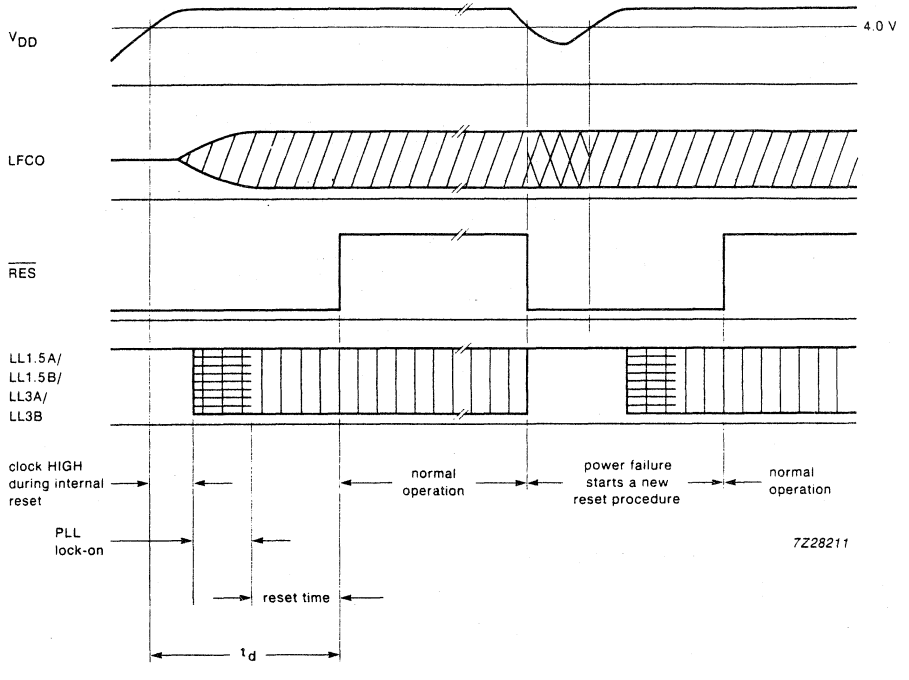


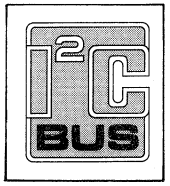
Fig.4 Reset waveform.

Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

SAA7191

Digital multistandard decoder - square pixel (DMSD-SQP)



GENERAL DESCRIPTION

The Digital Multistandard Decoder - Square Pixel (DMSD-SQP) is able to decode colour of PAL, NTSC-M and SECAM standards on the basis of a line-locked clock.

The input ports are either one 8-bit channel for the CVBS signals or two 8-bit channels, one for Y signals the other for sub-carriered chrominance signals from S-VHS sources.

The output ports are one 8-bit channel for processed Y signals and one 8-bit channel for multiplexed decoded -(B-Y) and -(R-Y) signals.

The input data rate is 29.5 MHz for both the channels in the 50 Hz mode, or 24.5454 MHz in the 60 Hz mode.

The output data rate is 14.75 MHz/ 12.2727 MHz for the Y-signal and 7.375 MHz/6.136 MHz (optional 3.6875 MHz/3.068 MHz) for the -(B-Y) and -(R-Y) signals (50 Hz modes/60 Hz mode). Output levels are in accordance with CCIR 601.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191	68	PLCC	plastic	SOT188AA,AGA

Digital multistandard decoder - square pixel (DMSD-SQP)

SAA7191

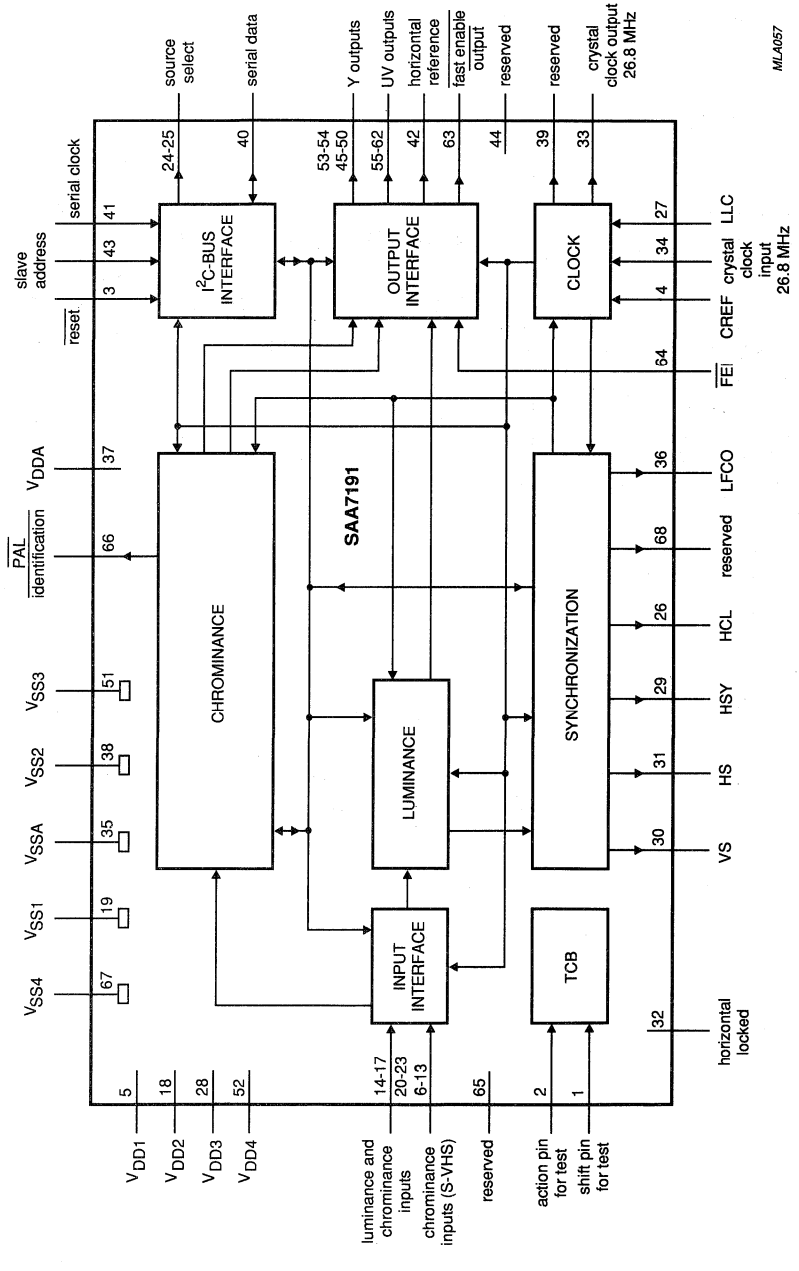


Fig.1 Block diagram.

Digital multistandard decoder - square pixel (DMSD-SQP)

SAA7191

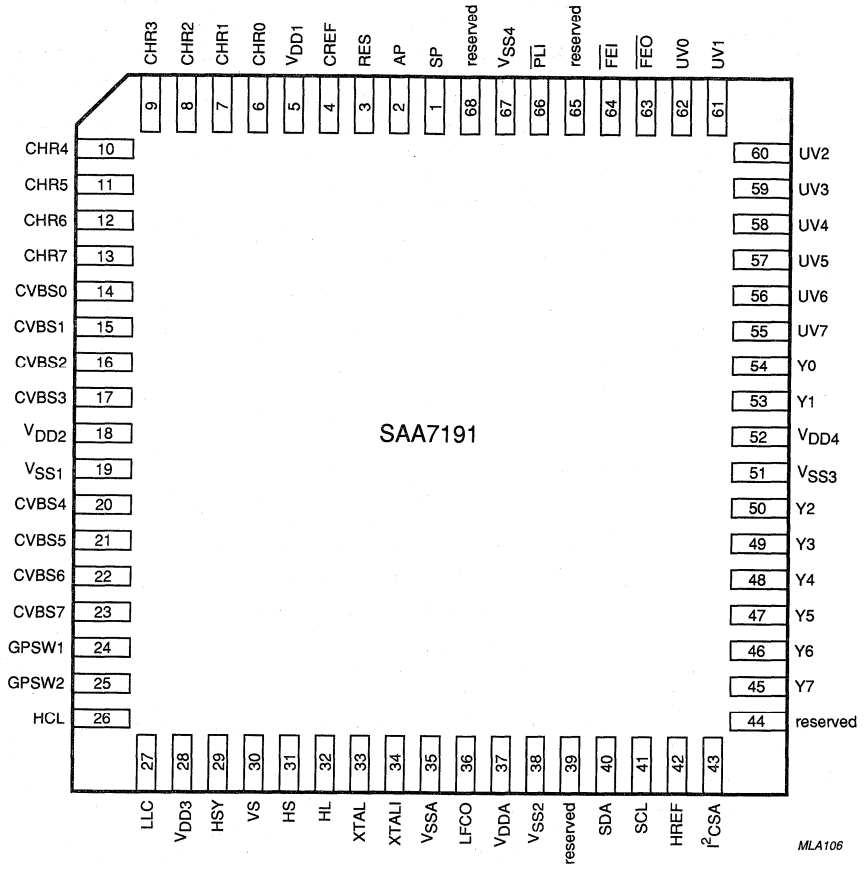


Fig.2 Pin configuration.

Digital multistandard decoder - square pixel (DMSD-SQP) SAA7191

PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	shift pin for testing; connected to ground in normal operation
AP	2	action pin for testing; connected to ground in normal operation
$\overline{RES}$	3	reset, active LOW; sets the device into a defined state. All data outputs are in a high impedance state. The I²C-bus is reset (waiting for the start condition). The LOW period must be maintained for a minimum of 30 LLC clock cycles.
CREF	4	clock reference; this is a clock qualifier signal generated by the Clock Generator Circuit (CGC). Using CREF all interfaces on the digital YUV bus are able to generate a bus timing with identical phase.
V_{DD1}	5	V_{DD}; positive supply voltage (+5 V)
CHR(0-7)	6 to 13	chrominance input signal; 8-bit digitized chrominance input from a S-VHS source in two's compliment format
CVBS(0-3)	14 to 17	composite video blanking input signal; lower 4 bits of the 8-bit digitized CVBS contains the luminance, chrominance and all synchronization information in two's complement format
V_{DD2}	18	V_{DD}; positive supply voltage (+5 V)
V_{SS1}	19	ground
CVBS(4-7)	20 to 23	composite video blanking input signal; higher 4 bits of the 8-bit digitized CVBS contains the luminance, chrominance and all synchronization information in two's complement format
GPSW1	24	general purpose switch 1 output signal; the state of this signal is set via the I²C-bus register 0Eh, bit 0; TTL compatible
GPSW2	25	general purpose switch 2 output signal; the state of this signal is set via the I²C-bus register 0Eh, bit 1; TTL compatible
HCL	26	horizontal clamp pulse (programmable); this signal can be used to indicate the black-level clamping period for the analog input interface, e.g. TDA8708 (ADC). The beginning and end of its HIGH period can be programmed via the I²C-bus registers 03h and 04h in the 50 Hz mode and registers 16h and 17h in the 60 Hz mode
LLC	27	line-locked clock input (system clock); the frequency is 1888 x f_H = 29.5 MHz in the 50 Hz mode and 1560 x f_H = 24.5454 MHz in the 60 Hz moded (525 lines per frame)
V_{DD3}	28	V_{DD}; positive supply voltage (+5 V)
HSY	29	horizontal sync indicator output signal (programmable); may be used to indicate the sync top portion of the CVBS input signal for gain control purposes. This signal is normally fed to the analog input interface, e.g. TDA8708 - ADC. The beginning and end of its HIGH period can be programmed via the I²C-bus registers 01h and 02h in the 50 Hz mode and registers 14h and 15h in the 60 Hz mode
VS	30	vertical sync output signal; this signal indicates the vertical sync with respect to the digital YUV output. The HIGH period of the signal is approximately 6 lines if the Vertical Noise Limiter (VNL) function is active. The positive slope contains the phase information
HS	31	horizontal sync output signal (programmable); the HIGH period is 128 LLC clock cycles. The position of the positive slope is programmable in 8 LLC increments over a whole line via the I²C-bus registers 05h in the 50 Hz mode and 18h in the 60 Hz mode
HL	32	horizontal PLL output signal; a HIGH state indicates that the internal PLL has locked
XTAL	33	crystal oscillator output signal; frequency = 26.8 MHz
XTAL1	34	second pin for crystal oscillator or connection of external oscillator; TTL compatible squarewave
V_{SSA}	35	ground; analog supply

SYMBOL	PIN	DESCRIPTION
LFCO	36	line frequency control output signal; this is the analog clock control signal driving the CGC. The frequency is a multiple of the actual line frequency (nominal 7.375/6.136363 MHz). The signal has a triangular waveform with a 4-bit accuracy
V_{DDA}	37	V_{DD}; positive analog supply voltage (+5 V)
V_{SS2}	38	ground
RESERVED	39	reserved pin; do not connect
SDA	40	serial data I/O; I²C-bus
SCL	41	serial clock input; I²C-bus
HREF	42	horizontal reference output signal; this signal is used to indicate active data on the digital YUV bus. The positive slope marks the start of a new active line. The HIGH period of HREF is either 768 Y samples or 640 Y samples long depending on the detected field frequency (50/60 Hz mode). HREF is used to synchronize data multiplexers/demultiplexers. The HREF signal is also present during the vertical blanking interval
I²CSA	43	I²C-bus slave address select input; used to distinguish between two I²C-bus addresses; LOW = address 8Ah, HIGH = address 8Eh
RESERVED	44	reserved pin; do not connect
Y(7-2)	45 to 50	digital Y (luminance) output signal; higher 6 bits of the 8-bit luminance output signal used as part of the digital YUV bus
V_{SS3}	51	ground
V_{DD4}	52	V_{DD}; positive supply voltage (+5 V)
Y(1-0)	53,54	digital Y (luminance) output signal; lower 2 bits of the 8-bit luminance output signal used as part of the digital YUV bus
UV(7-0)	55 to 62	digital UV (chrominance difference) output signal; multiplexed chrominance difference signal for U and V component of demodulated CVBS signal with 8-bit resolution. The format and multiplexing scheme can be chosen via the I²C-bus control. Part of the YUV bus
$\overline{FEO}$	63	fast enable output (active low); this signal is LOW when the Y and U/V outputs are in the HIGH impedance state
$\overline{FEI}$	64	fast enable input (active low); this signal is used to control fast switching on the digital YUV bus. A HIGH at this input forces the IC to set its Y and U/V outputs into the high impedance state after 4 LLC clock cycles. $\overline{FEI}$ and $\overline{FEO}$ provide a daisy chain structure for priority control of the YUV bus
RESERVED	65	reserved pin; do not connect
$\overline{PLI}$	66	PAL identifier output signal; marks the demodulated PAL signals; inverted line = $\overline{PLI}$ LOW, non-inverted line = $\overline{PLI}$ HIGH
V_{SS4}	67	ground
RESERVED	68	reserved pin; do not connect

FUNCTIONAL DESCRIPTION

Chrominance

The incoming chrominance signal (either from the CVBS or chrominance port, is fed via a high pass filter for DC elimination to two multipliers.
The multiplicator inputs of the multipliers are two sub-carrier signals from a local oscillator, 90° phase-shifted against each other, and at a frequency depending on the individual colour standard.
The multipliers operate as a quadrature demodulator for all PAL and NTSC signals, and as a frequency down-mixer for SECAM.
After three parallel low-pass filter stages, the two signals are serialized and applied to a gain controlled amplifier. Together with the preceding stages a final multiplexed low-pass filter produces the required bandwidth performance.
The PAL and NTSC originated signals are applied to a comb filter, while SECAM-originated signals are fed through a serial Cloche filter (centred at 0 Hz), a phase demodulator and a differentiator to produce frequency demodulated colour difference signals.
After a deemphasis, the SECAM signals are fed into a cross-over switch to provide both the serially-transmitted colour difference signals.
The colour difference signals are fed finally to the output formatter and to the output interface.

Luminance

The incoming CVBS signal is fed through a sample rate decimator to reduce the data rate to 12.2727 MHz for NTSC signals and 14.75 MHz for PAL/SECAM signals. After the SRD (with a switchable prefilter), high frequency components can be emphasized to compensate for loss in the following chrominance trap.
The chrominance trap (switchable for 3.58 MHz or 4.43 MHz centred colour signals) eliminates most of the colour carrier and must be bypassed for S-VHS signals.
The high frequency components of the luminance signal can be 'peaked' (sharpness control) via two band-pass filters with selectable transfer properties, and a coring circuit with selectable coring characteristic and amount and then added to the unpeaked signal.
Because of the different DC gains of both chrominance trap modes a switchable normalizing amplifier is used to match to a common DC amplification and cut-off sync pulse for the unpeaked signal for both modes.
For synchronization purposes, in order to generate a line-locked clock, the Y signal is taken from an output amplifier.
The processed luminance signal is fed via a programmable delay line to the output formatter.

Synchronization

The signal from the luminance processing is the input signal for the sync processing unit.
The bandwith is reduced to 1 MHz by lowpass filtering and the synchronization pulses are separated from the luminance signal. The synchronization pulses are then fed to phase detectors where they are compared with the divided clock frequency. The resultant output is applied to the loop filter which accumulates all phase deviations.
The loop filter drives an oscillator which generates the LFCO signal. An external analog PLL generates the required clock frequency (for compatibility reasons) from that oscillator frequency. The output signals (adjustable) e.g. HCL and HSY are generated according to the peripheral requirements.

CHARACTERISTICS

T_{amb} = 0 to 70 °C; V_{DD} = 4.5 to 5.5; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
Inputs					
V_{IL}	input voltage LOW (SDA, SCL)		−0.5	1.5	V
V_{IH}	input voltage HIGH (SDA, SCL)		3.0	V_{DD}+0.5	V
V_{IL}	input voltage LOW (any other)		−0.5	0.8	V
V_{IH}	input voltage HIGH (any other)		2.0	V_{DD}+0.5	V
I_{LI}	input leakage current		-	10.0	µA
C_I	input capacitance (clocks)		-	10.0	pF
C_I	input capacitance (data)		-	8.0	pF
C_I	input capacitance	I/O = HIGH Z	-	8.0	pF
Outputs					
V_{36}	output voltage (LFCO)		0	V_{DD}	V
$V_{36(p-p)}$	output amplitude (LFCO) (peak-to-peak value)	note 1	1.4	2.6	V
V_{OH}	output voltage HIGH (any other)	note 2	2.4	V_{DD}	V
V_{OL}	output voltage LOW (any other)	note 2	0	0.6	V
Timing (note 3)					
t_{LLC}	cycle time		31.0	45.0	ns
k_{LLC}	duty factor	t_{LLCH}/t_{LLC}	40.0	60.0	%
t_r	rise time (LL27)		-	5.0	ns
t_f	fall time (LL27)		-	6.0	ns
t_{sk}	static skew to LFCO2 signal		-	33.0	ns
$t_{SU;DAT}$	input data set-up time		-	11.0	ns
$t_{HD;DAT}$	input data hold time		-	3.0	ns
Data and control outputs (note 3)					
C_{load}	output load capacitance (data, VS and HREF)		15.0	50.0	pF
C_{load}	output load capacitance (control)		7.5	25.0	pF
t_{OH}	output hold time (HSY)	$C_{load(min)}$	5.0	-	ns
t_{OH}	output hold time (data, HREF and VS)	$C_{load(min)}$	13.0	-	ns
t_{OH}	output hold time (others)	$C_{load(min)}$	4.0	-	ns
t_{OD}	output delay time (HSY)	$C_{load(max)}$	-	80.0	ns
t_{OS}	output set-up time (others)	$C_{load(max)}$	14.0	-	ns
t_{SZ}	output disable time to 3-state		16.0	-	ns
t_{ZS}	output enable time from 3-state		14.0	-	ns

Notes to the characteristics

1. Data signals are Yn and UVn of the YUV bus. All other signals are control signals.

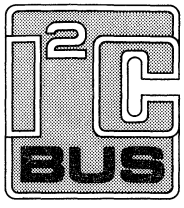
2. The levels have to be measured with load circuits.
   The loads depend on the type of output stage:

   outputs for control (no bus):
   1.2 kΩ to 3.0 V (TTL load), CL = 25 pF

   outputs for data (bus):
   1.2 kΩ to 3.0 V (TTL load), CL = 50 pF

   LFCO output of DMSD:
   10 kΩ to V_{SS}, CL = 15 pF

3. Effects of rise and fall times are included in the calculation of t_{SU}, t_{HD}, t_{OH} and t_{OD}.



Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

SAA7192
Digital colour space converter

INTRODUCTION

The Digital Color Space Converter (DCSC) is a matrix which is used to transform 8-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 8-bit format in accordance with the CCIR-601 recommendations.
The system accepts the formats of the DMSD2 family of decoders at the input. The maximum data rate is 16 MHz. The propagation delay of the device is constant. A matched pipeline delay line is available to enable the HREF signal to be synchronized with the video data at the output.

SYSTEM FUNCTIONS

The DCSC consists of the following functional blocks, as illustrated in Fig.1:

- Input Formatter with;
  multiplexer
  Y-delay line
  Cr and Cb Interpolating filters
- Conversion matrix
- Video look up tables
- Pipeline delay line
- I²C-bus interface

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT188AA,AGA

Digital colour space converter SAA7192

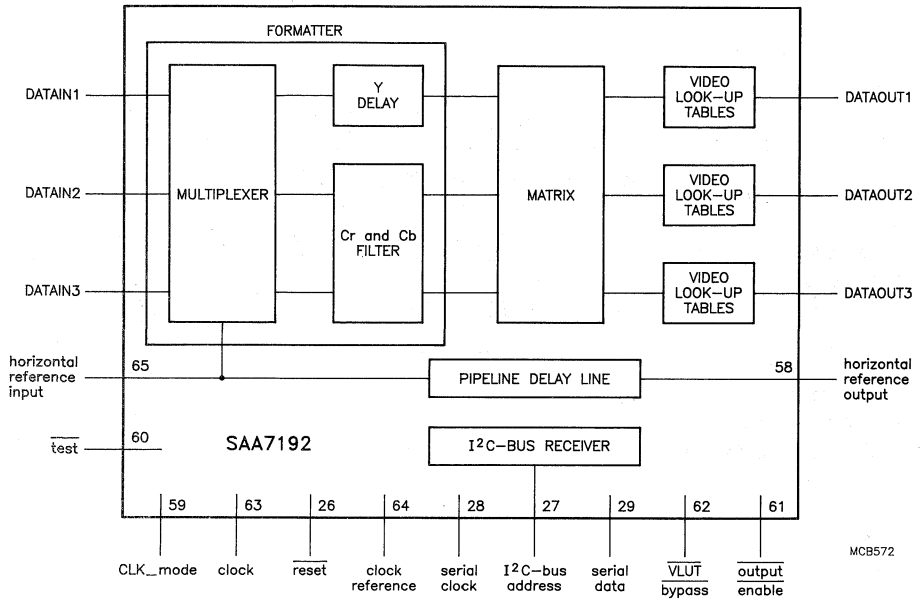


Fig.1 Block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

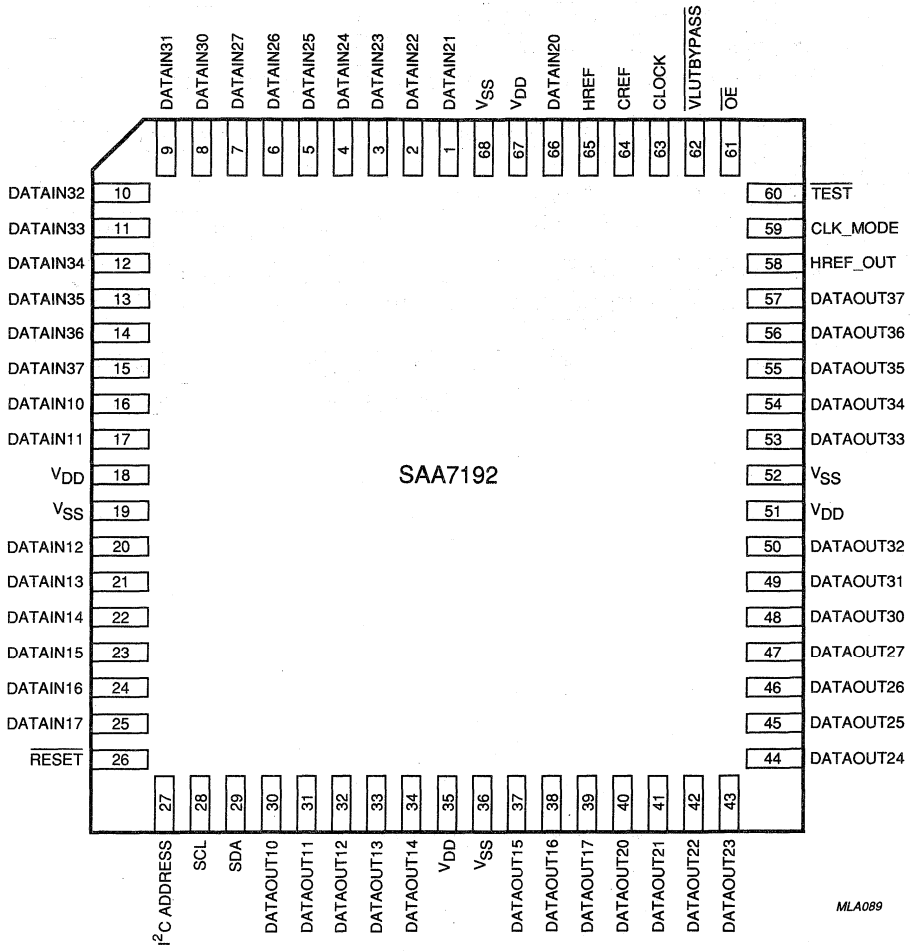


Fig.2 Pinning diagram.

Functional modes

Table 1 Functional Modes.

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN "Process Bypass"
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT.
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Figures 3 to 9b illustrate the various functional modes.

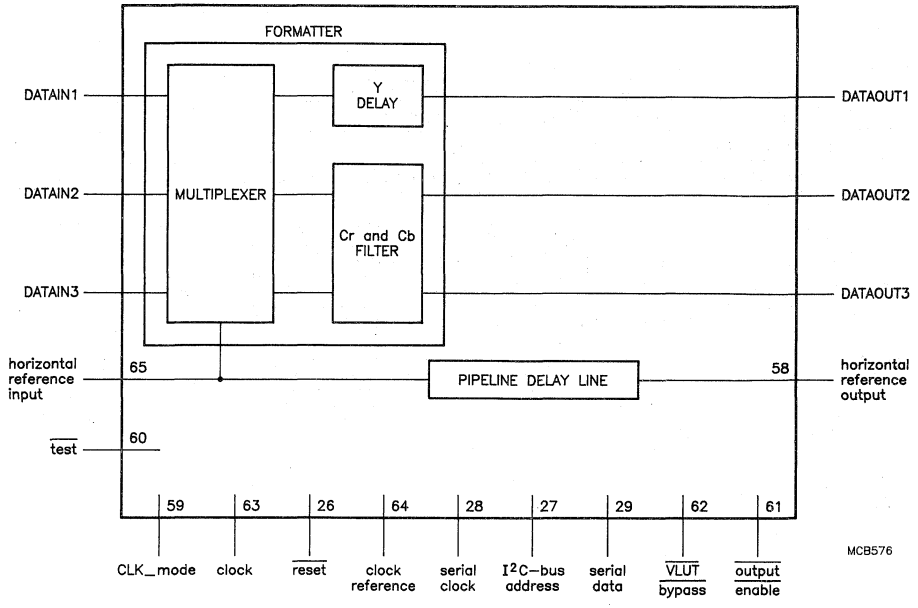


Fig.3 Functional mode 1 and 5.

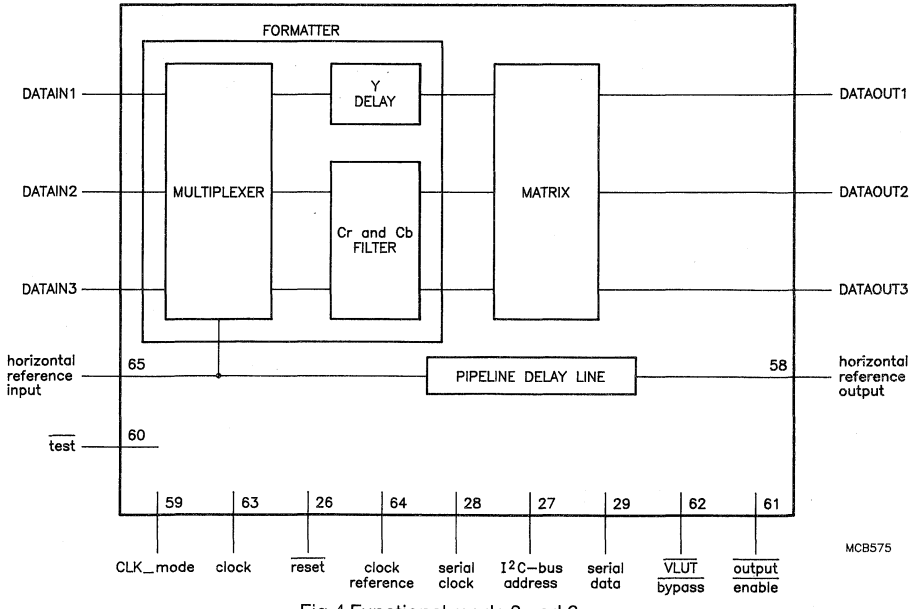


Fig.4 Functional mode 2 and 6.

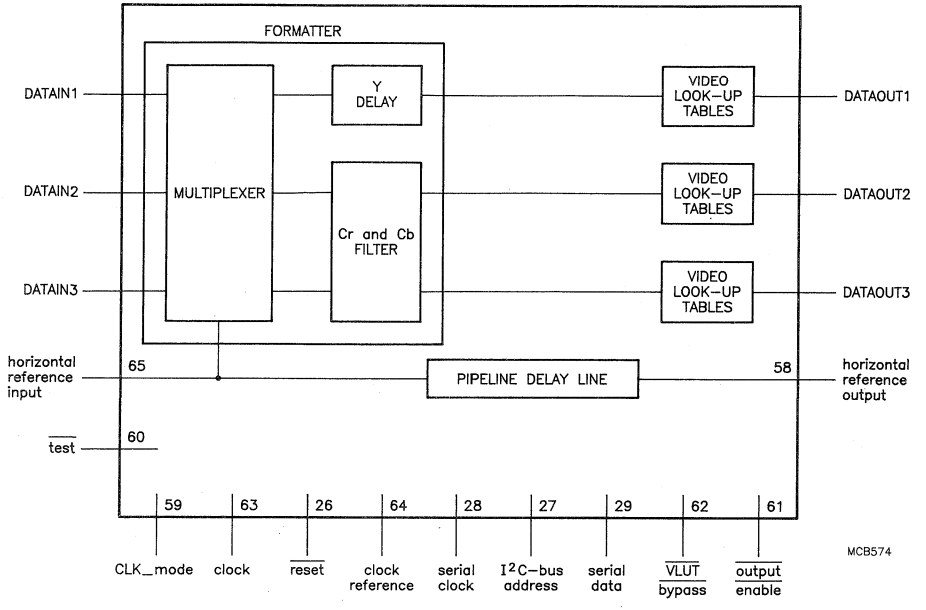


Fig.5 Functional mode 3 and 7.

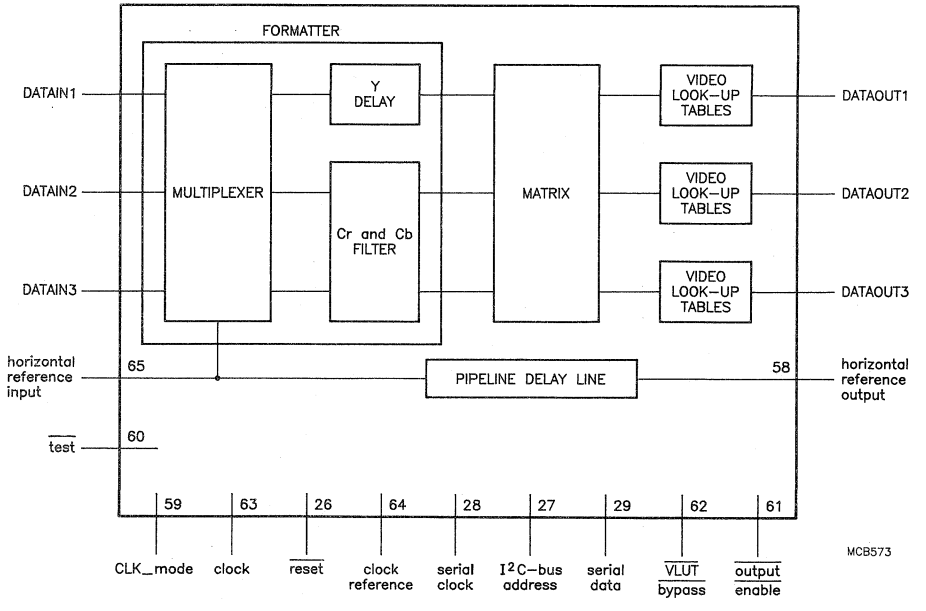


Fig.6 Functional mode 4 and 8.

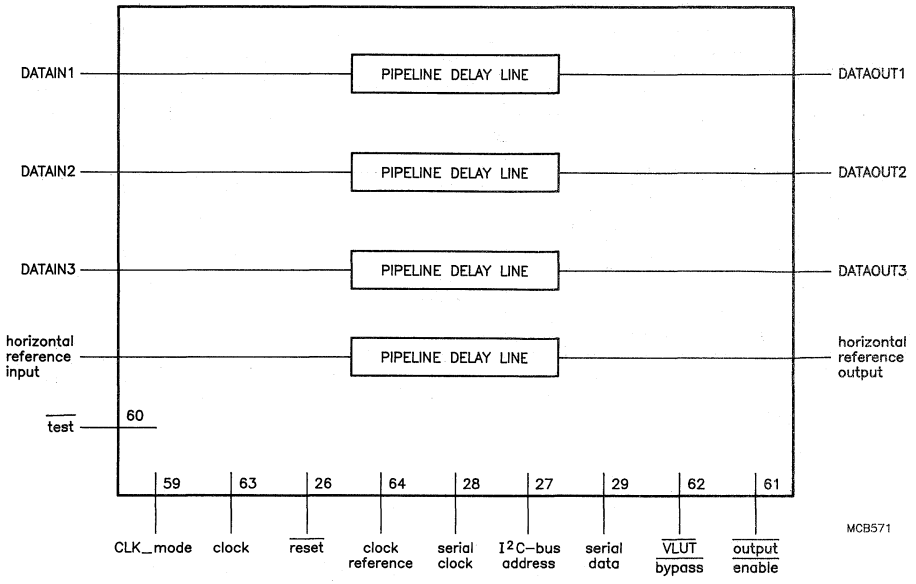


Fig.7 Functional mode 9.

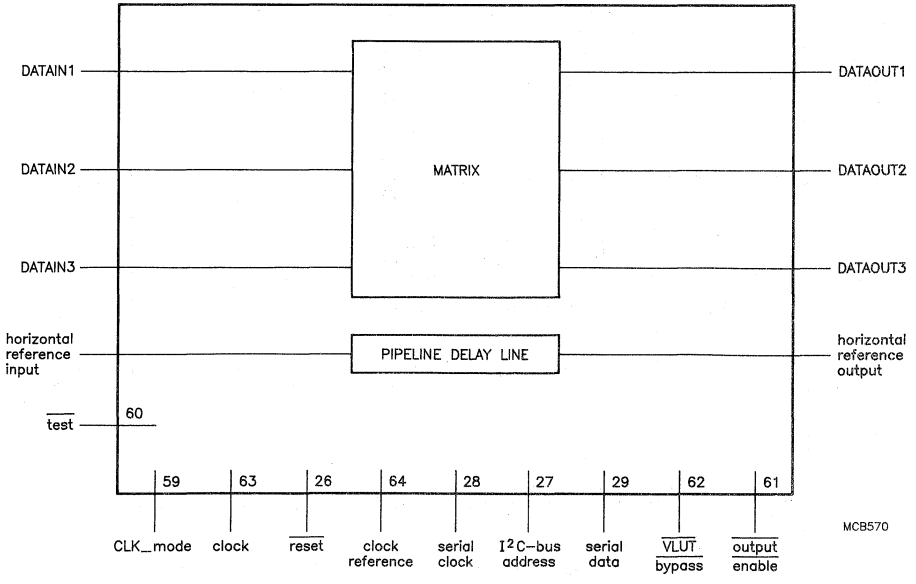


Fig.8 Functional mode 10.

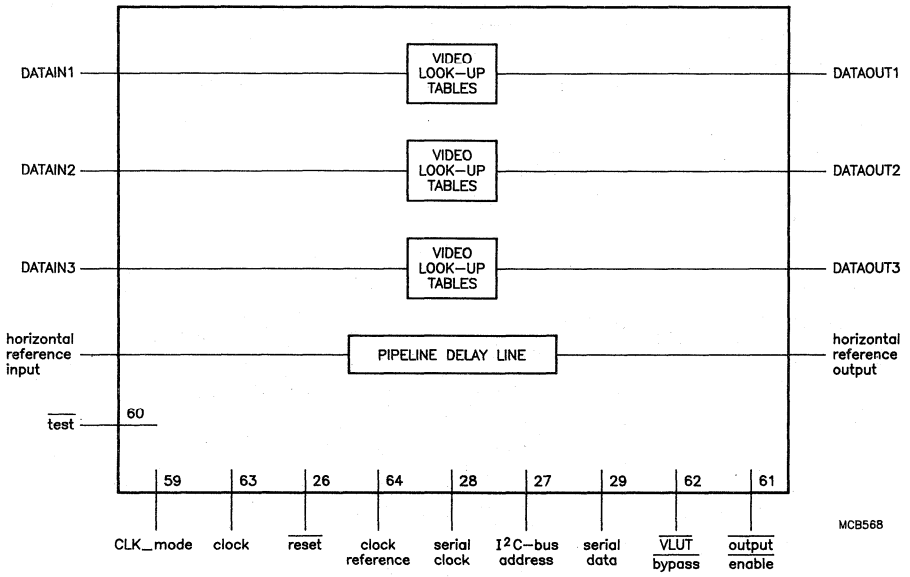


Fig.9a Functional mode 11.

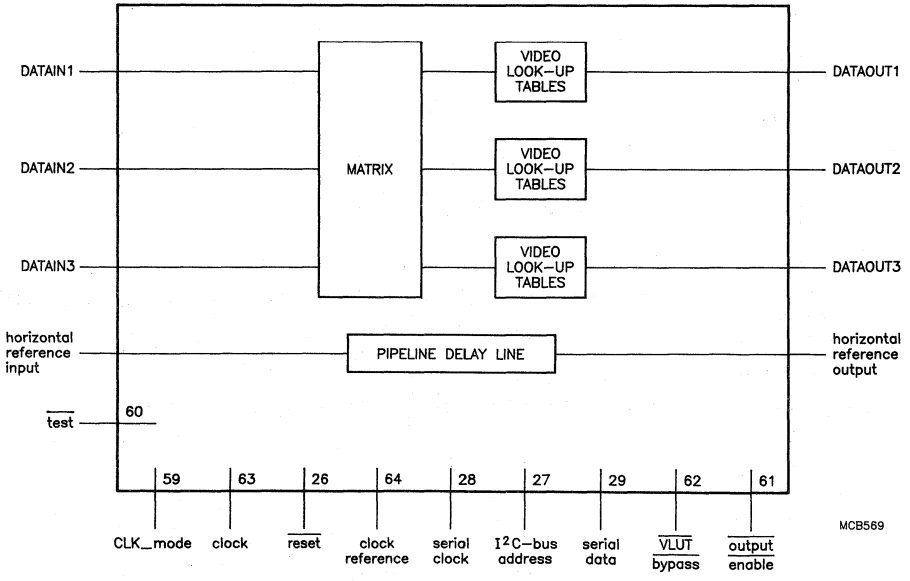


Fig.9b Functional mode 12.

Control facilities

After power-up all internal control signals of the device are at undefined values. The I²C-bus receiver must, therefore, be reset by using the external RESET signal. The control signals are then set to:

IICOE = 1
output in 3-state

FMTCNTRL = 4
format 4:4:4

$\overline{\text{MATBYPASS}}$ = 0
matrix bypassed

$\overline{\text{VLUTLOAD}}$ = 1
VLUT at READ operation

$\overline{\text{INRESET}}$ = 0
input data set to fixed values

Table 2 Input formats and functional modes

FMTCNTRL	$\overline{\text{MATBYPASS}}$	$\overline{\text{VLUTBYPASS}}$	FUNCTIONS
0	0	0	mode 1, input format 1 (DMSD2 format)
0	1	0	mode 2, input format 1 (DMSD2 format)
1	0	0	mode 1, input format 2
1	1	0	mode 2, input format 2
2	0	0	mode 5, input format 3 (DMSD2 format)
2	1	0	mode 6, input format 3 (DMSD2 format)
3	0	0	mode 5, input format 4 (parallel IN)
3	1	0	mode 6, input format 4 (parallel IN)
4	0	0	mode 9, input format 5 (parallel IN)
4	1	0	mode 10, input format 5 (parallel IN)
x	x	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

Note

The modes are given in Table 1.

The other control signals are:

$\overline{\text{VLUTLOAD}}$ = logic 1: VLOAD inactive
= logic 0: VLOAD datalines active to load VLUT

$\overline{\text{INRESET}}$ = logic 1: input latches at the formatter are always transparent
= logic 0: at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)

CLK_MODE = logic 1: DMSD mode (LL27 clock of DMSD feeds the DCSC)
= logic 0: DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 3 Output enable control

IICOE	$\overline{OE}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

Note

IICOE: output enable control of I^2C-bus (enables $\overline{OE}$)
$\overline{OE}$: output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

VIDEO DATA (DATAIN)

Table 4 Format 1 (4:1:1, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal, 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 5 Timing of Format 1; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN2, 7	U7	U5	U3	U1	U7	U5	U3
DATAIN2, 6	U6	U4	U2	U0	U6	U4	U2
DATAIN2, 5	V7	V5	V3	V1	V7	V5	V3
DATAIN2, 4	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

Table 6 Format 2 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals,8-bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 7 Timing of Format 2; the indexes show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

Table 8 Format 3 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 9 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
Clock A	0	1	2	3	4	5	6

Table 10 Format 4 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128b
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 11 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		Cb6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

Table 12 Format 5 (4:4:4, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	maximum 16.0 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless, binary 128
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 13 Timing of Format 5

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

CONTROL DATA

Clock

The line locked clock LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 5, 7, 9, 11 and 13.

The data rate on the input (DATAIN) is as follows;

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

Timing reference (Fig.10)

The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data. The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 14 Real-time control signals

$\overline{OE}$	= 1 : = 0 :	switches the output to high-z mode output enable, output stage in use
$\overline{VLUTBYPASS}$	= 1 : = 0 :	VLUT's in use VLUT's bypassed
$\overline{RESET}$	= 1 : = 0 :	device in use general reset
CLK_MODE	= 1 : = 0 :	DMSD mode (LL27 clock of DMSD feeds the DCSC) DCSC is feed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 15 I²C-bus controls

FMTCNTRL	= 0 : = 1 : = 2 : = 3 : = 4 : = 5 : = 6 : = 7 :	4:1:1 format, DMSD2 format 4:1:1 format, customized format 4:2:2 format, from DMSD2 4:2:2 format, parallel 4:4:4 format, parallel not used not used not used
$\overline{MATBYPASS}$	= 1 : = 0 :	matrix in use matrix bypassed
$\overline{VLUTLOAD}$	= 1 : = 0 :	VLOAD inactive VLOAD data lines active to load VLUT
VLUTDATA	:	load VLUT's via I²C-bus (256 x 8-bit)
$\overline{INRESET}$	= 1 : = 0 :	input latches at the formatter are always transparent at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE	= 1 : = 0 :	$\overline{OE}$ enabled switches the output to high impedance mode

Output signals

VIDEO DATA

$\overline{OE}$ (output enable, fast switch, active LOW) and IICOE (I^2C output enable, active HIGH) switchs the DATAOUT lines when in the high-impedance mode (see Control facilities).

Table 16 Format of DATAOUT (RGB if matrix in use)

DATAOUT1 (0 to 7)	Red
DATAOUT2 (0 to 7)	Green
DATAOUT3 (0 to 7)	Blue
To all three DATAOUT lines:	
Sampling frequency	12 to 16 MHz
Level	0 IRE; quantization level 16 100 IRE; quantization level 235

AUXILIARY DATA

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical Conditions

Start-up condition

No particular function except the external power-on-reset e.g. for I^2C-bus interface (RESET) is intended.

Operating time

As this device will be used in computers, it has been designed to operate continuously.

Temperature range

Refer to the characteristics.

Backup

No backup capability (standby) is provided internally.

Power down mode

No power-down capability is provided internally.

CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
Inputs					
V_{IL}	input voltage LOW (SDA, SCL)		−0.5	1.5	V
V_{IH}	input voltage HIGH (SDA, SCL)		3.0	V_{DD} +0.5	V
V_{IL}	input voltage LOW (any other)		−0.5	0.8	V
V_{IH}	input voltage HIGH (any other)		2.0	V_{DD} +0.5	V
I_{LI}	input leakage current		-	10	µA
C_I	input capacitance (clocks)		-	10	pF
C_I	input capacitance (data)		-	8	pF
Outputs					
V_{OH}	output voltage HIGH	note 1	2.4	V_{DD}	V
V_{OL}	output voltage LOW	note 1	0	0.6	V
C_L	output load capacitance (data and HREF)		15	40	pF
Timing					
t_{LL27}	cycle time	note 2	31	45	ns
k_{LL27}	duty factor		40	60	%
t_r	rise time		-	5	ns
t_f	fall time		-	6	ns
t_{CDL}	duty time LOW	note 3	26	-	ns
t_{CDH}	duty time HIGH		18	-	ns
t_{CS}	CREF set-up time		*	11	ns
t_{CH}	CREF hold time		*	3	ns
t_{HS}	HREF set-up time		*	11	ns
t_{HH}	HREF hold time		*	3	ns
$t_{SU;DAT}$	input data set-up time		11	-	ns
$t_{HD;DAT}$	input data hold time		3	-	ns
t_{OH}	ouput hold time		13	-	ns
$t_{OS;DAT}$	output data set-up time		14	-	ns
t_{SZ}	output disable time to 3-state		*	-	ns
t_{ZS}	output enable time from 3-state		*	-	ns

Note to the characteristics

1. The levels must be measured with the following load circuits; 0.6 kΩ to 3.0 V (2 TTL load); C_L = 40 pF.

2. DMSD-mode means that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal CREF is fed by the SCGC (SAA7157).

3. 16 MHz-mode means that the DCSC will work in any other environment. The CREF signal will be set to HIGH, the CLOCK signal can be any clock up to 16 MHZ.

* Value to be fixed

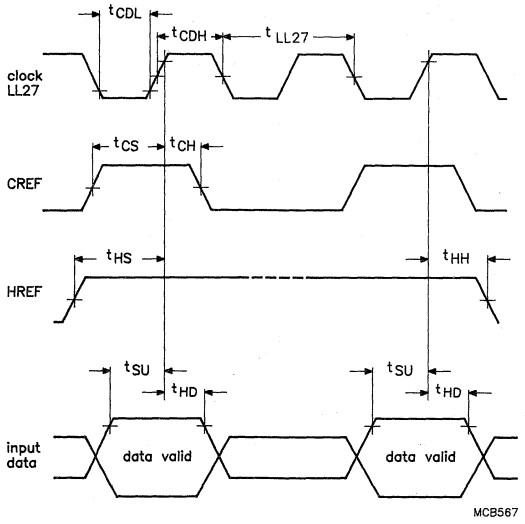


Fig.10 Input timing diagram.

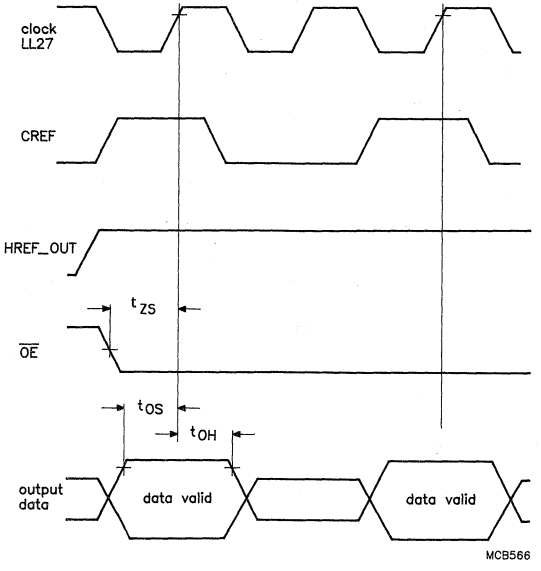


Fig.11 Output timing diagram.

Error condition

So as to inhibit unwanted operations, no information signal is available to the peripheral circuits. In the advent of an error the system has to be started again by applying the $\overline{\text{RESET}}$ signal.

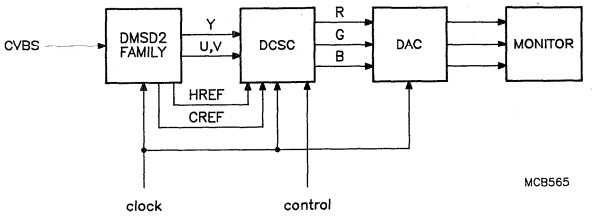


Fig.12 Application example.

SYSTEM BLOCK DESCRIPTION

INPUT FORMATTER

The formatter consist of five functional blocks;

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line;
- the timing control which creates the internal reference signals from the various inputs
- the bypass output multiplexer

Multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows;

FIL1 : Y Luminance
FIL2 : Cb colour-difference signal B-Y
FIL3 : Cr colour-difference signal R-Y

The formats and data rates of DATAIN are described in 'Video data' (see tables 4 to 13).

The sampling frequency of the FIL data lines is 16 MHz maximum. The levels of the FIL data lines are the same as characterized for the DATAIN signals.

The timing reference signals CLOCK, HREF and CREF, for distinguishing the incoming data signals, are described in 'Control data'.

The signal FMTCNTRL is used to control the multiplexer and the filter.

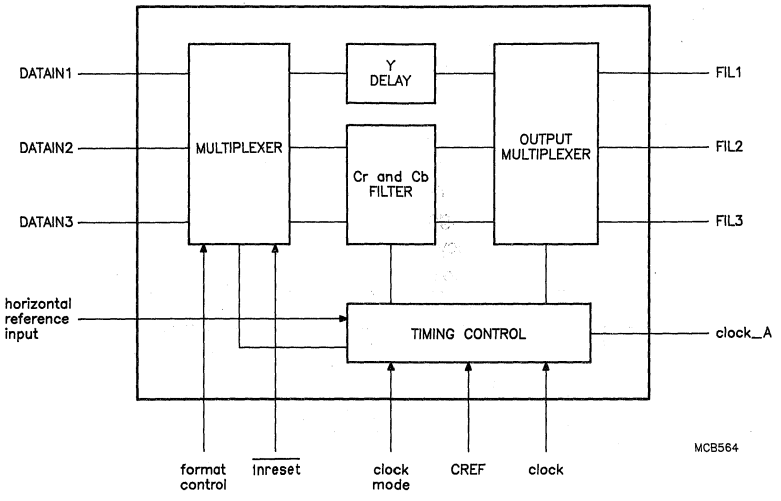


Fig.13 Input formatter.

FMTCNTRL
= 0 : 4:1:1 format; DMSD2 format
= 1 : 4:1:1 format; customized format
= 2 : 4:2:2 format; from DMSD2
= 3 : 4:2:2 format; parallel
= 4 : 4:4:4 format; parallel
= 5 : not used
= 6 : not used
= 7 : not used

$\overline{\text{INRESET}}$
= 1 : input latches transparent
= 0 : input latches has to be set to fixed values (Y to 16, Cr, Cb to 128) if HREF = 0

CLK_MODE
= 1 : DMSD mode (LL27 clock of DMSD feeds the DCSC)
= 0 : DCSC is feed by a clock of maximum 16 MHz without CREF signal.

Timing control

The timing control unit generates the required control signals from the incoming reference signals and the internally used CLOCK_A.

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in 'Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0).

DELAY LINE (LUMINANCE-DELAY)

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times the colour signal. Figure 14 illustrates the frequency response of the chrominance section.

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 15 illustrates the frequency response of the chrominance section.

Format 5 4:4:4

A bypass with a specified delay is inserted.

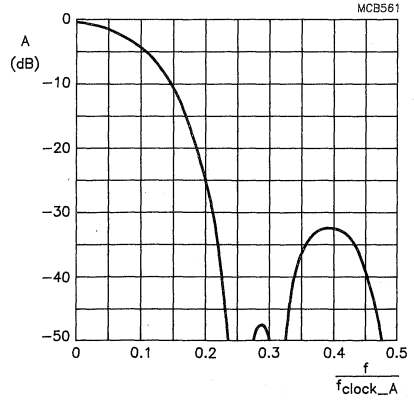


Fig.14 Frequency response of 4:1:1 filter.

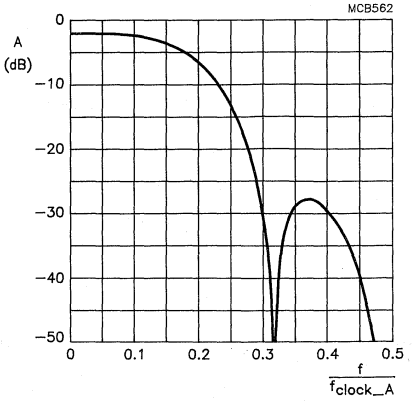


Fig.15 Frequency response of 4:2:2 filter

CONVERSIONAL MATRIX

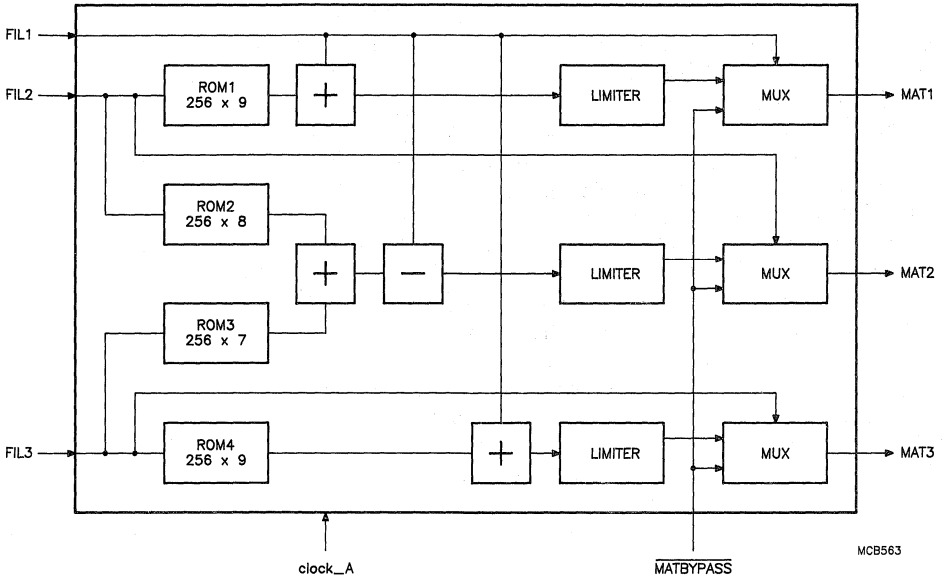


Fig.16 Block diagram MATRIX.

The properties of the conversion matrix are as follows:

- the conversion equations are (according to CCIR 601, with respect to the different quantisation on Y, Cb and Cr);

  Red = Y + 1.371 (Cr - 0.5)
  Green = Y - 0.698 (Cr - 0.5)
  - 0.336 (Cb - 0.5)
  Blue = Y + 1.732 (Cb - 0.5)

- the accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.

- the input and output data lines are 8-bit.

- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

Input/Output Data

The levels are as follows:

FIL1 : luminance signal Y
: 0 IRE; black, quantization level 16
100 IRE; white, quantization level 235

FIL2 : multiplexed colour difference signals Cr
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

FIL3 : multiplexed colour difference signals Cb
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

The data rate on the input is maximum 16 MHz

The levels at the input and output, for some specific colour patterns, are given in Table 17.

CONTROL SIGNALS

$\overline{\text{MATBYPASS}}$ = 1 : matrix in use
= 0 : matrix bypassed

Functional description

Four ROMs are used to obtain the coefficients with the required accuracy.

In the advent of non-standard input levels the limiter reduces the possible data values at the output (red, green, blue channel) to values between 0 and 255. Consequently, all negative values are set to 0 and all values higher than 255 are set to 255.

Table 17 Levels at the functional blocks

test number	Y FIL1	CR FIL2	CB FIL3	MAT1 R	MAT2 G	MAT3 B
1 (white)	235	128	128	235	235	235
2 (black)	16	128	128	16	16	16
3 (red)	82	240	90	235	16	16
4 (green)	145	34	54	16	236	16
5 (blue)	41	110	240	16	16	235

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

Functional description

The $\overline{\text{VLUTLOAD}}$ signal enables the memories to obtain data from the VLUTDATA signal via the I²C-bus (auto-increment mode). The three RAMs will also obtain the same data.

$\overline{\text{VLUTBYPASS}}$ will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as Colour Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.
The Gamma-correction function (also known as Gradation) is given as;

$Y = X^{\gamma}$

The VLUT's are realized by 256 x 8-bit RAMs.

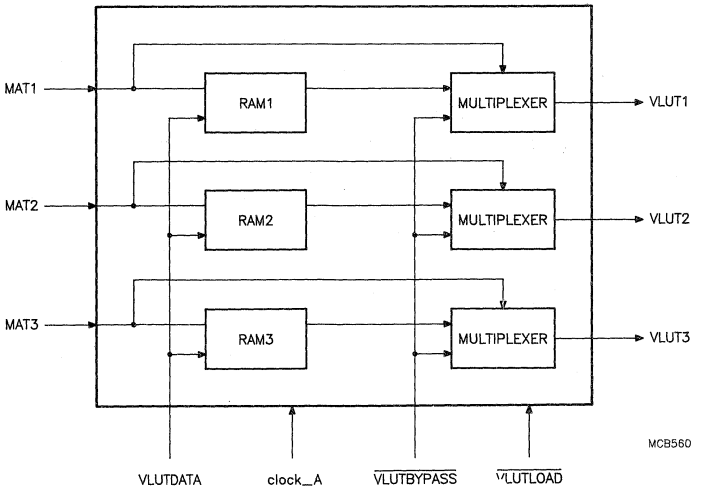


Fig.17 Block diagram video look up table.

I²C-bus receiver

Functional description

At switch-on all internal control signals are at undefined values and the I²C-bus receiver must, therefore, be reset by the external $\overline{\text{RESET}}$ signal. After reset the control signals will be set as follows:

IICOE	= logic 1	$\overline{\text{OE}}$ enabled
FMTCNTRL	= 4	format 4:4:4
$\overline{\text{MATBYPASS}}$	= logic 0	matrix bypassed
$\overline{\text{VLUTLOAD}}$	= logic 1	VLUT at read operation
$\overline{\text{INRESET}}$	= logic 0	input data set to fixed values

Receiver organisation

The address for the DCSC is as follows:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	0	0	0	X	0

R/W: write only

A0: hardware programmable address bit

S	DCSC ADDRESS	A	SUB-ADDRESS	A	DATA BYTE	A	P

where S = start
A = acknowledge
P = stop

Table 18 Sub-address and data byte formats

HEX SUBADD	BINARY - DATA								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
00	X	X	X	X	X	0	0	0	input formatter to Format 1
00	X	X	X	X	X	0	0	1	input formatter to Format 2
00	X	X	X	X	X	0	1	0	input formatter to Format 3
00	X	X	X	X	X	0	1	1	input formatter to Format 4
00	X	X	X	X	X	1	0	0	input formatter to Format 5
00	X	X	X	X	0	X	X	X	matrix bypassed
00	X	X	X	X	1	X	X	X	matrix in use
00	X	X	X	0	X	X	X	X	input data at fixed values
00	X	X	X	1	X	X	X	X	input data to formatter
00	X	X	1	X	X	X	X	X	$\overline{OE}$ enabled
00	X	X	0	X	X	X	X	X	output stages 3-state
00	X	0	X	X	X	X	X	X	VLUT write enabled
00	X	1	X	X	X	X	X	X	VLUT read enabled
01	X	X	X	X	X	X	X	X	VLUTDATA

where;

D0 to D2 = FMTCONTROL
D3 = $\overline{MATBYPASS}$
D4 = $\overline{INRESET}$
D5 = IICOE
D6 = $\overline{VLUTLOAD}$
D7 = not used

Philips Components

Data sheet	
status	Preliminary specification
date of issue	April 1991

SAA7197

Clock signal generation circuit (SCGC) for Desktop Video systems

FEATURES

- PLL frequency multiplier
- Two different clock frequencies
- Power fail detection circuit

APPLICATIONS

- Desktop video systems

GENERAL DESCRIPTION

The SAA7197 is a clock generation circuit (SCGC) which generates all clock signals required for a desktop video system utilizing the SAA719X family of devices. The circuit operates in either the phase-locked-loop mode (PLL) or voltage controlled oscillator mode (VCO).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	-	5.5	V
I_{DD}	digital supply current	10	-	60	mA
I_{DDA}	analog supply current	5	-	*	mA
$P_{tot(c)}$	total power consumption	-	-	0.4	W
T_{amb}	operating ambient temperature range	0	-	70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197P	20	DIL	plastic	SOT146
SAA7197T	20	SO20	plastic	SOT163A

* Value to be fixed.

Clock signal generation circuit (SCGC) for Desktop Video systems

SAA7197

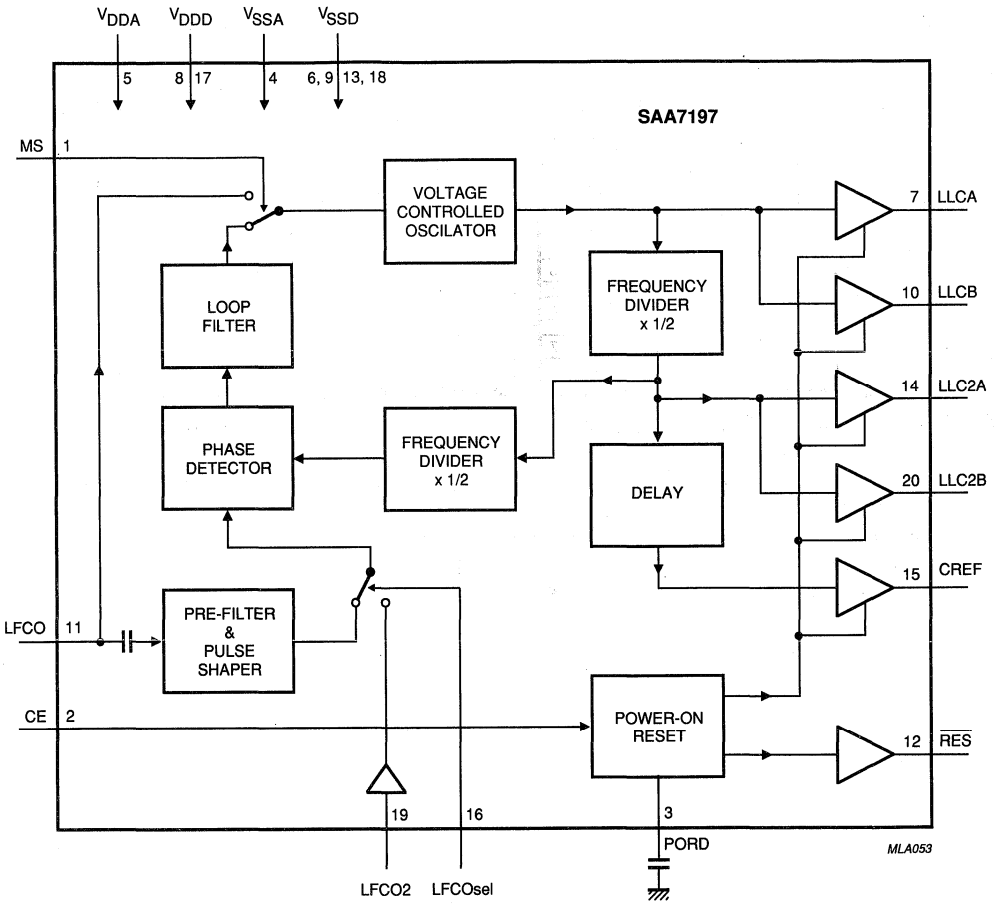


Fig.1 Block diagram.

PIN CONFIGURATION

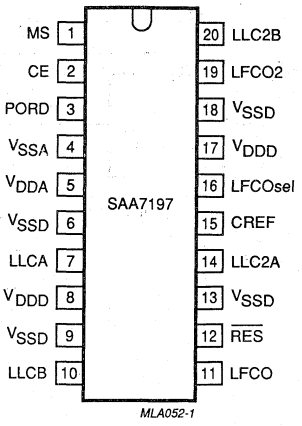


Fig.2 Pin configuration.

Clock signal generation circuit (SCGC) for Desktop Video systems

SAA7197

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	Mode Select input. Usually this input is LOW and the SCGC generates the different clocks using the LFCO or LFCO2 as reference frequency
CE	2	Chip Enable input. A HIGH level at CE enables the output buffers; a LOW level sets the clock buffers to HIGH and $\overline{RES}$ to LOW. The VCO operates on an internally adjusted frequency
PORD	3	Power-On Reset Delay. An external capacitor at this pin determines the duration of the reset state (see $\overline{RES}$)
V_{SSA}	4	Analog ground
V_{DDA}	5	Analog power supply
V_{SSD}	6	Digital ground
LLCA	7	LLCA is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
V_{DDD}	8	Digital power supply
V_{SSD}	9	Digital ground
LLCB	10	LLCB is a line-locked clock output signal of 4 times the LFCO or LFCO2 input frequency. The waveform is rectangular
LFCO	11	Line Frequency COntrol input. This signal received from the DMSD-SQP, is a multiple of the line frequency. It is the reference frequency for all clocks generated by the SCGC
$\overline{RES}$	12	RESET output (active LOW). This output indicates the reset state. After a power-ON or power failure $\overline{RES}$ goes LOW and remains in this state for a period that is determined by the external capacitor connected to pin PORD. If the supply voltage decreases below the operating range (power failure)*, $\overline{RES}$ goes LOW. After the power supply returns within the operating range and the POR delay is completed, $\overline{RES}$ goes HIGH. This signal can be used to reset the entire digital TV system. When CE is LOW, the $\overline{RES}$ output will be set LOW
V_{SSD}	13	Digital ground
LLC2A	14	LLC2A is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular
CREF	15	CLocK reference signal for Desktop Video system. This output is a clock qualifier signal of 2 times the LFCO or LFCO2 input frequency for bus clock generation
LFCOsel	16	Line Frequency COntrol select. This input signal selects either the LFCO signal from the DMSD (LFCOsel = LOW) or a TTL-compatible LFCO2 signal (LFCOsel = HIGH)
V_{DDD}	17	Digital power supply
V_{SSD}	18	Digital ground
LFCO2	19	Line Frequency COntrol 2 input. This signal received from an external line reference source, is a multiple of the line frequency. It is the TTL-compatible reference frequency for all clocks generated by the SCGC
LLC2B	20	LLC2B is a line-locked clock output signal of 2 times the LFCO or LFCO2 input frequency. The waveform is rectangular

* See section "**APPLICATION INFORMATION**"; Fig.4, reset waveform.

Clock signal generation circuit (SCGC) for Desktop Video systems

SAA7197

FUNCTIONAL DESCRIPTION

The SAA7197 generates all clock signals required for a desktop video system utilizing the SAA719X family of devices. These consist of the ADC8 (8-bit Analog-to-Digital Converter), DMSD-SQP (Digital Multi-Standard Decoder - for Square Pixel applications), and DCSC (Digital Colour Space Converter) and optional extensions. In conjunction with memory controllers this completes a system for desktop video applications.

The main function of the SCGC is a PLL which multiplys an incoming reference signal (LFCO or LFCO2) by the factors 2 and 4. The LFCO signal is a digital-to-analog converted signal provided by the DMSD-SQP's horizontal PLL. It is a multiple of the line frequency of 360 x f_H (6.14 MHz) with 60 Hz standards or 472 x f_H (7.38 MHz) with 50 Hz standards. Alternatively, the LFCO2 input can be used for TTL compatible signals from an external reference source.

The output signals from the PLL are LLCA and LLCB (4 x f_{LFCO}) and LLC2A and LLC2B (2 x f_{LFCO}). The waveforms are rectangular with a duty factor of 50%. The CREF output at 2 x f_{LFCO} is for controlling the internal clock dividers of the DMSD2-SQP chip family. The clock outputs of equal frequencies may be connected together externally.

The $\overline{RES}$ output signal indicates a stable power supply. This output can be used to drive other power-on reset circuits. An external capacitor, connected to pin 3 (PORD), determines the reset time. The clock signal output lines go HIGH during an internal power-on reset period.

The internal reset cycle is shorter than the external reset cycle. This is to ensure that the clock signals are delivered before $\overline{RES}$ goes HIGH. If the clock signals must be within a specified range before $\overline{RES}$ goes HIGH, it is important to apply the LFCO signal before the LOW-to-HIGH transition.

The power-on reset circuit is combined with a power failure detector.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}/V_{DDA}	supply voltage		−0.5	7.0	V
V_I	input voltage		−0.5	7.0	V
V_O	output voltage	I_{OM} = 20 mA	−0.5	7.0	V
P_{tot}	total power dissipation		-	1.1	W
T_{stg}	storage temperature range		-55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 5.5$ to 8.0 MHz; $T_{amb} = 0$ to +70 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DDD}	digital supply voltage		4.5	5.5	V
I_{DDD}	digital supply current		10	60	mA
V_{DDA}	analog supply voltage		4.5	5.5	V
I_{DDA}	analog supply current		3	*	mA
Inputs MS, CE, LFCO and LFC02					
I_{IL}	input leakage current		-	10	µA
MS, CE, LFCOsel and LFCO2					
C_I	input capacitance		-	5	pF
LFCO					
C_I	input capacitance		-	10	pF
CE, LFCOsel and LFCO2					
V_{IL}	input voltage LOW		0	0.8	V
V_{IH}	input voltage HIGH		2.0	V_{DDD}	V
LFCO2					
f_{LFCO2}	input frequency		5.5	8.0	MHz
LFCO					
V_{LFCO}	input voltage		0	V_{DDA}	V
f_{LFCO}	input frequency		5.5	8.0	MHz
$V_{LFCO(p-p)}$	input signal amplitude (peak-to-peak value)		1.0	V_{DDA}	V
Outputs LLCA, LLCB, LLC2A, LLC2B and CREF					
V_{OH}	output voltage HIGH	CE = LOW; $I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
RES					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.4	V
t_d	delay time (see Fig.4)	$C_{PORD} = 100$ nF	20	200	ms
CREF					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
C_L	output load capacitance		15	40	pF
t_{HD}	output hold time	note 1	4	-	ns
t_{SU}	output set-up time		12	-	ns

* Value to be fixed.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Outputs (continued) LLCA, LLCB, LLC2A and LLC2B					
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	V_{DDD}	V
V_{OL}	output voltage LOW	$I_{OL} = 2.0$ mA	0	0.6	V
	output frequency				
f_{LLCA}	LLCA		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
f_{LLCB}	LLCB		-	$4f_{LFCO}$ or $4f_{LFCO2}$	MHz
f_{LLC2A}	LLC2A		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
f_{LLC2B}	LLC2B		-	$2f_{LFCO}$ or $2f_{LFCO2}$	MHz
t_r	rise time	0.6 V to 2.6 V	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	5	ns
t_{comp}	composite rise time	note 2	-	8	ns
LLCA, LLCB, LLC2A and LLC2B					
	duty factor	notes 1 and 3			
K_{CLK1}	LLCA and LLCB		0.43	0.57	
K_{CLK3}	LLC2A and LLC2B		0.43	0.57	

Notes to the characteristics

1. $f_{LFCO} = 8$ MHz, with a 40 pF output load (typically 6.75 MHz); see Fig.3.

2. The composite rise time is the time duration from all clocks = LOW to all clocks = HIGH (within 0.6 V to 2.6 V, includes rise time, skew and jitter). Skew between two LLX - clocks will not deviate more than ± 2 ns if the output loads are matched within 20%.

3. The duty factor is mean value and defined at 1.5 V.

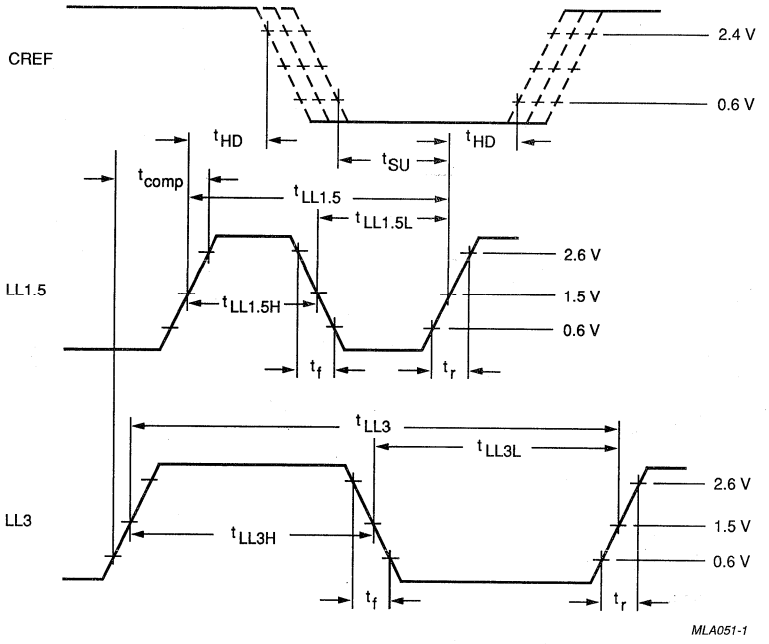


Fig.3 Timing waveform.

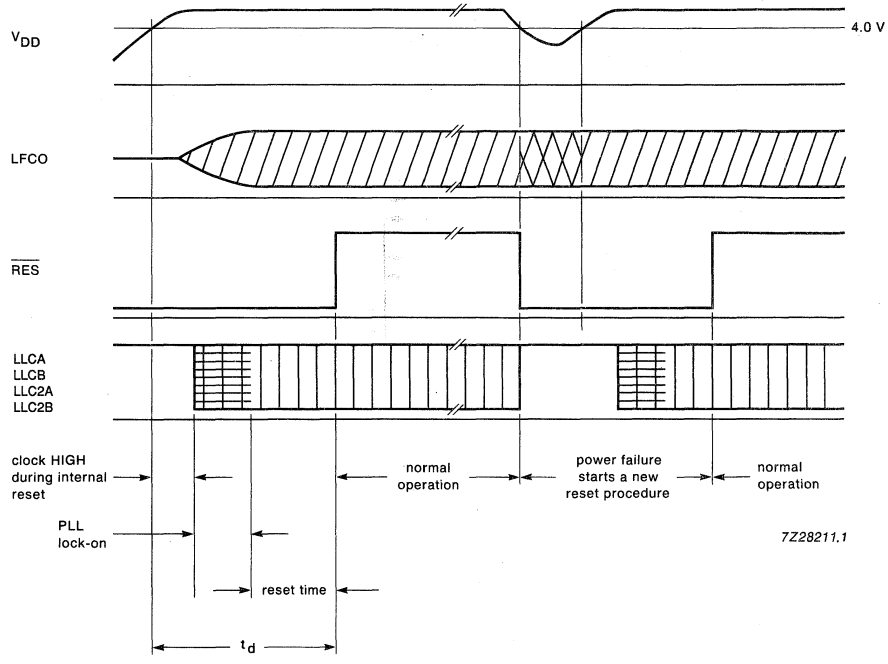


Fig.4 Reset waveform.

TELETEXT IC FOR ANALOG AND DIGITAL TV

GENERAL DESCRIPTION

The SAA9042 is a CMOS integrated circuit designed for reception, decoding and display of 625 and 525 line World System Teletext (WST).

It is used in conjunction with a teletext video processor (SAA5235/6 or SAA5191) for data regeneration, and a single-chip 64 K x 4-bit or 256 K x 4-bit dynamic RAM page memory.

The SAA9042 acquires teletext packets defined at levels 1, 2 and 3 in the WST specification and produces a level 1 display.

The device is μC controlled via the standard I^{2}C-bus and is compatible with analog, digital and features TV.

Features

General

- Interfaces with the Philips digital TV chip-set
- Interfaces with analog TV
- Directly interfaces up to 1 Mbit dynamic RAM
- Fully independent acquisition and display timing
- 3 display modes
  - normal
  - 32 kHz (progressive scan)
  - 100 Hz/120 Hz (field doubling)
- I^{2}C controlled
- Single 5 V power supply

Acquisition

- Simultaneous update of up to 8 pages
- Up to 100 page background memory capability
- Software selectable 625/525 line operation
- Full level One Features (FLOF) operation
- TOP compatible
- VPT compatible
- VBI and full channel operation
- Extension packets 26/27/28/29 and 30 fully decoded

Display

- Stable display by slaving from scan-related timing signals
- Automatic selection of six different languages
- Storage of 192 characters (13 x 10 dot matrix)
- Software controlled RGB level removes the need for hardware adjustment
- Up to 27 display rows; 0 to 24 and up to 2 status rows

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

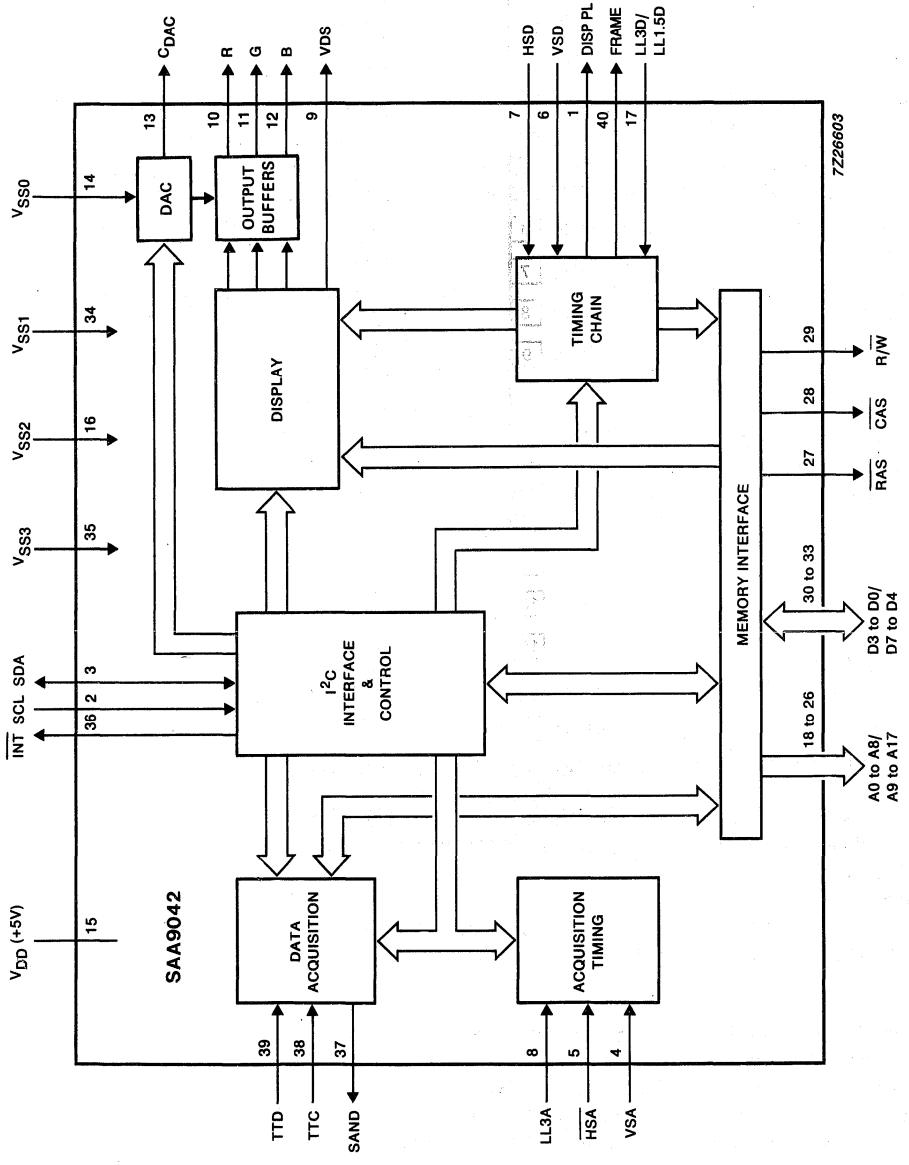


Fig.1 Block diagram.

PINNING

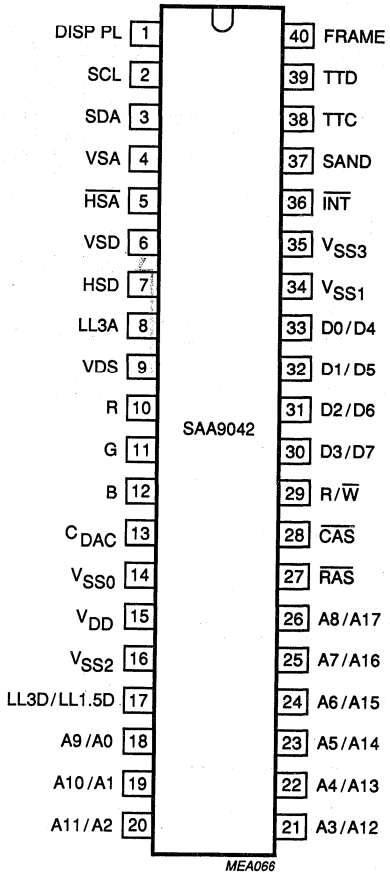


Fig.2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	DISP PL	**Display PL:** a programmable decode from the display-timing chain which can be used as a reference signal in an external PLL in scan-locked applications.
2	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
3	SDA	**Serial Data:** is the I^2C-bus data line connected to the microcontroller. It is an input/output function with an open-drain output.
4	VSA	**Vertical Synchronization Acquisition:** vertical synchronization signal from the SAA9051 (VS) or SAA5191 (VCS), derived from the incoming video. This input enables field timing to be established in the acquisition section.
5	$\overline{\text{HSA}}$	**Horizontal Synchronization Acquisition:** horizontal synchronization signal derived from the incoming video e.g. burst gate pulse. This active LOW input enables line timing to be established in the acquisition section.
6	VSD	**Vertical Synchronization Display:** synchronization signal indicating the vertical position of the TV picture. This input allows field synchronization of the display section.
7	HSD	**Horizontal Synchronization Display:** synchronization signal indicating the horizontal position of the TV picture. This input allows line synchronization of the TV picture.
8	LL3A	**Line-Locked system clock:** 13.5 MHz system clock input for the acquisition section.
9	VDS	**Video/Data Switch:** push-pull active HIGH 3-state output which controls the switching between text (HIGH) and normal TV (LOW) picture for both normal text and superimposed displays.
10	R	**Red, Green, Blue:** analog 3-state outputs which contain video character and background information for text display. The output level is adjustable over 16 steps and is controlled by V_{SS0}, V_{DD} and an internal register.
11	G	
12	B	
13	C_{DAC}	**DAC output:** DAC output level, requires an external decoupling capacitor not less than 1 μF.
14	V_{SS0}	**Ground:** ground connection for video outputs.
15	V_{DD}	**Power Supply:** + 5 V (typ.).
16	V_{SS2}	**Ground:** ground connection.
17	LL3D/ LL1.5D	**Line-Locked system clock:** 13.5 MHz or 27 MHz system clock input for the display, memory interface and control sections.
18 to 26	A0 to A8/ A9 to A17	**Address:** multiplexed address outputs for the external nibble-wide dynamic RAM (DRAM). With a 64-Kbit (16 K x 4) DRAM the address A8 pin is not used.
27	$\overline{\text{RAS}}$	**Row Address Strobe:** active LOW output for the external DRAM.
28	$\overline{\text{CAS}}$	**Column Address Strobe:** active LOW output for the external DRAM.
29	R/$\overline{\text{W}}$	**Read/Write:** active LOW write enable signal for the external DRAM.

pin no.	mnemonic	description
30 to 33	D3 to D0/ D4 to D7	**Data:** data inputs/outputs to and from the external nibble-wide DRAM.
34	V_{SS1}	**Ground:** ground connection.
35	V_{SS3}	**Ground:** ground connection.
36	$\overline{INT}$	**Interrupt:** open-drain active LOW output which provides an interrupt signal for a microprocessor indicating the arrival of a page or packet in any one of the acquisition channels, change in newsflash/subtitle status or power-on reset.
37	SAND	**Sandcastle:** 3-level output for the SAA5191 or SAA5236 representing the PL/$\overline{CBB}$ signal, derived from the acquisition timing chain.
38	TTC	**Teletext Clock:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor.
39	TTD	**Teletext Data:** input from the SAA5191 or SAA5236 supplied via an external coupling capacitor, internally clamped to V_{SS} for 4 to 8 μs of each line to maintain the correct DC level.
40	FRAME	**Frame:** output for de-interlacing ciruits. The signal is LOW for even fields and HIGH for odd fields when text but no picture is displayed. It is forced LOW when a TV picture is present.

DEVELOPMENT DATA

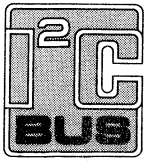
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.5	+ 6.5	V
DC input voltage	V_I	−0.5	V_{DD} + 0.5	V
DC input current	I_I	−20	+ 20	mA
DC output voltage	V_O	−0.5	V_{DD} + 0.5	V
DC output current	I_O	−20	+ 20	mA
DC V_{DD} current	I_{DD}	*	*	mA
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Electrostatic handling**	V_{es}	−1000	+ 1000	V

Notes to the ratings

1. All voltages are with respect to V_{SS}.
2. V_{SSO} is considered as an output.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Value to be fixed.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	note 1	V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	–	100	–	mA
Inputs	note 2					
TTD	note 3					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	22	50	nF
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input data set-up time	note 5	$t_{SU;DAT}$	40	–	–	ns
Input data hold time	note 5	$t_{HD;DAT}$	40	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	7	–	pF
Clamp start time	note 6	t_{CLon}	3.5	4.0	4.5	μs
Clamp finish time	note 6	t_{CLoff}	7.5	8.0	8.5	μs
Clamp output current	note 7	I_{clamp}	1.0	–	–	mA
TTC	note 8					
Input voltage						
(peak-to-peak value)		$V_{I(p-p)}$	2.0	–	5.0	V
External coupling capacitor		C_{ext}	–	10	10	nF
Peak input current		I_{IM}	−10	–	+ 10	mA
Input peaks relative to 50% duty factor		$\pm V_{IM}$	0.2	–	3.5	V
Input rise and fall times	notes 4 and 26	t_r, t_f	10	–	80	ns
Input capacitance	note 26	C_I	–	7	–	pF
Input clamp voltage		V_{clamp}	1.2	1.4	1.6	V
Clock frequency						
625 line		f_{TTC}	–	6.9375	–	MHz
525 line		f_{TTC}	–	5.7272	–	MHz

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (continued)	note 2					
$\overline{HSA}$	note 9					
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSA						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH	note 27	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3A (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
LL3A cycle time	note 10	t_{CA}	69	74	80	ns
LL3A HIGH time		t_{CAH}	28	–	–	ns
LL3A LOW time		t_{CAL}	28	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3A (AC mode)	13.5 MHz					
Mean voltage level	notes 25 and 26	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
SCL						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	note 26	C_I	–	–	7	pF
HSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	50	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
VSD						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	500	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
LL3D (TTL mode)						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times	notes 4 and 26	t_r, t_f	–	–	10	ns
LL3D cycle time						
13.5 MHz		t_{CA}	69	74	80	ns
27.0 MHz		t_{CA}	35	37	40	ns
LL3D HIGH time						
13.5 MHz		t_{CAH}	28	–	–	ns
27.0 MHz		t_{CAH}	14	–	–	ns
LL3D LOW time						
13.5 MHz		t_{CAL}	28	–	–	ns
27.0 MHz		t_{CAL}	14	–	–	ns
Input leakage current	V_I = 0 to V_{DD}	I_{LI}	−100	–	+ 100	μA
Input capacitance	note 26	C_I	–	–	10	pF
LL3D (AC mode)						
Mean voltage level	notes 25 and 26	V_{ACM}	−12	–	+ 12	V
AC voltage (peak-to-peak value)		$V_{AC(p-p)}$	1.0	–	3.0	V
Voltage HIGH w.r.t. mean		V_{ACH}	0.3	–	2.0	V
Voltage LOW w.r.t. mean		V_{ACL}	−2.0	–	−0.3	V
Input mark/space ratio w.r.t. mean t_{ACH}: t_{ACL} or t_{ACL} : t_{ACH}	note 28		30 : 70	–	70 : 30	
Series capacitor		C_S	47	100	220	pF
Input impedance	notes 24 and 26	Z_{ACI}	10	–	–	kΩ
Inputs/Outputs (I/O)	note 13					
SDA (open drain I/O)						
Input voltage LOW		V_{IL}	0	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
SDA (open drain I/O) (continued)						
Input rise time	notes 4 and 26	t_r	–	–	1	μs
Input fall time	notes 11 and 26	t_f	–	–	300	ns
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	0	–	0.4	V
Output fall time	notes 11 and 26	t_f	–	–	300	ns
Load capacitance		C_L	–	–	400	pF
D3 to D0						
Input voltage LOW		V_{IL}	0	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	V_{DD}	V
Input leakage current	note 12; V_I = 0 to V_{DD}; (with output off)	I_{LI}	−10	–	+ 10	μA
Input capacitance	note 26	C_I	–	–	7	pF
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 21	C_L	–	–	100	pF
Outputs	note 13					
SAND	note 22					
Output voltage LOW	I_{OL} = 0.2 mA	V_{OL}	0	–	0.3	V
Output voltage INTERMEDIATE	$\pm I_{OI}$ = 30 μA	V_{OI}	1.3	–	2.7	V
Output voltage HIGH	I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 1.1 V	note 26	t_r, t_f	–	–	400	ns
Output rise time V_{OL} to V_{OH} between 2.9 V and 4.0 V	note 26	t_r, t_f	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4.0 V and 0.4 V	note 26	t_r, t_f	–	–	50	ns
Load capacitance		C_L	–	–	30	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{INT}$ (open-drain output)						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output leakage current	output off; V_{PU} = 0 to V_{DD}	I_{LO}	−10	–	+ 10	μA
Output fall time	notes 15 and 26	t_f	–	–	50	ns
Load capacitance		C_L	–	–	100	pF
A0 to A8						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
$\overline{RAS}$, $\overline{CAS}$, R/$\overline{W}$						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 1.8 V	note 26	t_r, t_f	–	–	10	ns
Load capacitance	note 23	C_L	–	–	100	pF
DISP PL, FRAME						
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times	notes 16 and 26	t_r, t_f	–	–	200	ns
Load capacitance		C_L	–	–	200	pF
R, G, B (3-state)	note 29					
Output voltage LOW	note 17; I_{OL} = 2.0 mA	V_{OL}	V_{SS0}	–	V_{SS0}+0.2	V
Output voltage HIGH	note 18; I_{OH} = −2 mA	V_{OH}	–	*	–	V
Output rise and fall times between 0.6 V and 1.8 V	notes 4, 17 and 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output capacitance	OFF state; note 26	C_{off}	–	–	10	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA
VDS (3-state)	note 29					
Output voltage LOW	I_{OL} = 1.0 mA	V_{OL}	0	–	0.2	V
Output voltage HIGH	I_{OH} = −200 μA	V_{OH}	1.1	–	2.8	V
Output rise and fall times	note 26	t_r, t_f	–	–	10	ns
Load capacitance		C_L	–	–	30	pF
Output leakage current	OFF state; V_I = 0 to V_{DD}	I_{off}	−10	–	+ 10	μA

* Adjustable over 0.5 to 1.5 V, via the I^2C-bus.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
I²C-bus	note 20					
SCL clock frequency		f_{SCL}	0	–	100	kHz
Input clock period						
HIGH time		t_{HIGH}	4	–	–	μs
LOW time		t_{LOW}	4	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop set-up time from clock HIGH		$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop		t_{BUF}	4	–	–	μs
Start hold time		$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock LOW-to-HIGH transition		$t_{SU;STA}$	4	–	–	μs
Memory interface	note 14					
Cycle time		t_{CY}	–	481	–	ns
Transition time		t_T	–	–	10	ns
$\overline{RAS}$ pulse width		$t_{W;RAS}$	120	–	–	ns
$\overline{RAS}$ pre-charge time		$t_{PC;RAS}$	90	–	–	ns
$\overline{CAS}$ hold time		$t_{HD;CAS}$	120	–	–	ns
Page mode cycle time		$t_{CY;PM}$	120	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_d	25	–	–	ns
$\overline{CAS}$ pulse width		$t_{W;CAS}$	60	–	–	ns
$\overline{CAS}$ pre-charge time		$t_{PC;CAS}$	50	–	–	ns
Row address set-up time		$t_{SU;ROW}$	0	–	–	ns
Row address hold time		$t_{HD;ROW}$	15	–	–	ns
Column address set-up time		$t_{SU;COL}$	0	–	–	ns
Column address hold time		$t_{HD;COL}$	20	–	–	ns
Read command set-up time		$t_{SU;RD}$	0	–	–	ns
Read command hold time referenced to $\overline{CAS}$		$t_{HD;RDC}$	0	–	–	ns
Read command hold time referenced to $\overline{RAS}$		$t_{HD;RDR}$	10	–	–	ns
Access time from $\overline{CAS}$		$t_{ACC;CAS}$	–	–	60	ns

parameter	conditions	symbol	min.	typ.	max.	unit
Write command pulse width		$t_{W;WR}$	50	–	–	ns
Write command hold time		$t_{HD;WR}$	40	–	–	ns
Data-in set-up time		$t_{SU;DATI}$	0	–	–	ns
Data-in hold time		$t_{HD;DATI}$	40	–	–	ns
Access time from $\overline{RAS}$		$t_{ACC;RAS}$	–	–	120	ns
$\overline{RAS}$ hold time after $\overline{CAS}$		$t_{HD;RC}$	60	–	–	ns
$\overline{CAS}$ to $\overline{RAS}$ pre-charge time		$t_{PC;CR}$	20	–	–	ns
Column address hold time referenced to $\overline{RAS}$		$t_{HD;COLR}$	80	–	–	ns
Data-in hold time referenced to $\overline{RAS}$		$t_{HD;DATIR}$	100	–	–	ns

Notes to the characteristics

1. The rise time of V_{DD} from 0 to 4.5 V must be >150 ns to ensure that the internal power-on reset triggers. For this circuit to reset the chip, V_{DD} must be initially <1.0 V or fall to <1.0 V for at least 100 ns. Spikes on V_{DD} are tolerable provided that V_{DD} is not reduced to <2.5 V.
2. All inputs are protected against static charge under normal handling.
3. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor.
4. Rise and fall times are measured between 10% and 90% levels.
5. Teletext input data set-up and hold times are measured with respect to 50% duty factor level of the rising edge of the teletext clock input (TTC). Data stable $1 \geqslant 2.0$ V, data stable $0 \leqslant 0.8$ V.
6. Clamp times measured from the line sync reference point, assuming acquisition timing is set correctly.
7. Clamp transistor on, $V_{TTD} - V_{SSI} \leqslant 0.1$ V.
8. The TTC input has an internal clamping diode.
9. HSA is falling edge triggered.
10. Minimum and maximum cycles times are ± 7.1% of the typical value.
11. Fall time is measured between 3.0 V and 1.5 V.
12. Applies even when $V_{DD} = 0$ V.
13. All input/outputs and outputs are protected against static charge under normal handling.
14. For details of memory interface timings to and from external DRAM see Fig. 5 and Fig. 6.

DEVELOPMENT DATA

Notes to the characteristics (continued)

15. Output fall time measured between 4.0 V and 1.0 V levels with a 3.3 kΩ load to 5.0 V.
16. Output rise and fall times measured between 0.8 V and 2.0 V levels.
17. Measured with $V_{SSO} = V_{SS}$ and output voltage (C_{DAC}) = 1.5 V.
18. Measured with $V_{SSO} = V_{SS}$ and output voltage (C_{DAC}) = 0.5 V to 1.5 V.
19. Skew delay time measured at 0.7 V levels.
20. For details of I²C-bus timings see Fig. 3; timings are referred to V_{IH} = 3.0 V and V_{IL} = 1.5 V.
21. Load capacitance measured with two DRAM data inputs; 50 pF maximum.
22. A current of 1 μA flows out of the SAA5191 or SAA5236 while its SAND input is in the range of 1 V to 3.5 V.
23. Load capacitance measured with eight DRAM data inputs; 80 pF maximum.
24. Through a 200 pF capacitor with a 13.5 MHz sinewave.
25. To be applied via the series capacitor only.
26. This specification point is included because of its importance to the application environment; it is not however guaranteed.
27. When connected to the SAA5191, it is acceptable for the clock frequency to initially attain ⩽ 15 MHz in order to achieve synchronism.
28. When connected to the SAA5191, it is acceptable for the input voltage to attain V_{DD} + 0.9 V. The input current must be restricted as specified in the RATINGS.
29. These outputs can be made 3-state via the I²C-bus.

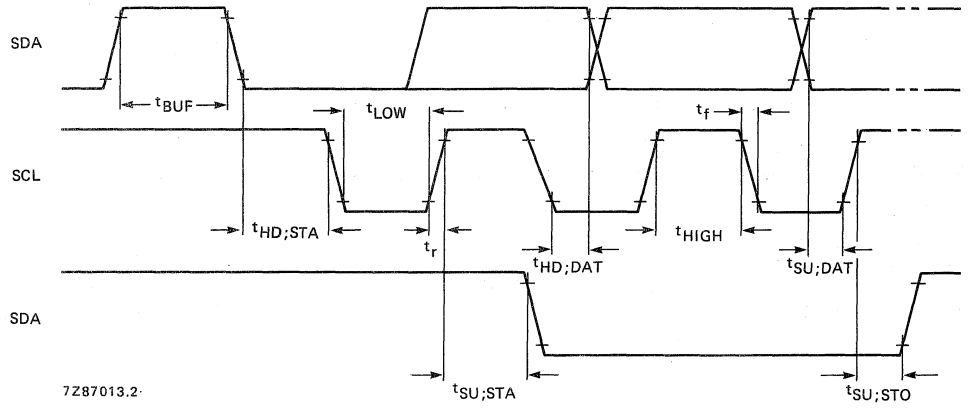


Fig.3 I²C-bus timing.

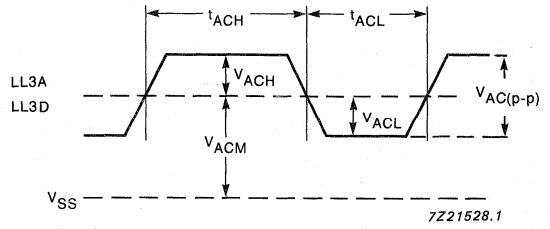


Fig.4 Line-Locked system clock LL3A and LL3D timing diagram.

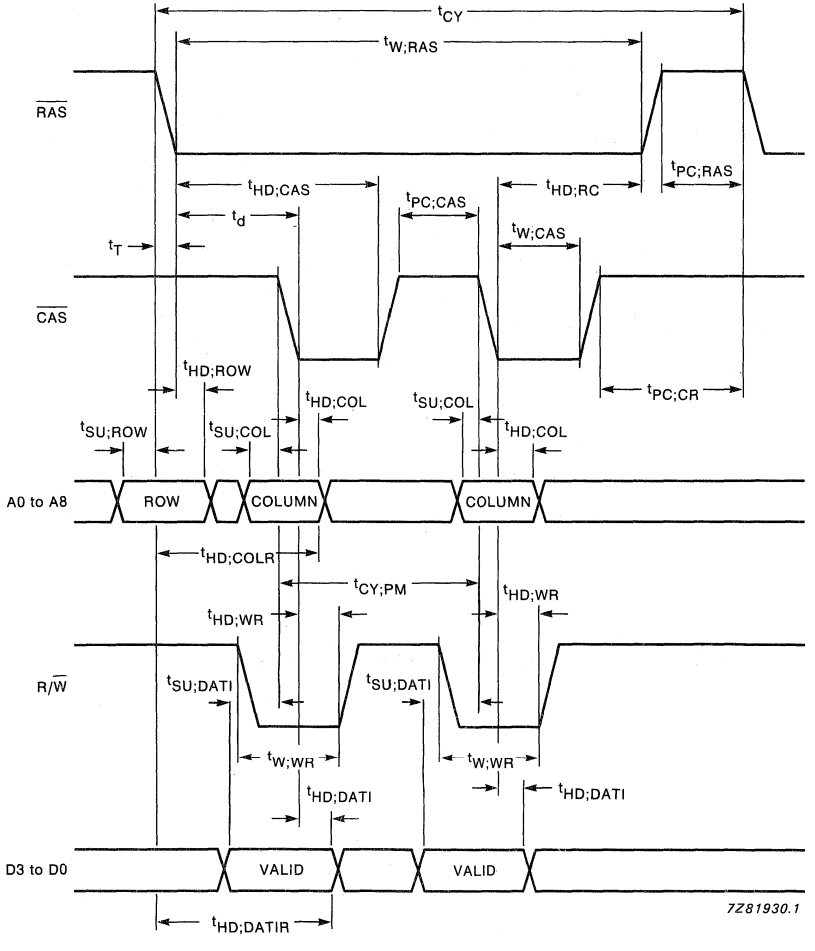


Fig.5 Memory interface timing for write cycle to external DRAM.

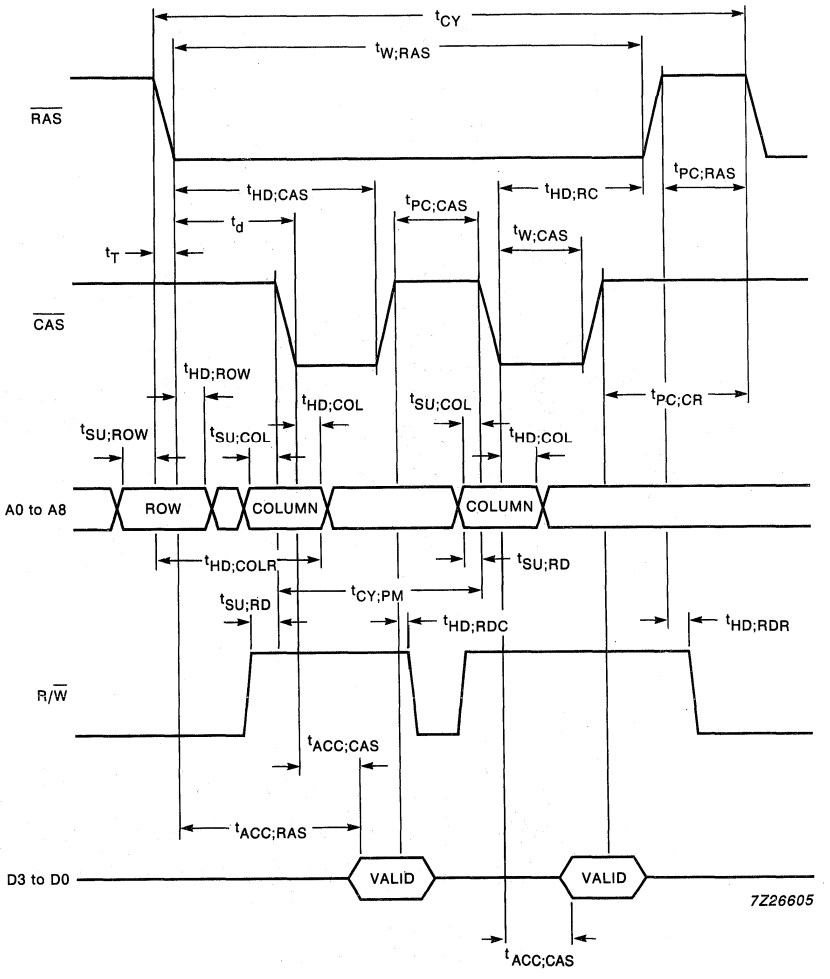
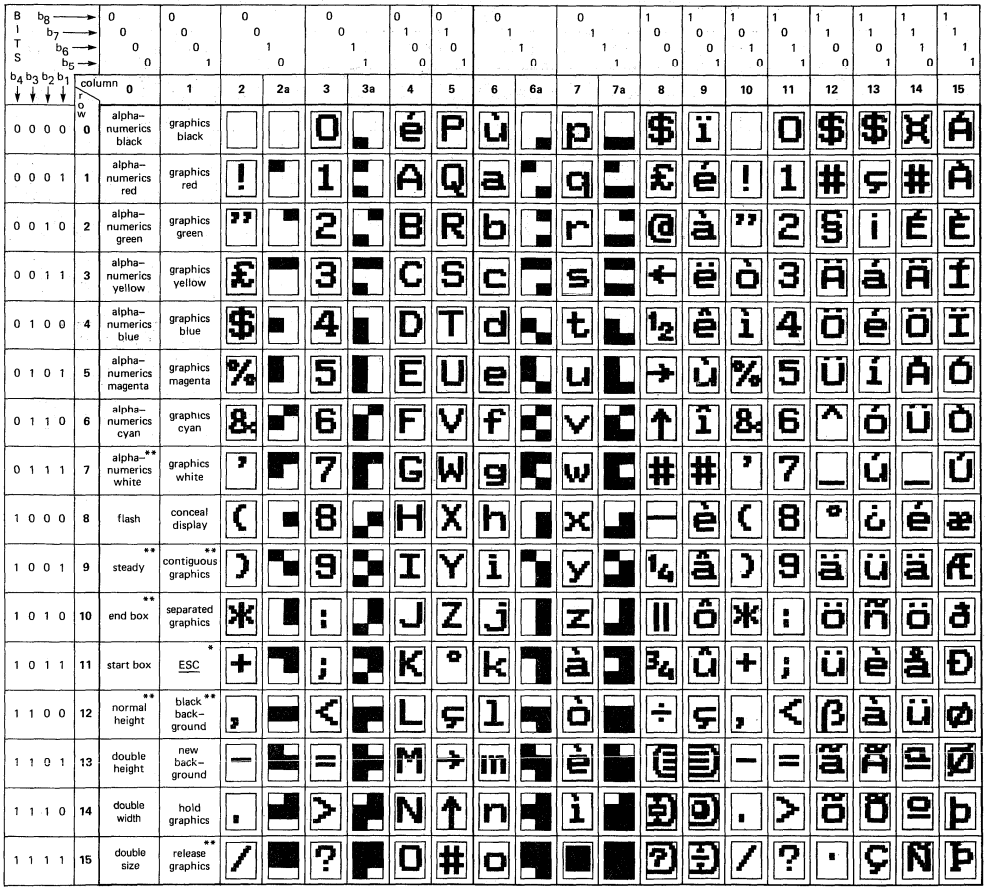


Fig.6 Memory interface timing for read cycle from external DRAM.

DEVELOPMENT DATA



*These control characters are reserved for compatability with other data codes.

**These control characters are presumed before each row begins.

Fig.7 SAA9042A West European character set.

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à

7Z22659.2

(1) Where PHCB are the page Header Control Bits.
Other combinations of PHCB default to English.

Fig.8 SAA9042A West European national option sets.

APPLICATION INFORMATION

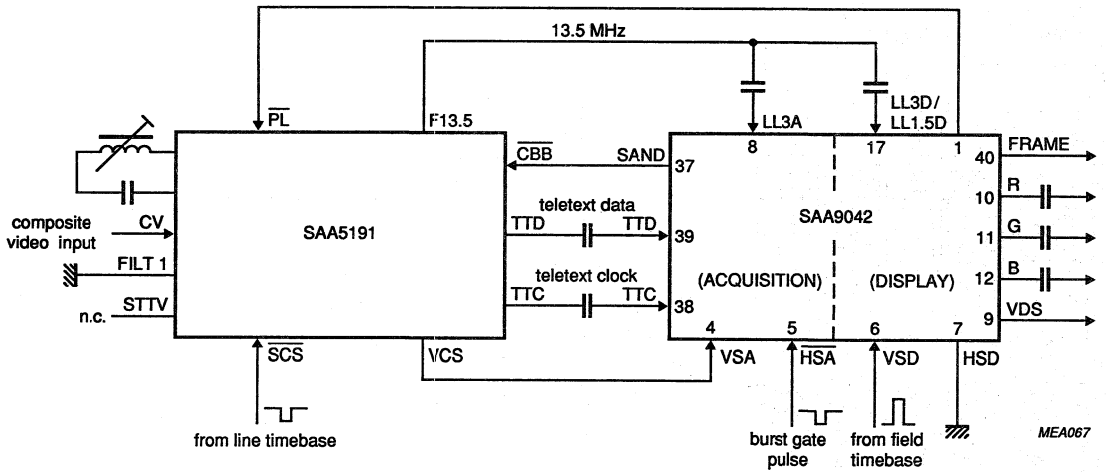


Fig.9 Synchronization of SAA9042 in analog TV (slave sync mode).

APPLICATION INFORMATION (continued)

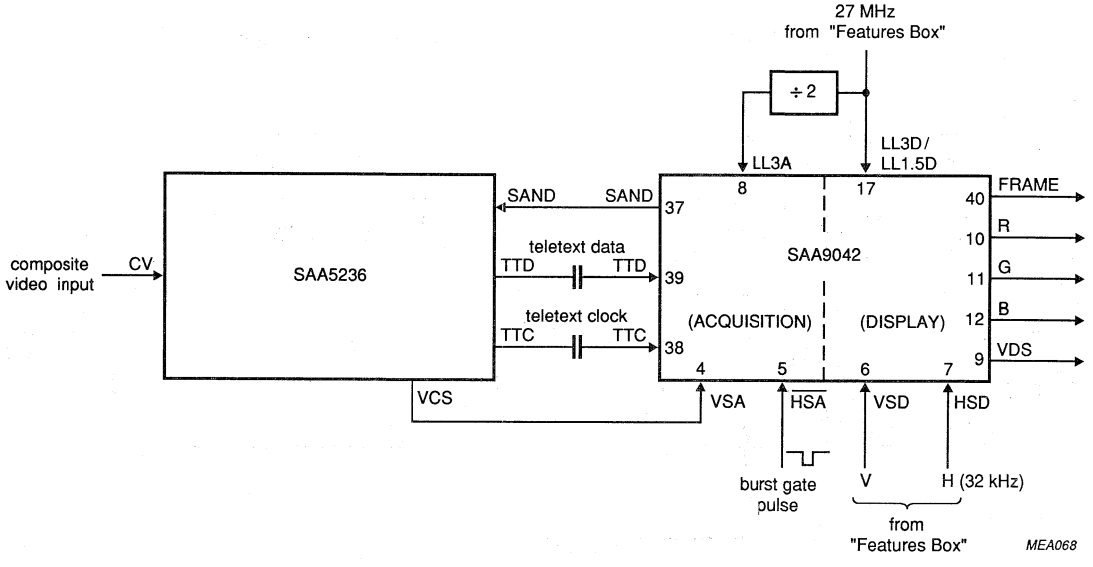


Fig.10 Synchronization of SAA9042 in analog TV with 2 x H features.

DEVELOPMENT DATA

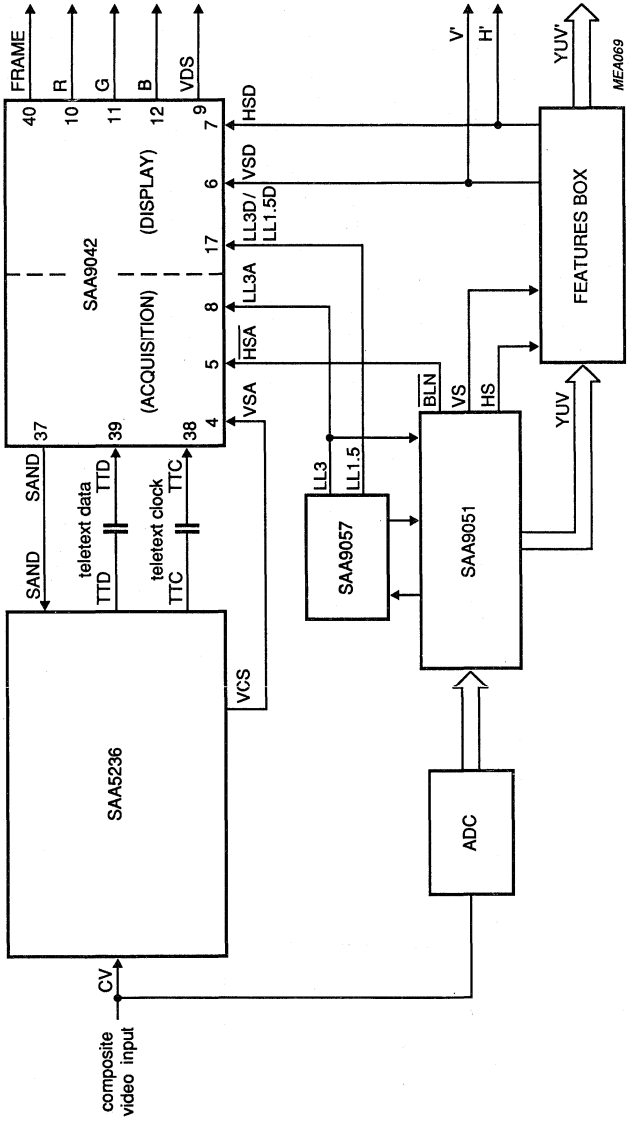


Fig.11 Synchronization of SAA9042 in digital TV with 2 x H features.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	July 1990

SAA9051

Digital multistandard TV decoder with separate chrominance and luminance inputs

FEATURES

- All operations based on a sampling frequency of 13.5 MHz, providing:
  - full adaptability to all transmission standards
  - capability for memory-based features
- Separate chrominance and luminance input (Y/C)
- CVBS input for standard applications
- CVBS throughput capability for SECAM application
- Luminance signal processing for all TV standards (PAL, NTSC, SECAM, B/W)
- Horizontal and vertical synchronization detection for all standards
- Chrominance signal processing for all quadrature amplitude modulated colour-carrier signals
- Requires only one crystal
- Controlled via the I²C-bus
- User-programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filter (NTSC)
- Wide range hue control

GENERAL DESCRIPTION

The SAA9051 digital multistandard decoder (S-DMSD) performs demodulation and decoding of all quadrature modulated colour TV standards, as well as performing luminance and processing for all TV standards with CVBS or Y/C input signals.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9051	68	PLCC	plastic	SOT188

Digital multistandard TV decoder with separate chrominance and luminance inputs

SAA9051

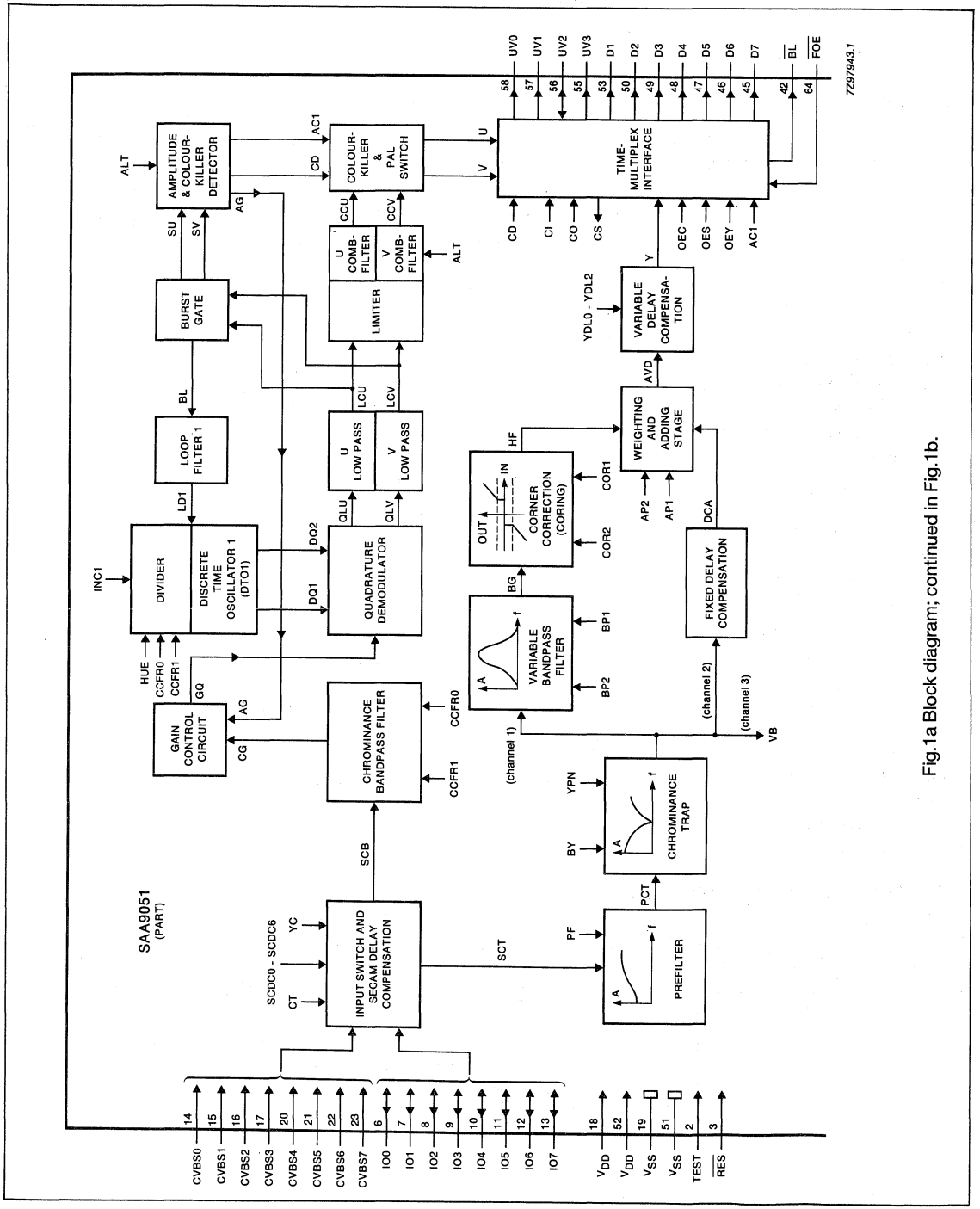


Fig.1a Block diagram; continued in Fig.1b.

Digital multistandard TV decoder with separate chrominance and luminance inputs

SAA9051

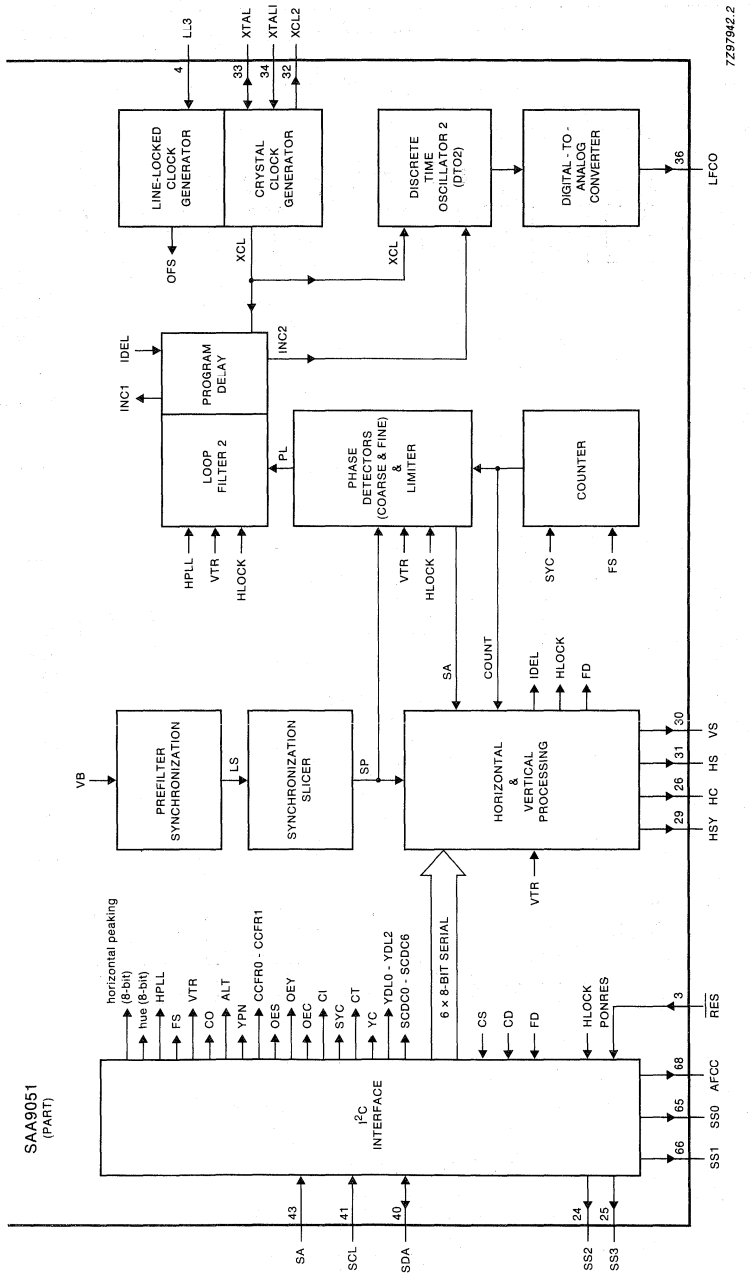


Fig.1b Block diagram; from Fig.1a.

PIN CONFIGURATION

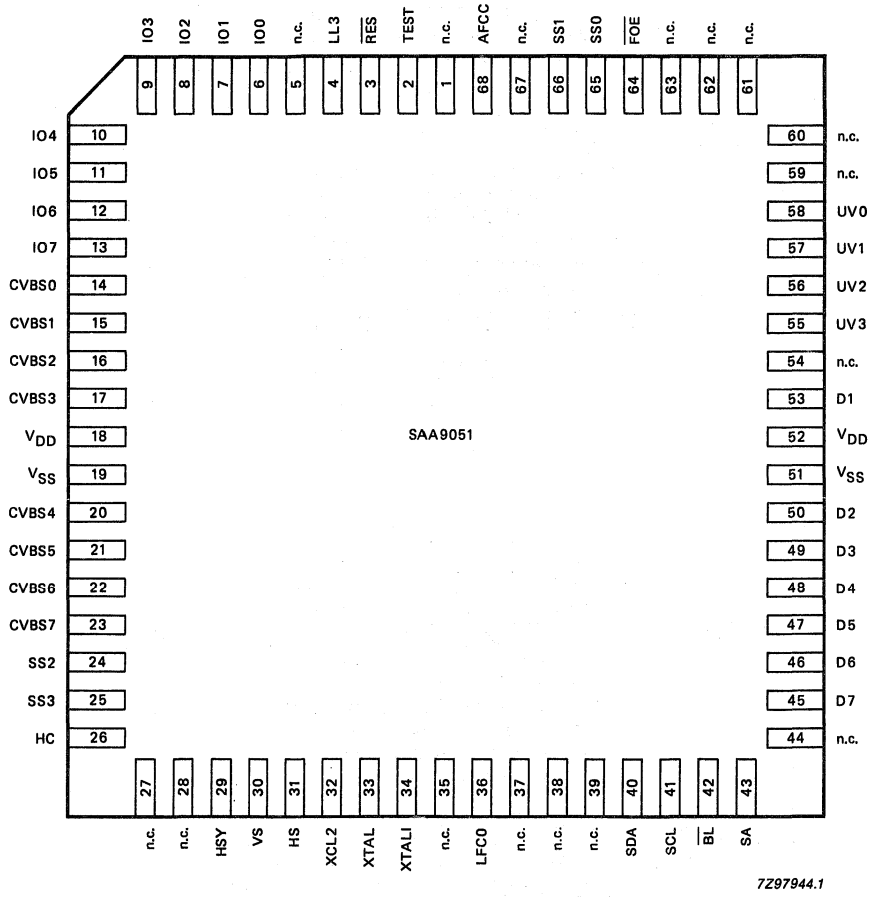


Fig.2 Pinning configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
TEST	2	test input (active HIGH); when HIGH enables scan-test mode
$\overline{RES}$	3	reset input (active LOW); results in the I²C-bus control registers 1 to 3 and internal stages being reset during the reset phase. The minimum LOW period of $\overline{RES}$ is 120 LL3 clock cycles
LL3	4	13.5 MHz line-locked system clock
n.c.	5	not connected
IO0 (LSB) – IO7 (MSB)	6 – 13	bidirectional data path; chrominance input for separate luminance and chrominance input (Y/C) or CVBS output for SECAM decoder SAA9056. Two's complement format (IO0 is only used internally for CVBS throughput)
CVBS0 (LSB) – CVBS7 (MSB)	14 – 17, 20 – 23	digitalized composite video blanking and synchronization signals; containing luminance, chrominance and all synchronization information or luminance, blanking and synchronization signals in the event of separate luminance and chrominance (Y/C) input. Two's complement format (CVBS0 is only used internally for CVBS throughput)
V_{DD}	18	positive supply voltage (+5 V)
V_{SS}	19	ground (0 V)
$\overline{SS2}$ – $\overline{SS3}$	24 – 25	source select output signals; I²C-bus controlled, TTL compatible switches
HC	26	programmable horizontal output pulse; when used in conjunction with the TDA9045 or TDA8708 it indicates the black-level position before analog-to-digital conversion. The start and stop times are programmable, between – 9.4 µs and +9.5 µs in steps of 74 ns, via the I²C-bus
n.c.	27 – 28	not connected
HSY	29	programmable horizontal output pulse; when used in conjunction with the TDA9045 OR TDA8708 it indicates the synchronization pulse position before analog-to-digital conversion. The start and stop times are programmable, between –14.2 µs and +4.7 µs in steps of 74 ns, via the I²C-bus
VS	30	vertical synchronization output; indicates the vertical position of the picture for 50/60 Hz field frequency

PINNING (continued)

SYMBOL	PIN	DESCRIPTION
HS	31	horizontal synchronization pulse output (duration = 64 LL3 clock cycles). HS is programmable, between −32 µs and +32 µs in steps of 300 ns, via the I²C-bus
XCL2	32	clock output; half of the crystal clock frequency (12.288 MHz). In phase with XTAL (pin 33)
XTAL	33	crystal oscillator input/inverting amplifier output; input to the internal clock generator from an external oscillator or output of the inverting amplifier to an external crystal (24.576 MHz)
XTALI	34	input to the inverting amplifier from an external crystal (24.576 MHz); connect to ground if an external oscillator is used
n.c.	35	not connected
LFCO	36	line frequency control; analog output representing a multiple of the line frequency (6.75 MHz) with 4-bit resolution, the phase of which is compared to the system clock by the CGC (SAA9057)
n.c.	37 – 39	not connected
SDA	40	I²C-bus serial data input/output
SCL	41	I²C-bus serial clock input
$\overline{BL}$	42	blanking signal output (active LOW); indicates the active video and line blanking periods. $\overline{BL}$ also synchronizes the data multiplexers/demultiplexers
SA	43	I²C-bus select address; input for selection of the appropriate I²C-bus slave address
D7 (MSB) – D1 (LSB)	45 – 50, 53	luminance data output
V_{SS}	51	ground (0 V)
V_{DD}	52	positive supply voltage (+5 V)
n.c.	54	not connected
UV3 – UV0	55 – 58	multiplexed PAL or NTSC colour difference signal output or SECAM CS input signal from the SECAM decoder. Output data format is two's complement. The multiplexer is synchronized to the rising-edge of $\overline{BL}$
n.c.	59 – 63	not connected
$\overline{FOE}$	64	fast output enable signal (active LOW); sets D1 – D7 and UV0 – UV3 outputs to the HIGH-impedance Z-state

SYMBOL	PIN	DESCRIPTION
SS0 – SS1	65 – 66	source select output signals, set via the I²C-bus; used to control the input switch (e.g. TDA9045)
n.c.	67	not connected
AFCC	68	additional output for circuit control; activated via the I²C-bus

FUNCTIONAL DESCRIPTION

(see Fig.1)

The S-DMSD performs demodulation and decoding for all quadrature modulated colour TV standards (PAL-B, G, H, I, M, N, NTSC 4.43 MHz, NTSC-M), as well as performing luminance and parts of the synchronization processing for TV standards (PAL, NTSC and SECAM). All of the controllable functions, user as well as factory adjustments, are accessed via I²C-bus. Thereby enhancing the adaptability of the digital TV concept.

Operation is based on a line-locked sampling frequency of 13.5 MHz, making the system fully adaptable to all line frequencies and requiring only one crystal for all TV standards.

The S-DMSD is designed to operate in conjunction with the SAA9057A (CGC). If the CGC is not utilized the designer must ensure:

- a reset pulse is applied to the S-DMSD after a power failure
- that a continuous clock signal (minimum 1 MHz) is connected to the S-DMSD.

Y/C processing

In the Y/C mode, the following occurs:

- The chrominance signal is input at the IO port (IO0 – IO7) and transmitted via the input switch/ SECAM delay compensation circuit (multiplexer) to the chrominance bandpass filter (see section chrominance path)
- The other components, Y signal and synchronization pulse, are input via inputs CVBS0 – CVBS7 and transmitted via the input switch/SECAM delay compensation circuit to the luminance prefilter.

CVBS processing

In the CVBS mode:

- The CVBS signal is separated into its luminance (VBS) and chrominance (CG) parts by the chrominance trap and bandpass circuits. These circuits can be switched by the standard identification signals (CCFR0, CCFR1/YPN) according to the detected colour-carrier frequency, 3.58 MHz or 4.43 MHz.
- On reception of a SECAM signal the signal is transmitted to the SECAM decoder (SAA9056) via the IO port (IO0 – IO7). Bit CT enables the 3-state buffer between both parts.

Luminance path

The luminance path is separated into three channels after the chrominance trap stage (see Fig.1). The following occurs:

CHANNEL 1 SIGNAL

The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed (centre frequency is programmable via bits BP1 and BP2). The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed (amount of low amplitude noise removal is programmable via bits COR1 and COR2). The signal HF is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

CHANNEL 2 SIGNAL

The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.

FUNCTIONAL DESCRIPTION (continued)

Luminance path (continued)

CHANNEL 3 SIGNAL

The channel 3 signal VB is transmitted to the prefilter synchronization stage, see section 'Synchronization path'.

COMBINING CHANNEL 1 AND CHANNEL 2 SIGNALS

The channel 1 signal HF is weighted and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7 bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from –4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

Chrominance path

In the chrominance path the following occurs (see Fig.1):

The chrominance signal CG is transmitted from the chrominance bandpass stage to the gain control circuit (see note 1). The gain control stage ensures that the chrominance signal has constant burst amplitude. The signal GQ is transmitted to the quadrature demodulator, where demodulation of the quadrature modulated chrominance signal GQ to colour difference signals occurs. The signals QLU and QLV are transmitted to a low-pass filter for filtering. The signals LCU and LCV are transmitted to the limiter and comb-filter stage. The comb-filter stage (see note 2) separates remaining vertically correlated luminance components for NTSC (for PAL, the signals are phase corrected). The signals CCU and CCV are transmitted to the colour-killer and PAL switch stage (see note 3). At this stage signals which do not comply with the selected standard are removed. In PAL mode this stage restores the correct phase of signal V. The signals are then transmitted to the time multiplexed interface and output via UV0 – UV3.

Notes

1. The gain control stage is controlled by signal AG which is derived form the amplitude and colour-killer detector stage (ACKD). A non-standard burst to amplitude ratio results in an automatic colour-leveling stage functioning as an amplitude detector to ensure correct amplitude and avoid overflow/ limiter defects.

2. The comb-filter can be altered from alternate to non-alternate mode by the ALT signal.

3. The colour-killer and PAL switch stage are controlled by the amplitude and colour-killer detection circuit using signals AC1 and CD.

COLOUR-CARRIER FREQUENCY REGENERATION

The regeneration of the colour-carrier frequency is performed by the phase-locked-loop (PLL) which comprises of a quadrature demodulator, low-pass filter, burst gate, loop filter 1 and divider/discrete time oscillator (DTO1). The DTO1 is controlled by the standard identification signals CCFR0 – CCFR1 and the Hue signal which influences the demodulation phase of the chrominance signal.

Synchronization path

In the synchronization circuit, prefilter synchronization is implemented to normalize the synchronization pulse slopes. A synchronization-slicer provides the detected synchronization pulses (SP) to the horizontal and vertical processing and phase detector stages.

HORIZONTAL AND VERTICAL PROCESSING

The horizontal and vertical processing comprises part of a PLL circuit for regeneration of the horizontal synchronization (HS) and an adaptive filter for detection of the vertical synchronization (VS). The horizontal and vertical processing also generates:

- coincidence signal HLOCK which controls the mute function
- standard identification signal FD which identifies nominal 525 or 625 lines per picture.

PHASE DETECTORS

The phase detectors that receive the SP signal, also part of the PLL, control the generation of the line-locked clock (PL). Loop filter 2, which has a variable bandwidth dependent on the time constant signal VTR, generates two increment signals (INC1 and INC2) with different delays. INC2 is programmable via the increment delay signal IDEL. INC1 corrects the regenerated subcarrier frequency at DTO1 and INC2 performs phase incrementing of DTO2. The crystal clock generator provides a stable 24.576 MHz clock input to DTO2 which in turn supplies the 4-bit DAC with a digital control signal of 432 or 429 times the line frequency. The analog output LFCO from the DAC is transmitted to the SAA9057 (CGC).

Output interface

The signals OES, OEY, OEC, CO, CI and CD control the output interface (see Fig.5). All but one of these signals are received via the I²C-bus, the exception being signal CD which is detected in the S-DMSD. A power-ON reset results in these signals being set to zero.

Table 1 OES signal

OES	OUTPUTS	OUTPUT STATUS
0	HS and VS	inactive (HIGH-impedance Z-state)
1	HS and VS	active

Table 2 CO, CI and CD signals

CO	CI	CD	OUTPUTS	OUTPUT STATUS
0	X	X	UV0 – UV3	colour OFF (zero)
1	0	0	UV0 – UV3	colour OFF (controlled by CD)
1	0	1	UV0 – UV3	colour ON (controlled by CD)
1	1	X	UV0 – UV3	colour forced ON

Where:

X = don't care.

$\overline{\text{FOE}}$ signal

In PIPCO (picture-in-picture controller, SAA9068) applications, the PIPCO requires access to the digital YUV-bus on a pixel time-base. This requirement is catered for by PIPCO generated signal $\overline{\text{FOE}}$, which forces all data output of the S-DMSD and DSD (SAA9056) into the HIGH-impedance Z-state. The $\overline{\text{FOE}}$ signal does not affect the synchronization data lines (HS and VS) or the blanking data line ($\overline{\text{BL}}$), see Fig.6.

FUNCTIONAL DISCRIPTION (continued)

Output interface (continued)

Table 3 OEC, OEY, $\overline{FOE}$, $\overline{BL}$, D1 – D7 and UV0 – UV3 signals

OEC	OEY	$\overline{FOE}$	$\overline{BL}$	D1 – D7	UV0 – UV3	REMARKS
0	0	X	HIZS	HIZS	HIZS	status after power-ON reset
1	1	1	active	HIZS	HIZS	
1	1	0	active	active	active	
0	1	1	active	HIZS	HIZS	
0	1	0	active	active	active	

Where:

X = don't care
HIZS = HIGH-impedance Z-state.

Note to Table 3

1. Combinations other than those shown in Table 3 are not allowed.

CS signal

The CS signal is transmitted from the digital SECAM decoder (DSD) during the H-blanking period and is received via the UV2 input (see Fig.5). The CS bit is read by the S-DMSD once per line at LL3 clock cycle number 748, see Fig.7.

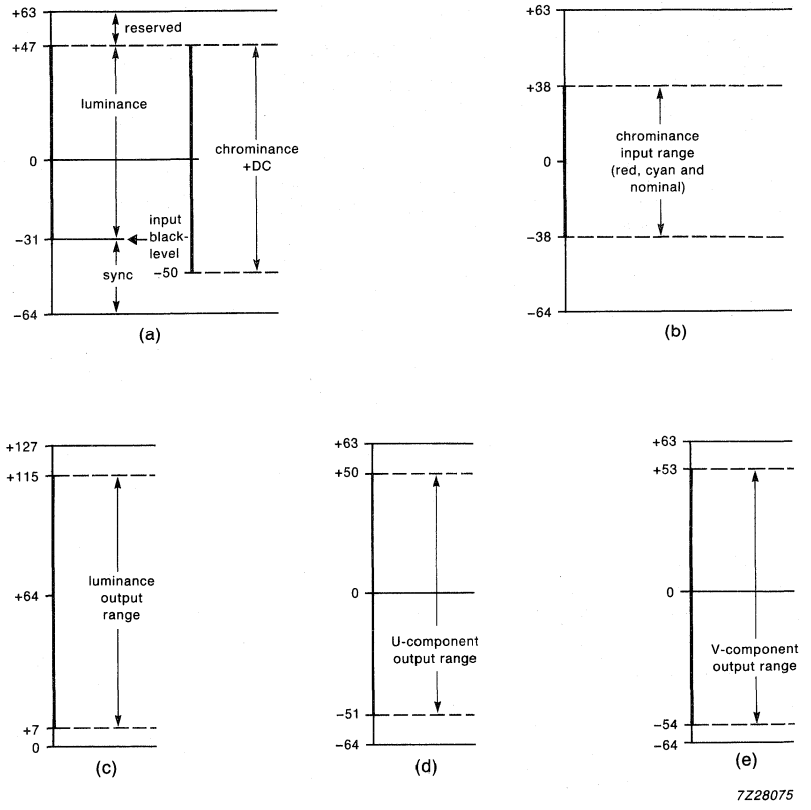
I²C bus interface (see Tables 1 to 3)

The following control signals are received via the I²C bus interface:

- standard identification signals (CCFR0, CCFR1, ALT, FS, YPN)
- video recorder/TV time constant (VTR)
- hue control (HUE)
- delay programming of the horizontal signals (HS, HC, HSY)
- increment-delay (IDEL)
- luminance aperture-correction control (BY, PF, BP2, COR2, COR1, AP2, AP1)
- luminance delay compensation (YDL0, YDL1, YDL2)
- fixed clock generation command (HPLL)
- internal colour ON/OFF (CO)
- internal colour forced ON, test purposes only (CI)
- synchronization output enable (OES)
- luminance output enable (OEY)
- chrominance output enable (OEC)
- switch signals (source select signals SS0, SS1, SS2, SS3)
- additional output for circuit control (AFCC)
- chrominance source select CVBS/ chrominance input/output (CT/ YC).
- SECAM chrominance delay compensation (SCDC0, SCDC21, SCDC2, SCDC3, SCDC4, SCDC5, SCDC6).

Signals transmitted from the S-DMSD via the I²C bus are:

- standard identification signals (FD, CS)
- colour-killer status signal (CD)
- coincidence information (HLOCK)
- power-on-reset of S-DMSD (PONRES).



(a) CVBS1 to CVBS7 input range

(b) IO1 to IO7 input range

(c) Y output range

(d) U output range –(B – Y)

(e) V output range –(R – Y)

Fig.3 Diagram showing input/output range of the S-DMSD; all levels in EBU colour bar, values in binary, 100% luminance and 75% chrominance amplitude.

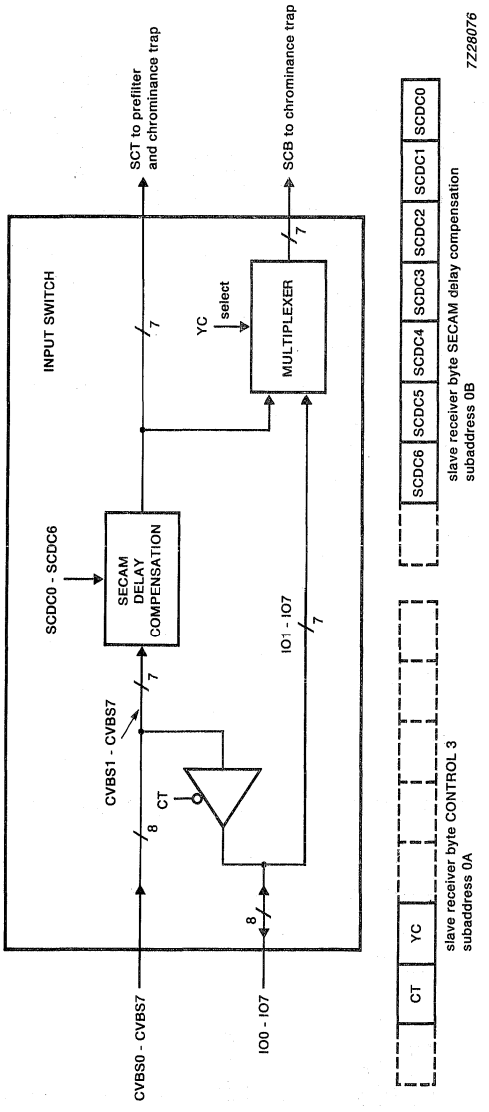


Fig.4 Schematic diagram of the input switch.

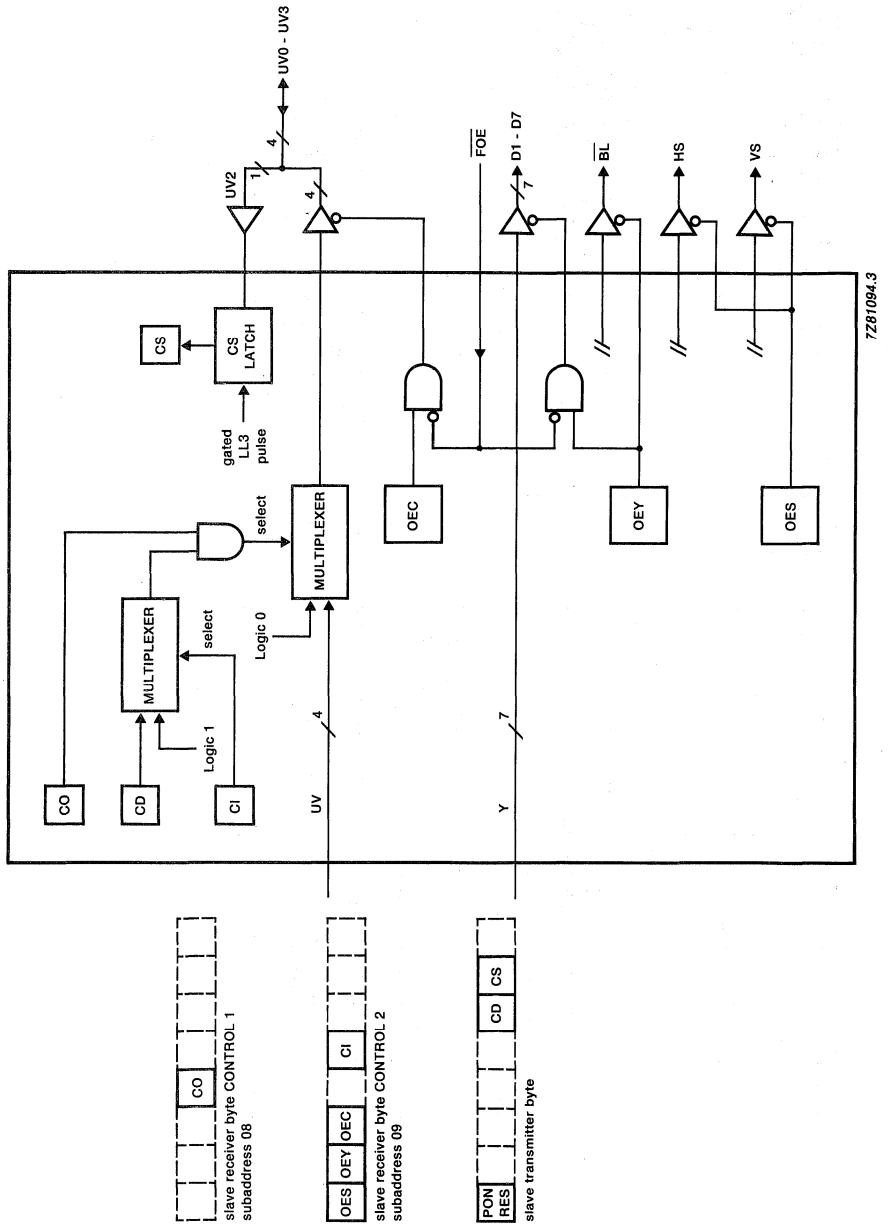


Fig.5 Schematic diagram of control signals at the output interface.

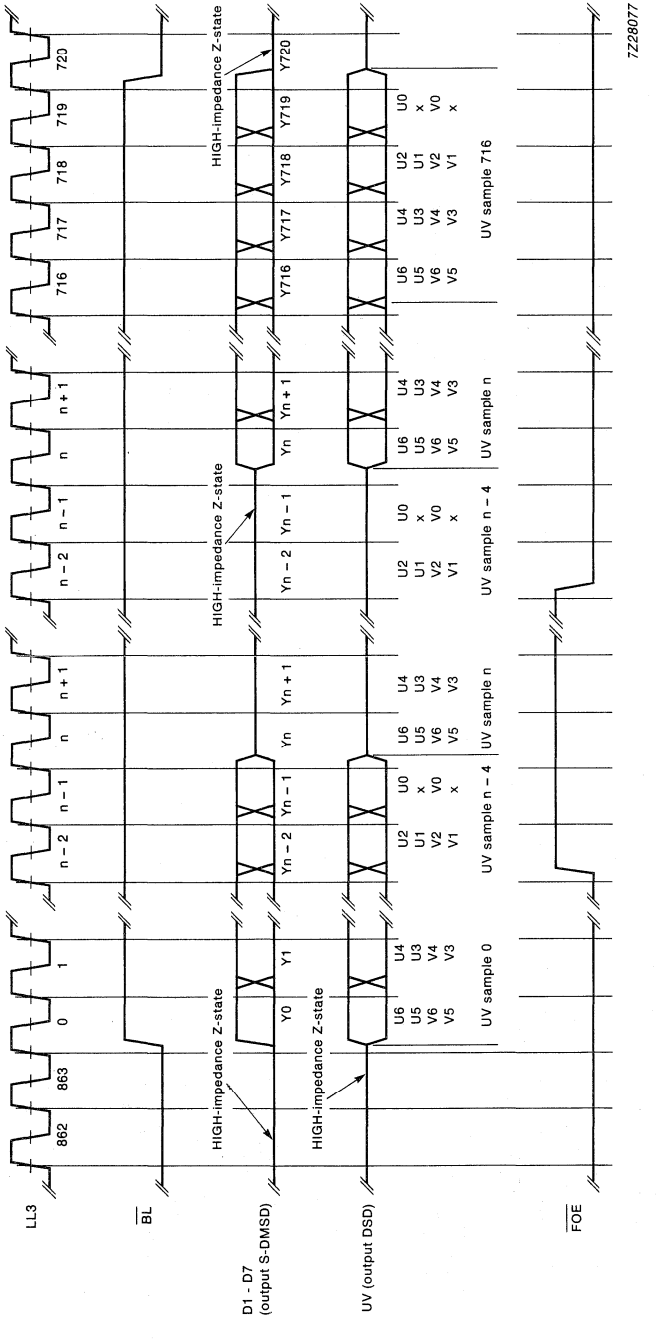
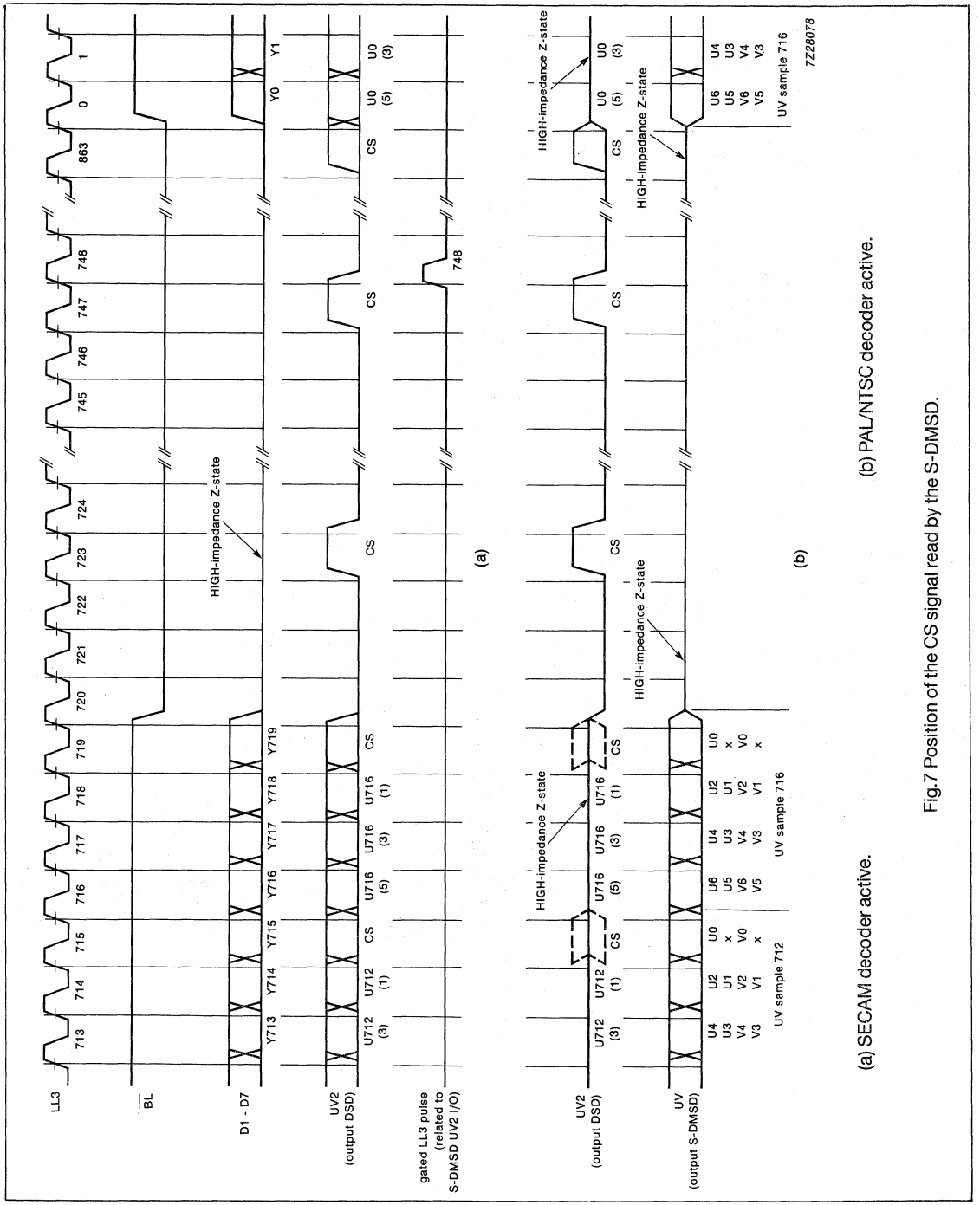


Fig.6 Timing waveform of the output data and $\overline{FOE}$ signals.



(a) SECAM decoder active. (b) PAL/NTSC decoder active.

Fig.7 Position of the CS signal read by the S-DMSD.

SLAVE RECEIVER ORGANIZATION

Slave address and receiver format

There are two slave addresses, programmable via input SA, which determine the operating mode of the S-DMSD, see Table 4.

Table 4 Slave addresses

SLAVE RECEIVER ADDRESS									REMARKS
SA	A6	A5	A4	A3	A2	A1	A0	*	
0	1	0	0	0	1	0	1	0	binary value (8A hex)
1	1	0	0	0	1	1	1	0	binary value (8E hex)

Where:

* = logic 0, receiver mode
* = logic 1, transmitter mode.

Table 5 Subaddress byte and data byte formats

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay IDEL	00	A07	A06	A05	A04	A03	A02	A01	A00
HSY start time	01	A17	A16	A15	A14	A13	A12	A11	A10
HSY stop time	02	A27	A26	A25	A24	A23	A22	A21	A20
HC start time	03	A37	A36	A35	A34	A33	A32	A31	A30
HC stop time	04	A47	A46	A45	A44	A43	A42	A41	A40
HS start time (after PHI1)	05	A57	A56	A55	A54	A53	A52	A51	A50
Horizontal peaking	06	BY	PF	BP2	BP1	COR2	COR1	AP2	AP1
Hue control	07	A77	A76	A75	A74	A73	A72	A71	A70
Control 1	08	HPLL	FS	VTR	CO	ALT	YPN	CCFR1	CCFR0
Control 2	09	OES	OEY	OEC	X	CI	AFCC	SS1	SS0
Control 3	0A	SYC	CT	YC	SS3	SS2	YDL2	YDL1	YDL0
SECAM delay compensation	0B	X	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
Reserved	0C – 0F	X	X	X	X	X	X	X	X

Where:

X = don't care.

Notes to Table 5

The subaddress is automatically incremented. This enables quick initialization, within one transmission, by the I²C-bus controller.

The subaddresses shown are acknowledged by the device. Subaddresses 10 to 1F (reserved for the SECAM decoder SAA9056) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.

After power-on-reset the control registers 1 to 3 (subaddresses 08, 09 and 0A) are, with the exception of bits YDL0 – YDL2 of counter 3, set to logic 0. All other registers are undefined.

The least significant bit of an analog control or alignment register is defined as AX0.

SUBADDRESS 00

Table 6 Increment delay control IDEL (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS*							
		A07	A06	A05	A04	A03	A02	A01	A00
–1 to –110	–148 ns (min. value)	1	1	1	1	1	1	1	1
–1 to –110	–16.3 µs (outside available range)	1	0	0	1	0	0	1	0
–111 to –214	–16.44 µs	1	0	0	1	0	0	0	1
–111 to –214	–31.7 µs (max. value if FS = logic 1)	0	0	1	0	1	0	1	0
–215	–31.85 µs (outside central counter range if FS = logic 1)**		0		0		1		0
–216	–32 µs (max. value if FS = logic 0)**	0	0	1	0	1	0	0	0
–217 to –256	–32.148 µs (outside central counter if FS = logic 0)**		0		0		1		0
–217 to –256	–37.9 µs (outside central counter)**	0	0	0	0	0	0	0	0

Where:

* A sign bit, designated A08 and internally set to HIGH, indicate values are always negative.

** The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ±7.1% of the nominal frequency.

SUBADDRESS 01

Table 7 Horizontal synchronization HSY start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 1/13.5 MHz = 74 ns)	CONTROL BITS							
		A17	A16	A15	A14	A13	A12	A11	A10
+ 191 to + 1	–14.2 µs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	–0.074 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
–1 to –64	+0.074 µs	1	1	1	1	1	1	1	1
–1 to –64	+4.7 µs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 02

Table 8 Horizontal synchronization HSY stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A27	A26	A25	A24	A23	A22	A21	A20
+ 191 to + 1	−14.2 μs (max. negative value)	1	0	1	1	1	1	1	1
+ 191 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −64	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −64	+4.7 μs (max. positive value)	1	1	0	0	0	0	0	0

SUBADDRESS 03

Table 9 Horizontal clamp HC start time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A37	A36	A35	A34	A33	A32	A31	A30
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 04

Table 10 Horizontal clamp HC stop time (application dependent)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/13.5 MHz = 148 ns)	CONTROL BITS							
		A47	A46	A45	A44	A43	A42	A41	A40
+ 127 to + 1	−9.4 μs (max. negative value)	0	1	1	1	1	1	1	1
+ 127 to + 1	−0.074 μs	0	0	0	0	0	0	0	1
0	0 μs reference point	0	0	0	0	0	0	0	0
−1 to −128	+0.074 μs	1	1	1	1	1	1	1	1
−1 to −128	+9.5 μs (max. positive value)	1	0	0	0	0	0	0	0

SUBADDRESS 05

Table 11 Horizontal synchronization HS start time after PHI1 (application dependent); 50 Hz; 625 lines (FS = 0)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 109	Forbidden; outside available central counter range		0		1		1		0
+ 108 to + 1	–32 µs (max. negative value)	0	1	1	0	1	1	0	0
+ 108 to + 1	–0.296 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
–1 to –107	+0.296 µs	1	1	1	1	1	1	1	1
–1 to –107	+31.7 µs (max. pos. value)	1	0	0	1	0	1	0	1
–108 to –128	Forbidden; outside available central counter range		1		0		0		1
–108 to –128	Forbidden; outside available central counter range		1		0		0		0

Table 12 Horizontal synchronization start time after PHI1 (application dependent); 60 Hz; 525 lines (FS = 1)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/13.5 MHz = 296 ns)	CONTROL BITS							
		A57	A56	A55	A54	A53	A52	A51	A50
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		1
+ 127 to + 107	Forbidden; outside available central counter range		0		1		1		0
+ 106 to + 1	–31.8 µs (max. negative value)	0	1	1	0	1	0	1	0
+ 106 to + 1	–0.294 µs	0	0	0	0	0	0	0	1
0	0 µs reference point	0	0	0	0	0	0	0	0
–1 to –107	+0.294 µs	1	1	1	1	1	1	1	1
–1 to –107	+31.5 µs (max. pos. value)	1	0	0	1	0	1	0	1
–108 to –128	Forbidden; outside available central counter range		1		0		0		1
–108 to –128	Forbidden; outside available central counter range		1		0		0		0

Programming IDEL, HSY, HC and HS

The variables IDEL, HSY, HC and HS are programmed using data words via the I²C-bus. In the following examples a decrease in value corresponds to an increase in time.

IDEL (Fig.8)

The IDEL data word compensates for the time delays in data processing between loop filter 2, quadrature demodulator and internal/external (system) signal paths. The internal delay (t_{REF}) is the period required for INC1 to pass from the loop filter 2, through the divider and through DTO1. This delay corrects the relationship between the subcarrier frequency and the line frequency. The external path is a result of the following time delays (time delay is given in term of LL3 clock cycles):

- t_{IDEL}; programmable delay time
- t_a; processing time of DTO2 and the DAC
- t_b; chrominance bandpass and gain control stage delay times
- t_{CGC}; clock generator circuit delay time
- t_{ADC}; analog-to-digital converter delay time
- t_{INP}; input switch delay time.

As delay t_a and t_b are known constants, t_{IDEL} is programmed, range of –115 to –214/216 LL3 clock cycles, as follows:

- $t_{IDEL} = -115 - 0.5$ (* - $t_{CGC} - t_{ADC} - t_{INP}$).

HSY

Referring to Fig.9 point (1) and periods a and b:

- HSY start time = $t_{(1)}$ – a (LL3 clock cycles)
- HSY stop time = $t_{(1)}$ – b (LL3 clock cycles)

Programming range of HSY start/stop time: +191 to –64 (LL3 clock cycles).

HC

Referring to Fig.9 point (1) and periods c and d:

- HC start time = $t_{(1)}$ – c (LL3 clock cycles)
- HC stop time = $t_{(1)}$ – d (LL3 clock cycles)

Programming range of HSY start/stop time: +127 to –128 (LL3 clock cycles).

HS

The HS reference positions in PAL and NTSC modes are shown in Fig.9 at points (3) and (4) respectively. To move the HS pulse to the centre of blanking pulse BL the following equation is used:

- HS (NTSC);

position of HS relative to the zero point (LL3 clock cycles)
4 LL3 clock cycles

- HS (PAL);

position of HS relative to the zero point (LL3 clock cycles)
4 LL3 clock cycles

The length of HS is 64 LL3 clock cycles.

* Value to be fixed.

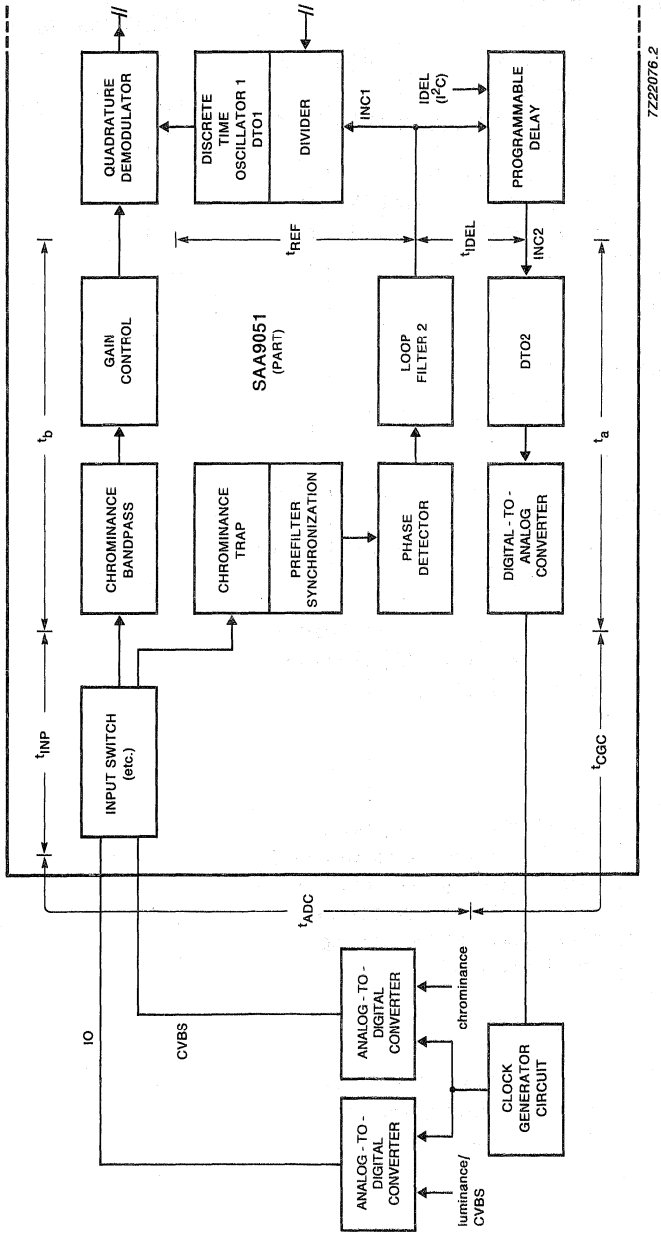
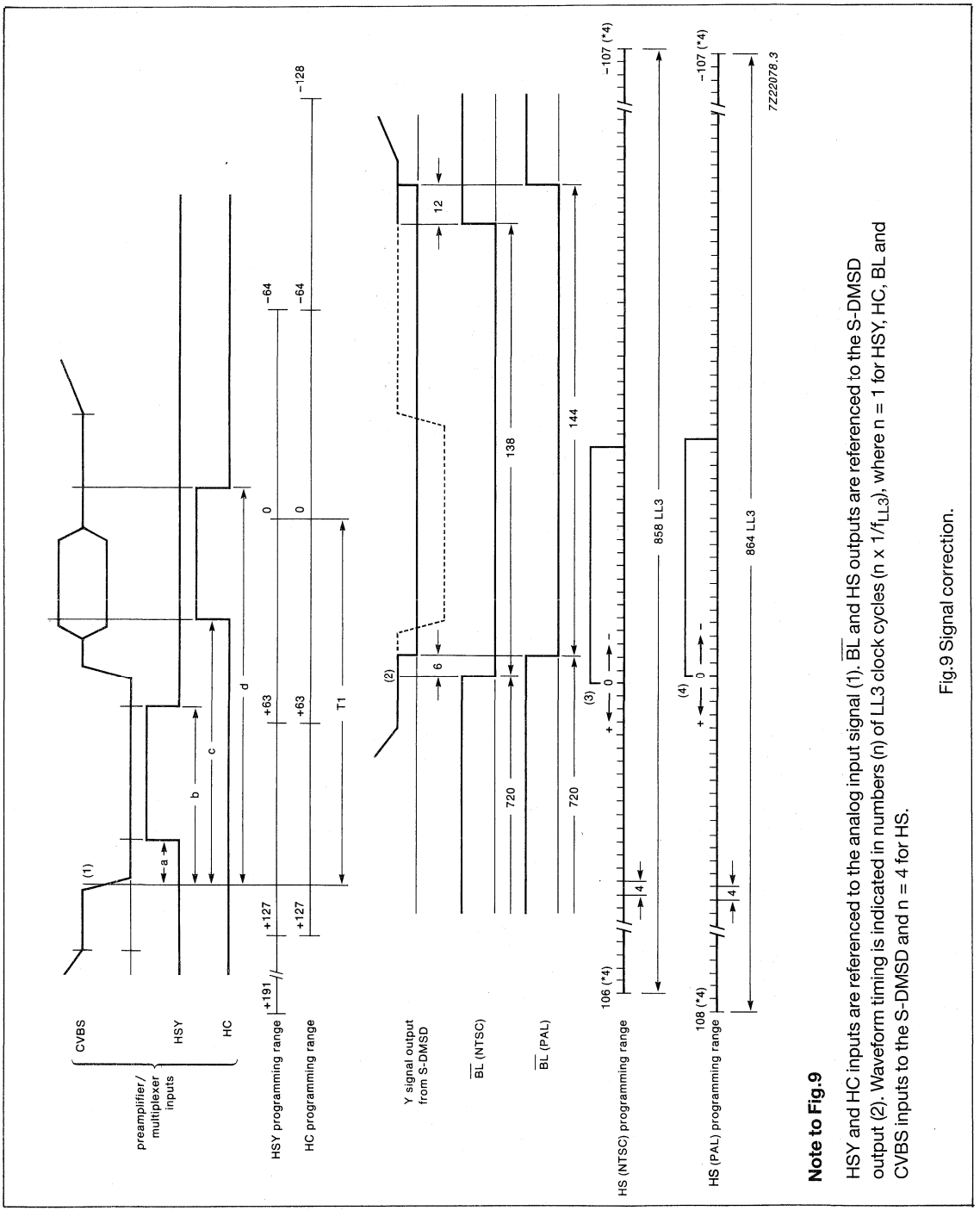


Fig.8 Compensation of delay times by incrementing delay control IDEL.



Note to Fig.9

HSY and HC inputs are referenced to the analog input signal (1). $\overline{BL}$ and HS outputs are referenced to the S-DMSD output (2). Waveform timing is indicated in numbers (n) of LL3 clock cycles (n x $1/f_{LL3}$), where n = 1 for HSY, HC, BL and CVBS inputs to the S-DMSD and n = 4 for HS.

Fig.9 Signal correction.

Programming of the luminance path of the S-DMSD

The VBS (without chrominance) or CVBS input signal enters the prefilter (a high-pass transfer function with maximum amplification of 9.5 dB). The control bit PF switches the filter into the bypass mode. The next stage is the chrominance trap which can be programmed (zero point) to 4.43 MHz (PAL) or 3.58 MHz (NTSC) by the control bit YPN. Bit BY activates the bypass function for the YUV mode of the S-DMSD. The chrominance trap output signal is then divided into three channels:

- Channel 1 signal; The channel 1 signal is transmitted to the programmable bandpass filter where the high luminance frequencies are removed, the centre frequency is programmable via bits BP1 and BP2. The signal BC is transmitted to the coring (corner correction) stage where low amplitude noise is removed, the amount of low amplitude noise removal is programmable via bits COR1 and COR2. The signal HF is transmitted to the weighting stage and adding stage, see 'Combining channel 1 and channel 2 signals'.
- Channel 2 signal; The channel 2 signal is transmitted to the fixed delay compensation stage where delay compensation and black level adjustment occurs. The signal DCA is transmitted to the weighting and adding stage, see section 'Combining channel 1 and channel 2 signals'.
- Combining Channel 1 and Channel 2 signals; The channel 1 signal HF is weighted, programmable via bits AP2 and AP1 and added to the Channel 2 signal DCA. The combined signals are matched to the specified amplitude and the word size is reduced to 7-bits. The signal AVD is transmitted to the variable delay compensation stage where compensation for IF group delays occurs, the amount of delay is programmable (from –4 to +3 LL3 clock cycles, see note) via bits YDL0 – YDL2. The signal Y is transmitted to the time multiplexed interface where the signal is output via D1 – D7.

Note

Differences in the delay compensation required for PAL and NTSC are catered for by identification signal YPN which switches the chrominance trap to the appropriate colour-carrier frequency 3.58 MHz or 4.43 MHz.

- Channel 3 signal; The channel 3 signal VB is transmitted to the pre-filter synchronization stage, see section 'Synchronization path'.

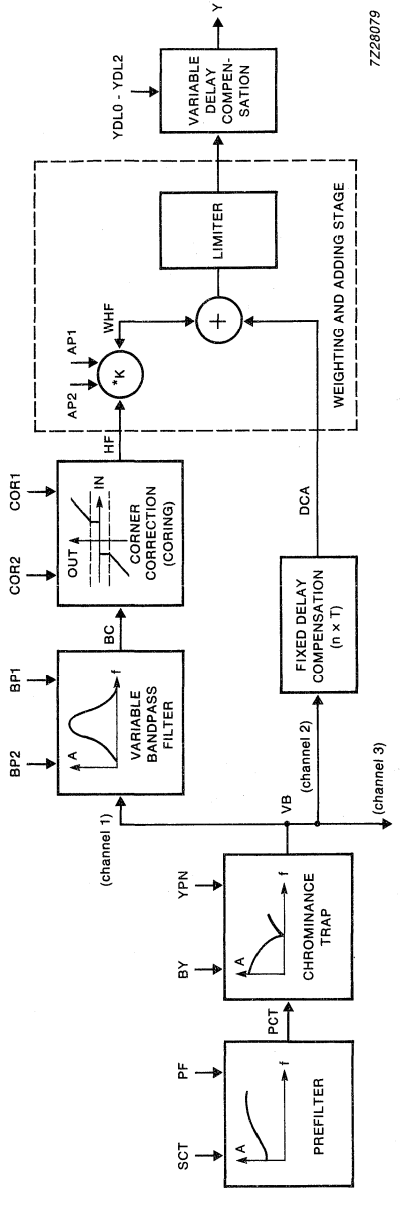


Fig.10 Luminance path of the S-DMSD.

SUBADDRESS 06

Table 13 Chrominance trap select (BY switches the chrominance trap to the bypass mode; YPN selects the notch-frequency)

PREFILTER	CONTROL BITS	
	BY	YPN
PAL (4.43 MHz)	0	0
NTSC (3.58 MHz)	0	1
bypass	1	X

Table 14 Disconnecting the luminance prefilter (user dependent)

PREFILTER	CONTROL BIT PF
ON	0
OFF	1

Table 15 Bandpass control (BP1 and BP2 control the centre frequency of the bandpass filter, see Figs 12 to 15)

BANDPASS TYPE (CENTRE FREQUENCY)	CONTROL BITS	
	BP2	BP1
type 1 (4.1 MHz)	0	0
type 2 (3.8 MHz)	0	1
type 3 (2.6 MHz)	1	0
type 4 (2.9 MHz)	1	1

Table 16 Coring threshold level (COR1 and COR2 control the suppression of low amplitude and high frequency signal components, see Fig.11)

THRESHOLD	CONTROL BITS	
	COR2	COR1
coring off	0	0
coring on (–8 to 7 LSB)	0	1
coring on (–16 to 15 LSB)	1	0
coring on (–32 to 31 LSB)	1	1

Note to Table 16

The thresholds are related the word width of the bandpass filter (12 bits).

Table 17 Aperture correction factor (AP1 and AP2 select the weighting factor K of the high frequency (HF) luminance components, see Fig.10)

WEIGHTING FACTOR K	CONTROL BITS	
	AP2	AP1
0.	0	0
0.25	0	1
0.5	1	0
1.	1	1

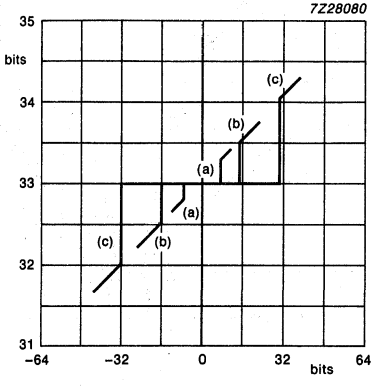


Fig.11 Coring stage response; (a) for COR2 = 0 and COR1 = 1; (b) for COR2 = 1 and COR1 = 0; (c) for COR2 = 1 and COR1 = 1.

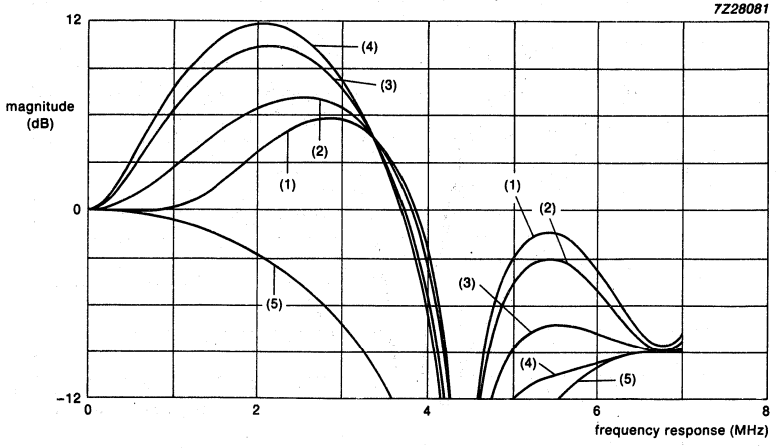


Fig.12 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

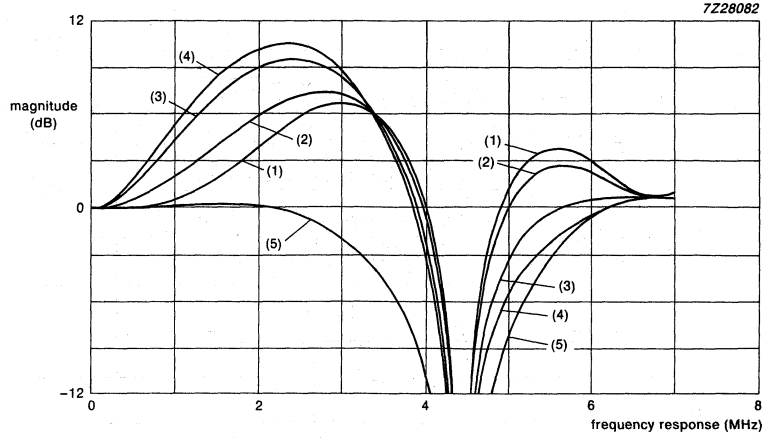


Fig.13 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); PAL mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

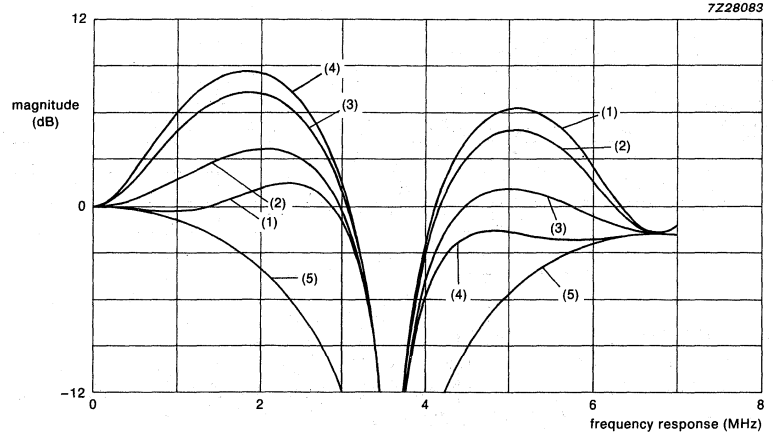


Fig.14 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter OFF; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

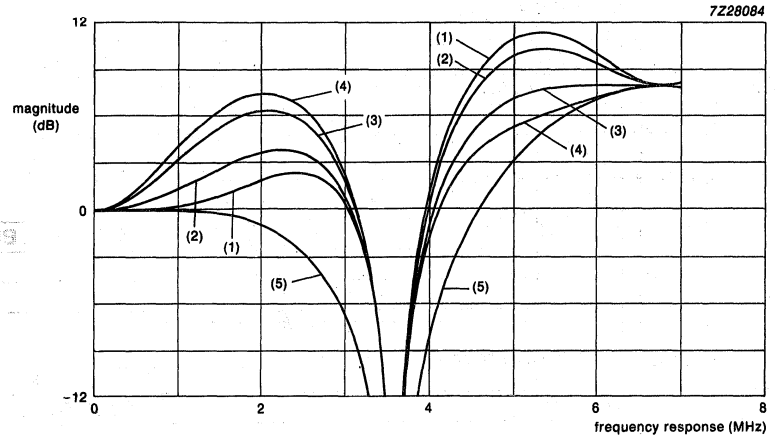


Fig.15 Magnitude of the frequency response of the unlimited summation signal (combining channel 1 and channel 2); NTSC mode; prefilter ON; Responses 1 to 5 show various comb-filter combinations programmable by bits BP2 and BP1, via the I²C-bus.

SUBADDRESS 07

Table 18 Hue phase (user dependent, see notes 1 to 3)

HUE PHASE (deg)	CONTROL BITS							
	A77	A76	A75	A74	A73	A72	A71	A70
+ 178.6 to 0	1	1	1	1	1	1	1	1
0.	1	0	0	0	0	0	0	0
0. to −180	0	0	0	0	0	0	0	0

Notes to Table 18

1. Step size per least significant bit (A70) = 1.4 degree.
2. Reference point for positive colour difference signals = 0 degree.
3. The hue phase may be shifted ±180 degrees from the reference point using bit A77, the colour difference signals are then switched from normally positive to negative polarity.

SUBADDRESS 08

Table 19 Horizontal clock PLL (application dependent)

FUNCTION	HPLL CONTROL BIT
horizontal clock PLL open, horizontal frequency fixed	1
horizontal clock PLL closed	0

Table 20 Field frequency select (system mode dependent)

FUNCTION	CONTROL BIT FS
60 Hz; 525-line mode	1
50 Hz; 625-line mode	0

Table 21 VTR/TV mode select (system mode dependent)

FUNCTION	CONTROL BIT VTR
VTR mode	1
TV mode	0

Table 22 Colour on control (system mode dependent)

FUNCTION	CONTROL BIT CO
colour ON	1
colour OFF (all colour output samples zero)	0

Table 23 Alternate/non–alternate mode (system mode dependent)

FUNCTION	CONTROL BIT ALT
alternate mode (PAL)	1
non-alternate mode (NTSC)	0

Table 24 Chrominance trap select and amplitude matching (system mode dependent)

CHROMINANCE TRAP	CONTROL BIT YPN
3.58 MHz	1
4.43 MHz	0

Table 25 Colour carrier frequency control (system mode dependent)

COLOUR CARRIER FREQUENCY	CONTROL BITS	
	CCFR1	CCFR0
4 433 618.75 Hz (PAL-B, G, H, 1; NTSC 4.43)	0	0
3 575 611.49 Hz (PAL-M)	0	1
3 582 056.25 Hz (PAL-N)	1	0
3 579 545 Hz (NTSC-M)	1	1

SUBADDRESS 09

Table 26 Synchronization output enable (system mode dependent)

FUNCTION	CONTROL BIT OES
outputs HS and VS active	1
outputs HS and VS HIGH-impedance Z-state	0

Table 27 Y-output enable (system mode dependent)

FUNCTION	CONTROL BIT OEY
outputs D0 – D6 and $\overline{BL}$ active	1
outputs D0 – D6 and $\overline{BL}$ HIGH-impedance Z-state	0

Table 28 Chrominance output enable (system mode dependent)

FUNCTION	CONTROL BIT OEC
outputs UV0 – UV3 active; if CD = logic 1, chrominance signal output; if CD = logic 1, zero signal	1
outputs UV0 – UV3 HIGH-impedance Z-state	0

Table 29 Internal colour forced ON/OFF (test purposes only)

FUNCTION	CONTROL BIT CI
colour forced ON, if CO = logic 1 (CD = X) or colour OFF, if CO = logic 0 (CD = X)	1
colour OFF, if CO = logic 0 (CD = X) or colour controlled by CD, if CO = logic 1	0

Where:

X = don't care.

Table 30 Additional output for circuit control

FUNCTION	CONTROL BIT AFCC
output AFCC = HIGH	1
output AFCC = LOW	0

Table 31 Source-select (system mode dependent)

FUNCTION	CONTROL BIT SS0 – SS3
output SS0 – SS3 = HIGH	1
output SS0 – SS3 = LOW	0

Note to Table 31

SS2 and SS3 are part of subaddress 0A.

SUBADDRESS 0A

Table 32 Disabling of HSY and HC pulses (system mode dependent)

FUNCTION	CONTROL BIT SYC
HYS and HC output pulses disabled	1
HSY and HC output pulses enabled	0

Table 33 Chrominance input/output 3-state control

FUNCTION	CONTROL BIT CT
CVBS output active	1
output HIGH-impedance Z-state	0

Table 34 Chrominance source select

FUNCTION	CONTROL BIT YC
Y/C separate inputs	1
CVBS input	0

Table 35 Variable delay compensation of the luminance path (YDL0 – YDL2 control the luminance delay in order to compensate different chrominance delays throughout the system)

DELAY (N =)	CONTROL BITS		
	YDL2	YDL1	YDL0
0	0	0	0
+ 1	0	0	1
+ 2	0	1	0
+ 3	0	1	1
– 4	1	0	0
– 3	1	0	1
– 2	1	1	0
– 1	1	1	1

Note to Table 35

The delay is given in terms of clock cycles:

- 13.5 MHz = N x 74 ns.

SUBADDRESS 0B

Table 36 SECAM chrominance delay compensation (system mode dependent)

PROGRAMMABLE DELAY*	CONTROL BITS						
	SCDC6	SCDC5	SCDC4	SCDC3	SCDC2	SCDC1	SCDC0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
8	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.
16	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.
32	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
63	0	1	1	1	1	1	1
64	1	1	1	0	0	0	0
65	1	1	1	0	0	0	1
.	.	.	.	.	.	.	.
79	1	1	1	1	1	1	1
Maximum delay selected by single control bit							
	16	32	16	8	4	2	1

* Delay in number of LL3 clock cycles.

SLAVE TRANSMITTER ORGANIZATION

Slave transmitter format

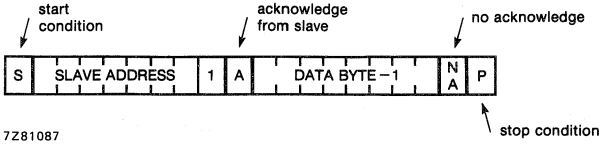


Fig.16 Slave transmitter format (a general call address is not acknowledged).

Note to Fig.16

Data bits D0, D3 and D5 are inverted in slave transmitter byte.

The format of data byte 1 is:

D7	D6	D5	D4	D3	D2	D1	D0
PONRES	HLOCK	1	FD	0	CD	CS	0

Table 37 Description of data byte 1

BIT	DESCRIPTION
PONRES	Status bit for power-on-reset ($\overline{RES}$) and after a power failure. logic 1 after the first power-on-reset and after a power failure. Also set to logic 1 after a severe voltage dip that may have disturbed slave receiver data in the PAL/NTSC decoder (SAA9050). PONRES sets all data bits of control registers 1 and 2 to zero. logic 0 after a successful read of the PAL/NTSC decoder status byte
HLOCK	Status bit for horizontal frequency lock (transmitter identification, stop or mute bit): logic 1 if horizontal frequency is not locked (no transmitter available); logic 0 if horizontal frequency is locked (transmitter received)
FD	Detected field frequency status bit: logic 1 when received signal has 60 Hz synchronization pulses; logic 0 when received signal has 50 Hz synchronization pulses
CD	PAL/NTSC colour-detected status bit: logic 1 when PAL/NTSC colour signal is detected; logic 0 when no PAL/NTSC colour signal is detected
CS	SECAM colour-detected status bit: logic 1 when SECAM colour signal is detected; logic 0 when no SECAM colour signal is detected.

Default coefficients set for the S-DMSD and SAA9056

The default coefficients are set for operation with the TDA8703 or TDA8708, these devices are analog-to-digital converters with built-in sample rate converter. The 3-state outputs of the chrominance ADC are controlled by the SS3 switch in this example (all numbers are hex values).

The slave addresses are as follows:

- S-DMSD; 8A or 8E
- SAA9056; 8A or 8E

Table 38 Slave address (SAA9051 part)

SUBADDRESS	FUNCTION	SHORT DELAY	LONG DELAY
00	inc. delay	5E	7E
01	HSY start	37	73
02	HSY stop	07	43
03	HC start	F6	32
04	HC stop	C7	03
05	HS start	FF	FF
06	H-peaking	02	02
07	HUE control	00	00
08	control 1	38 (77 NTSC)	38 (77 NTSC)
09	control 2	E3	E3 (D3 SECAM)
0A	control 3	58 (28 YUV mode)	58 (28 YUV mode)
0B	SECAM delay	00	3C

Notes to Table 38

1. Subaddress 05; application dependent.
2. Subaddress 08; HPLL is in the VTR mode. Hex value for TV mode is 18 (58 for NTSC).

Table 39 Slave address (SAA9056 part)

SUBADDRESS	FUNCTION	VALUE
10	luminance delay	C0 – FF
11	$\overline{BL}$ delay	00
12	burst gate start	42
13	burst gate stop	56
14	sensitivity	20
15	filter	24
16	control	00 (02 active)

Note to Table 39

Subaddress 16; set to 04 when used in conjunction with SAA9056 and the CS bit is to be transmitted in the horizontal blanking.

Table 40 Operating modes of the S-DMSD

INPUT	CT	YC	SS3	CE	SCDC	IDEL	YPN	BY	FS	ALT	CCFR1	CCFR0	REMARKS
PAL B, G, H, I													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	0	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	0	0	
PAL M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	1	0	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	1	0	1	
PAL N													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	1	1	0	
YUV	0	1	0	0	A	A	0 (1)	1	0	1	1	0	
SECAM													
CVBS	1	0 (1)	1	1	B	B	0	0	0	0 (1)	0 (1)	0 (1)	
YUV	0	1 (0)	0	1	B	B	0 (1)	1	0	0 (1)	0 (1)	0 (1)	
NTSC 4.43 MHz													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	0	0	0	0	0	0	use FS = 1 for 60 Hz vertical frequency
YUV	0	1	0	0	A	A	0 (1)	1	1	0	0	0	use FS = 1 for 60 Hz vertical frequency
NTSC M													
CVBS	1 (0)	0	1 (0)	0	B (A)	B (A)	1	0	1	0	1	1	
YUV	0	1	0	0	A	A	1 (0)	1	1	0	1	1	

Where:

A = short time delay.
B = long time delay.

Notes to Table 40

1. SS3 is assumed to control the 3-state output of the chrominance ADC (active LOW).
2. To avoid data collision care must be taken with the programming of CT and SS3 (in this equal they are always equal).

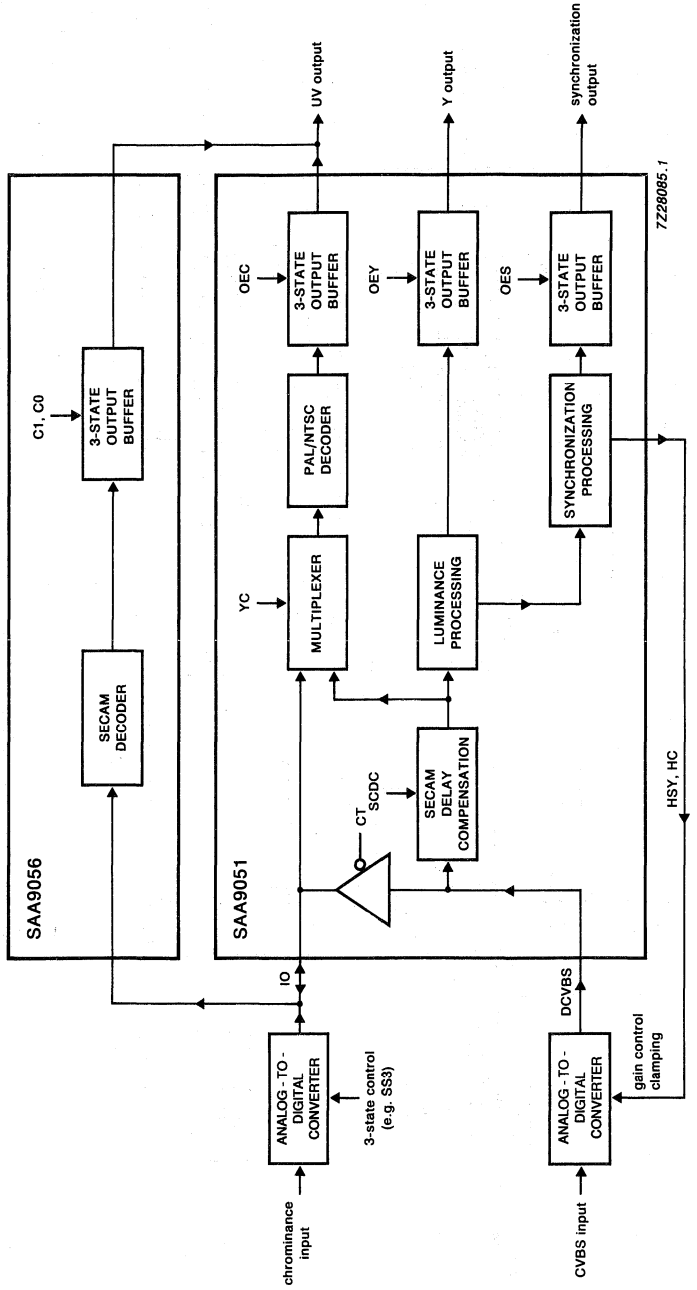
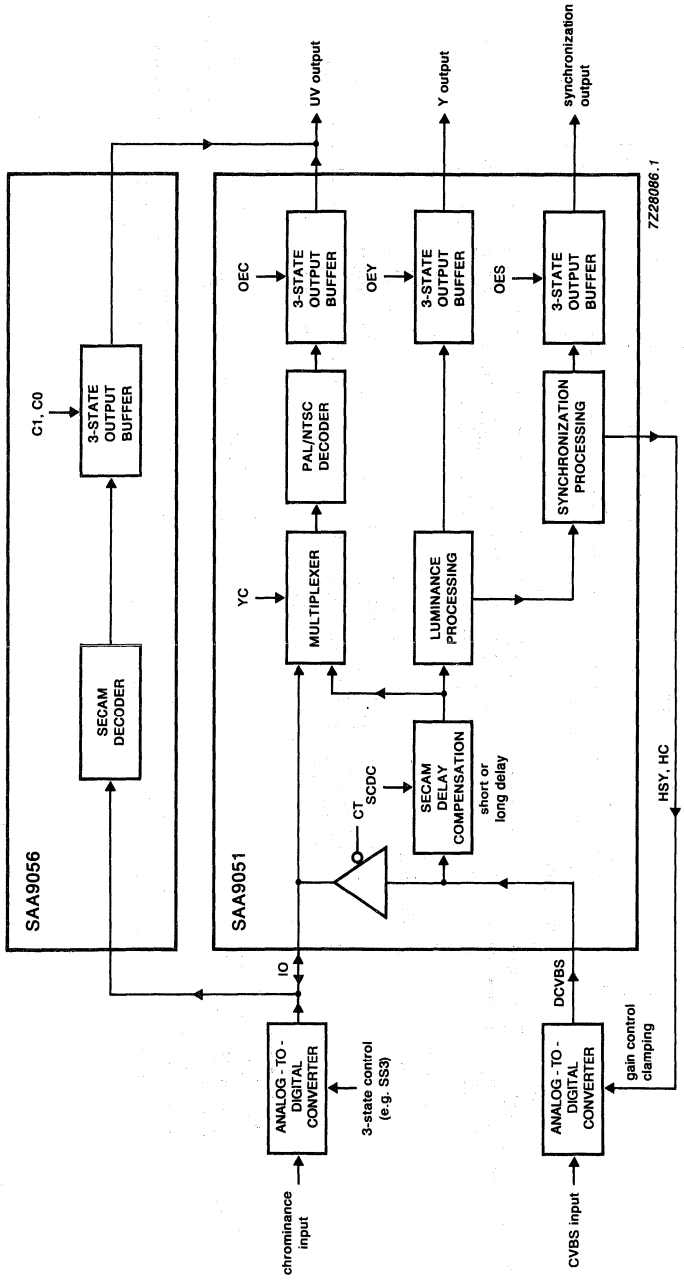
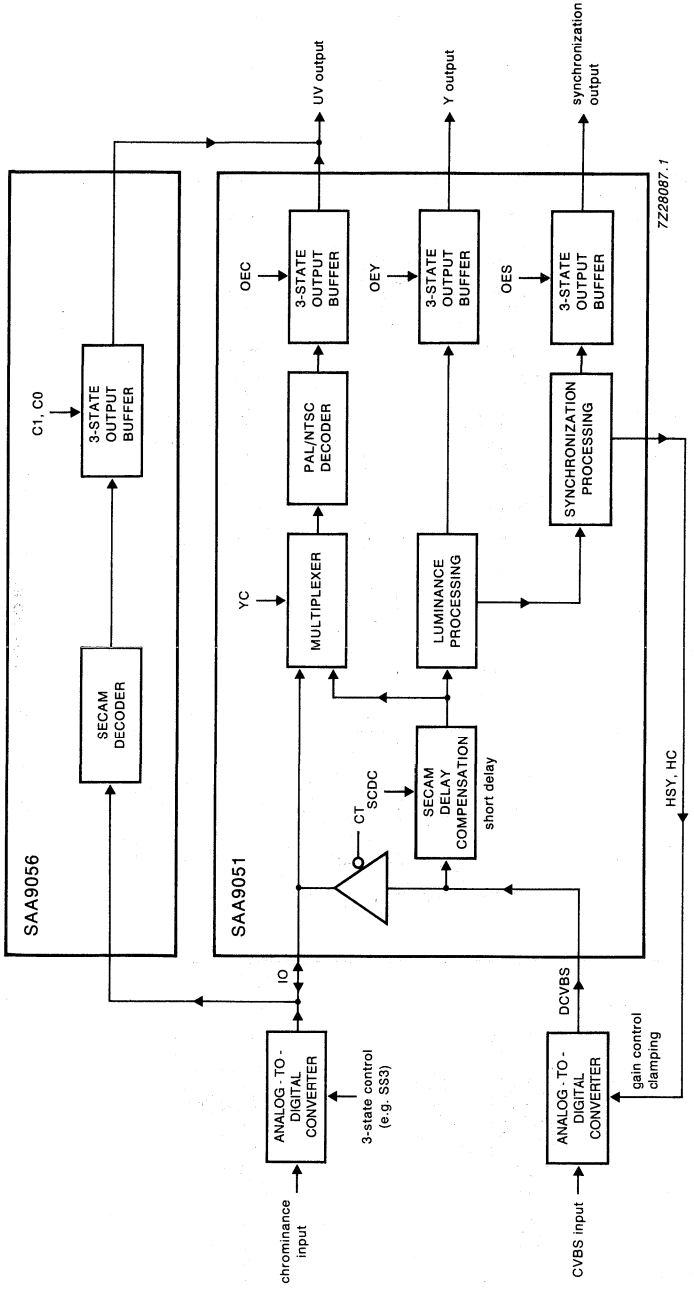


Fig.17 SAA9051 signal flow when used in conjunction with SAA9056.



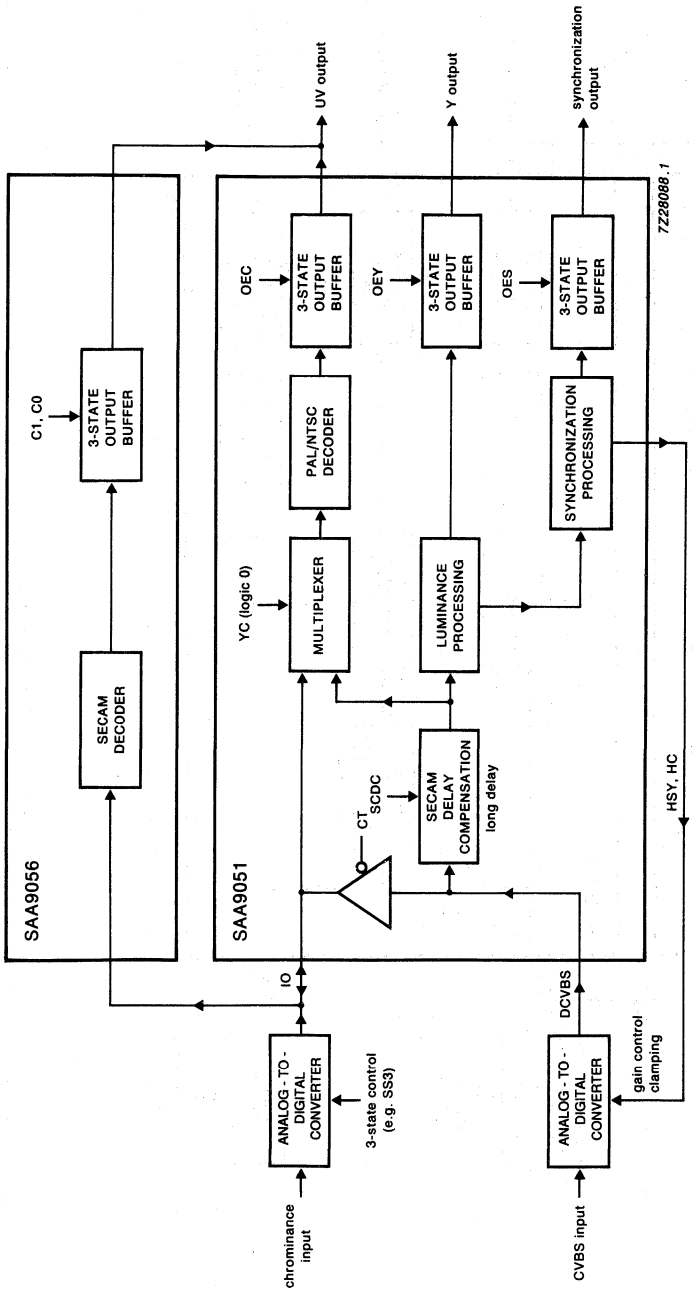
(a) PAL or NTSC with CVBS input signal.

Fig.18 Signal flow in different operating modes.



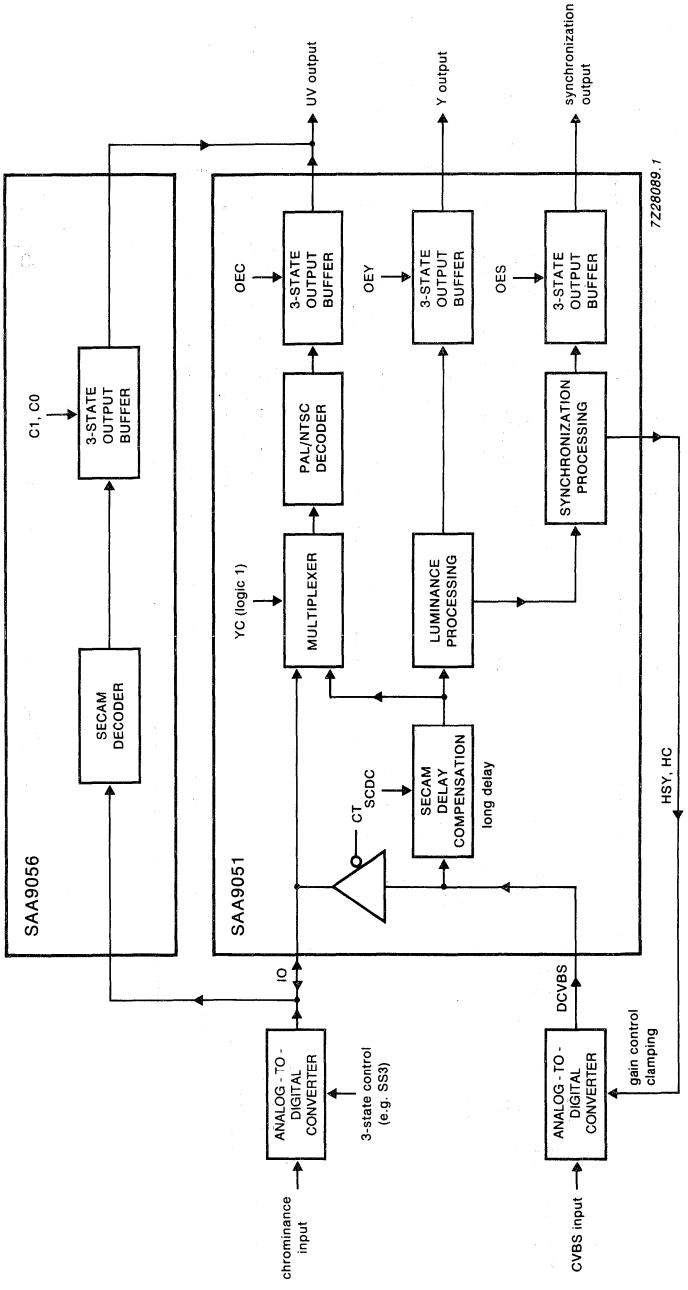
(b) PAL or NTSC with Y/C input signal.

Fig. 18 Signal flow in different operating modes.



(c) SECAM with CVBS input signal.

Fig.18 Signal flow in different operating modes.



(d) SECAM with Y/C input signal.

Fig.18 Signal flow in different operating modes.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage range		−0.5	+ 7.0	V
V_I	Input voltage range		−0.5	+ 7.0	V
V_O	Output voltage range	I_{Omax} = 20 mA	−0.5	+ 7.0	V
P_{tot}	Maximum power dissipation per package		-	3000	mW
T_{amb}	Operating ambient temperature range		0	+ 70	°C
T_{stg}	Storage temperature range		−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V; T_{amb} = 0 to +70 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	note 1	-	380	550	mA
Inputs **Input voltage LOW**						
V_{IL}	pins 2 – 4, 6 – 17, 20 – 23, 43, 56 and 64		–0.5	-	+ 0.8	V
V_{IL}	pins 40 and 41		–0.5	-	+ 1.5	V
Input voltage HIGH						
V_{IH}	pins 2 – 3, 6 – 17, 20 – 23, 43, 56 and 64		2.0	-	V_{DD}	V
V_{IH}	pin 4		2.0	-	V_{DD}	V
V_{IH}	pins 34, 40 and 41		3.0	-	V_{DD}	V
Input leakage current						
I_I	pins 2 – 4, 6 – 17, 20 – 23, 40 – 41, 43 and 64		-	-	10	µA
Input capacitance						
C_I	pin 4		2	-	10	pF
C_I	pins 2 – 3, 14 – 17, 20 – 23, 43 and 64		2	-	7.5	pF
C_I	pins 6 – 13	HIGH-impedance Z-state	2	-	7.5	pF
Outputs **Output voltage LOW**						
V_{OL}	pins 6 – 13, 24 – 26, 29 – 32, 42, 45 -50, 53, 55 – 58, 65 – 66 and 68	I_{OL} = 2.0 mA	0	-	0.6	V
V_{OL}	pin 40 and 41	I_{OL} = 5.0 mA	0	-	0.45	V
Output voltage HIGH						
V_{OH}	pins 6 – 13, 24 – 26, 29 – 33, 42 and 45 – 50, 53, 55 – 58, 65 – 66 and 68	I_{OH} = –0.5 mA	2.2	-	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output capacitance						
C_O	pins 45 – 50, 53 and 55 – 58		-	-	7.5	pF
LFCO output (peak-to-peak value)						
$V_{o(p-p)}$	$R_L \geq 10$ kΩ; $C_L < 15$ pF		1	-	-	V
$V_{o(p-p)}$	$R_L \geq 1$ kΩ; $C_L < 15$ pF		0.5	-	-	V
Timing (see Fig.19)						
t_{C3}	LL3 cycle time		69	-	80	ns
t_{C3H}/t_{C3}	LL3 duty factor		43	-	57	%
t_r, t_f	LL3 rise and fall times	note 3	-	-	6	ns
$t_{SU;\ DAT}$	Input data set-up time		12	-	-	ns
$t_{HD;\ DAT}$	Input data hold time		5	-	-	ns
t_{HD}	Output data hold time		5	-	-	ns
t_D	Output data delay time	except HCY and HS; $C_L = 25$ pF; $I_{OL} =$ 2.0 mA; $V_{OH} = 2.2$ V	-	-	50	ns
t_D	HCY and HS output delay time	$C_L = 25$ pF; $I_{OL} =$ 2.0 mA; $V_{OH} = 2.6$ V	-	-	80	ns
C_L	Output data load capacitance		7.5	-	25	pF
Crystal oscillator (see Fig.20)						
f_n	Nominal frequency	third harmonic	-	24.576	-	MHz
$\Delta f/f_n$	Permissible deviation f_n		-	±50 x 10^{-6}	-	
$\Delta f/f_n$	Temperature deviation from f_n		-	±20 x 10^{-6}	-	
T_{XTAL}	Temperature range		0	-	+ 70	°C
C_{LXTAL}	Load capacitance		8	-	-	pF
R_r	Maximum resonance resistance		-	40	-	Ω
C_1	Motional capacitance		-	1.5 ±20%	-	fF
C_0	Parallel capacitance		-	3.5 ±20%	-	pF

Notes to the characteristics

1. Inputs LOW and outputs not connected, $V_{DD} = 5$ V.
2. 4-bit triangular waveform clocked at 24.576 MHz, AC coupled at pin 36.
3. Rising and falling edges of the clock signal are assumed to be smooth e.g. due to roll-off low-pass filtering.

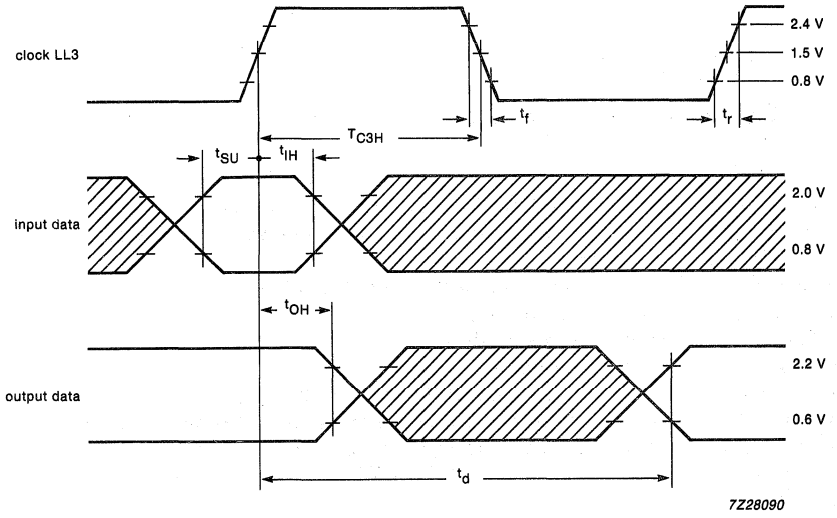


Fig.19 Timing diagram.

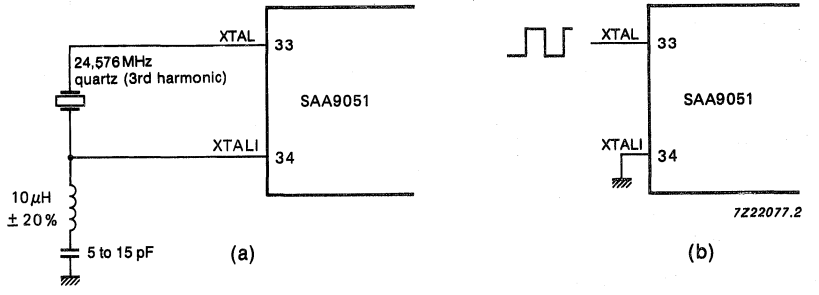


Fig.20 Oscillator circuit requirements; (a) with quartz crystal; (b) with external clock.

S-VHS DIGITAL SECAM DECODER (SDSD)

GENERAL DESCRIPTION

The SAA9056 is designed to provide colour difference signals for a digital TV signal processing system.

Features

- Phase-linear chrominance bandpass filter for cross-colour improvement
- Programmable filter characteristics for optimum adaption for different IF stages
- Recursive "Cloche" (Bell) filter
- Zero-crossing detection, FM demodulator with high AM rejection
- One demodulator for both carrier frequencies
- Base-band signal adjustment in gain and offset
- De-emphasis with recursive filter structure
- Line delay and cross-over switch for colour difference signals
- Output multiplexer for the UV format of the Digital Multistandard Secam Decoder
- Standard identification circuit with programmable sensitivity
- Programmable I^2C-bus address

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

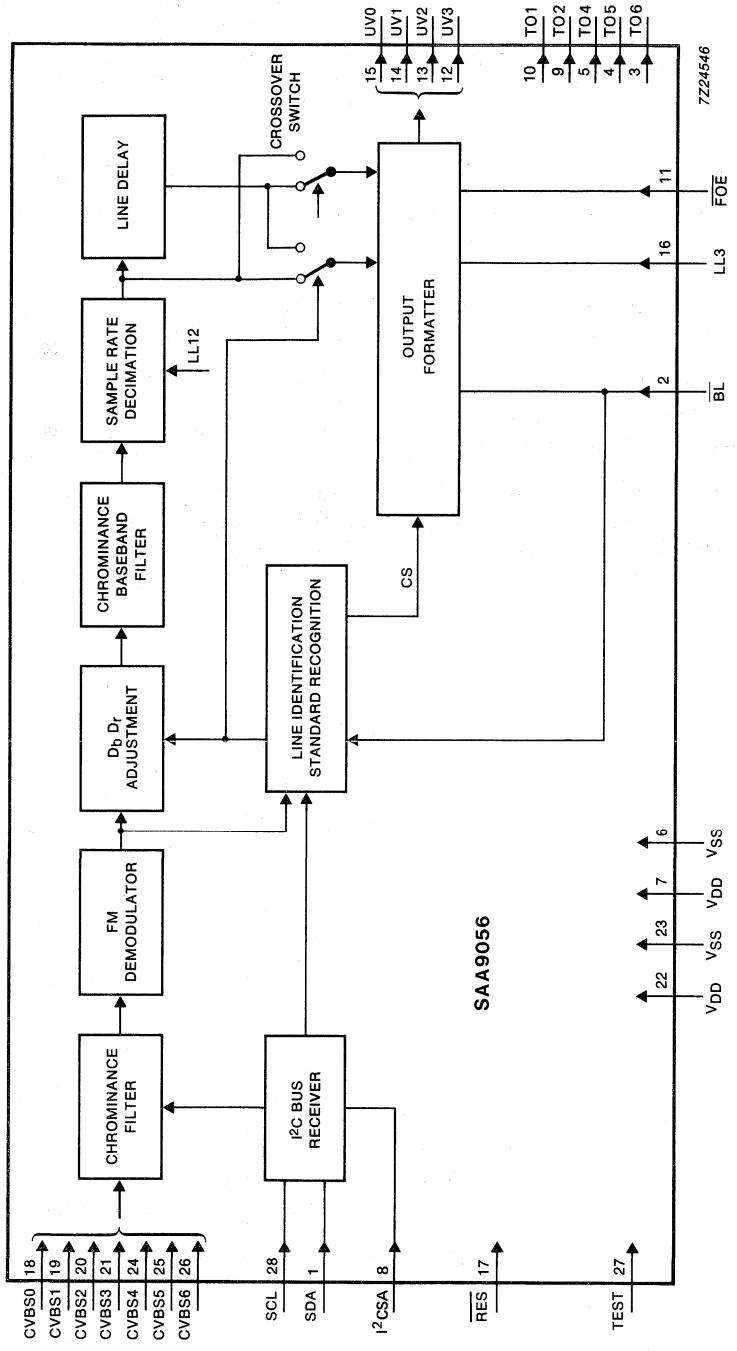


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

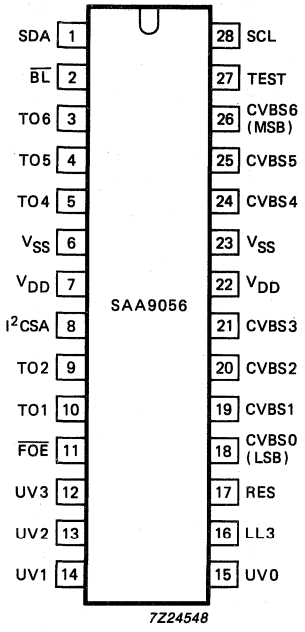


Fig.2 Pinning diagram.

1	SDA	I^2C-bus serial data input, receive only, no data is transmitted from the SDSD
2	$\overline{BL}$	This signal from the digital multistandard decoder indicates the active video and line blanking period
3	TO6	Test output pin, used during test mode only. Do not connect this pin
4	TO5	As pin 3
5	TO4	As pin 3
6	V_{SS}	Ground
7	V_{DD}	+ 5 V supply
8	I^2CSA	I^2C-bus select address. Input to select two different I^2C-bus slave addresses
9	TO2	As pin 3
10	TO1	As pin 3
11	$\overline{FOE}$	Fast output enable signal, forces the UV-outputs to High-Z state
12	UV3	UV colour difference signals, via this port the decoded colour difference signals are transmitted to the DMSD in a mixed parallel/serial format. Additionally the status flag CS (colour in SECAM detected) is encoded in the UV data stream. The output drivers can be set to high impedance (3-state) via the I^2C-bus.
13	UV2	As pin 12
14	UV1	As pin 12
15	UV0	As pin 12
16	LL3	LL3 is the line-locked system clock at 13.5 MHz
17	$\overline{RES}$	The reset signal (active LOW) disables the UV buffers. Minimum LOW-time on this input = 10 LL3-cycles
18	CVBS0	Composite video, blanking and synchronization (LSB) input
19	CVBS1	As pin 18
20	CVBS2	As pin 18
21	CVBS3	As pin 18
22	V_{DD}	As pin 7
23	V_{SS}	As pin 6
24	CVBS4	Composite video, blanking and synchronization
25	CVBS5	As pin 24
26	CVBS6	As pin 24 (MSB)
27	TEST	This signal (active HIGH) enables the scan test mode
28	SCL	I^2C-bus serial clock input

FUNCTIONAL DESCRIPTION

The S-VHS Digital SECAM Decoder (SDSD) forms an integral part of a digital TV signal processing system. The system incorporates a Video Processor and Input Selector (TDA9045), an A/D Converter (SAA9079), a Sample Rate Converter (SAA9058), a Digital Multi-Standard Decoder with separate chrominance and luminance input (SAA9051), a Digital Deflection Controller (SAA9062/3/4)*, a Clock Generator Circuit (SAA9057), a Video Processor with DACs (SAA9060), a Colour Transient Improvement Circuit (TDA4565), a Video Control Combination Circuit (TDA4580), and an Octuple 6-bit DAC and a Feature Box. Figure 9 illustrates the timing of the input and output signals relative to the input clock (LL3).

The S-DMSD (SAA9051) decodes and demodulates the colour information from all TV standards which employ a quadrature modulated colour carrier. The S-DMSD also processes the luminance and synchronization signals and generates auxiliary signals.

The SDSD separates the colour information which it demodulates and decodes to provide the colour difference signals. These signals are subsequently encoded to produce a serial/parallel data stream at the UV outputs. Figure 4 illustrates the formatting and timing of the UV output port.

To enable other sources (eg PIP-CO) to access the digital YUV-bus, a fast output enable signal ($\overline{FOE}$) is provided. Two LL3-cycles after the $\overline{FOE}$ becomes inactive (HIGH), the UV output port of the SDSD is forced to the High-Z state. When the $\overline{FOE}$ signal is active (LOW) again, it needs two LL3-cycles and the UV output port of the SDSD becomes active (see Fig.4).

The chrominance bandpass filter for separating the frequency modulated colour carrier consists of several phase-linear FIR filters which improve the cross-colour behaviour. The non-linear phase (Bell) filter has a recursive structure (IIR filter). Figure 3 illustrates the frequency response of the chrominance band-pass filter and Bell filter. One of the FIR filters can be programmed via the I^2C-bus to provide optimal adaption for the various IF stages. Different responses can be selected by means of a 7-bit control word. Figure 8 illustrates some examples of frequency responses of the programmable adaptive filer.

Only one FM demodulator is used to demodulate the chrominance signal; this accomodates both carrier frequencies regardless of the centre frequency. It is a zero-crossing demodulator with a real time divider which is a pipeline structure. After demodulation the baseband signal is adjusted, line sequentially, to the appropriate colour difference signal. During the clamping period, the demodulated reference carrier is compared with the previous reference signal by the line identification circuit. The identification circuit compares the phase of the two demodulated burst signals and, if the phase relationship is incorrect for several lines (not SECAM), the CS flag (colour in SECAM) will be reset.

The baseband filter consists of a linear phase low-pass filter together with a de-emphasis filter with a recursive structure. Figure 5 illustartes the frequency response of the de-emphasis and band-pass filters for the colour difference signals. After filtering, the sample rate is reduced to a quarter (LL12 = 3.375 MHz). The word length is truncated to seven bits. The resultant signal is delayed by one line period (64 μs = 216 clock periods of 3.375 MHz). The signals, delayed and non-delayed, can be switched either directly or cross-wise to two different outputs which correspond to the colour difference signals.

The cross-over switch is controlled by the line identification circuit. At the end of the chrominance path an output formatter transforms the 14 bits (2 x 7 bits clocked by 3.375 MHz) to a 4-bit wide channel which is clocked by 13.5 MHz (LL3). The bits are separated into odd and even and then serialized.

* The digital TV signal processing system has the option of using one of three Digital Deflection Controllers (SAA9062/3/4). The choice of DDC is dependent on the format of the CRT and the line/field frequency.

The format for the UV output is the same as that of the UV I/O port in the S-DMSD (SAA9051). The timing multiplexer is controlled by the external signal $\overline{BL}$ from the S-DMSD. Signal $\overline{BL}$ is also used as a line-locked synchronization signal to generate several internal burst gate pulses.

The CS flag is transmitted via the chrominance data-stream because the SDSD has no I²C-bus transmitter. The CS bit is read once per line by the S-DMSD at LL3 clock cycle number 748 (see Fig.6). If no SECAM colour is detected the UV port will be set to zero. After reset the UV lines will be set to high impedance (3-state) and the SDSD must be re-initialized via the I²C-bus to enable further operation.

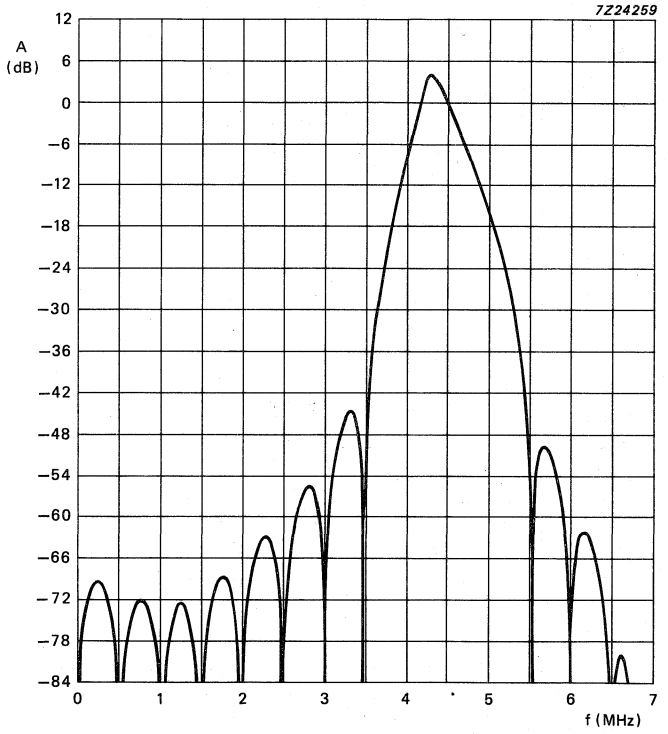


Fig. 3 Frequency response of chrominance bandpass and Bell filter.

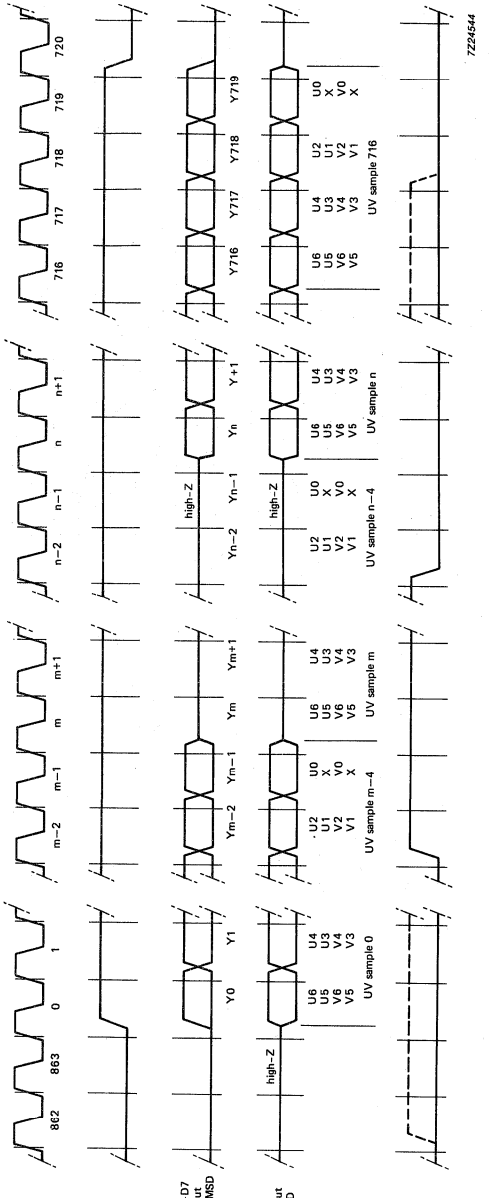


Fig.4 Timing of $\overline{FOE}$ signal.

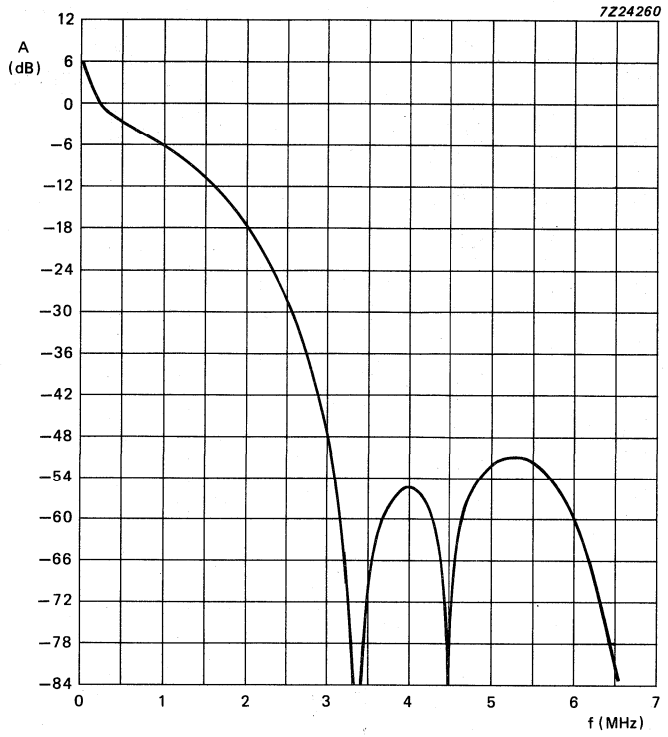
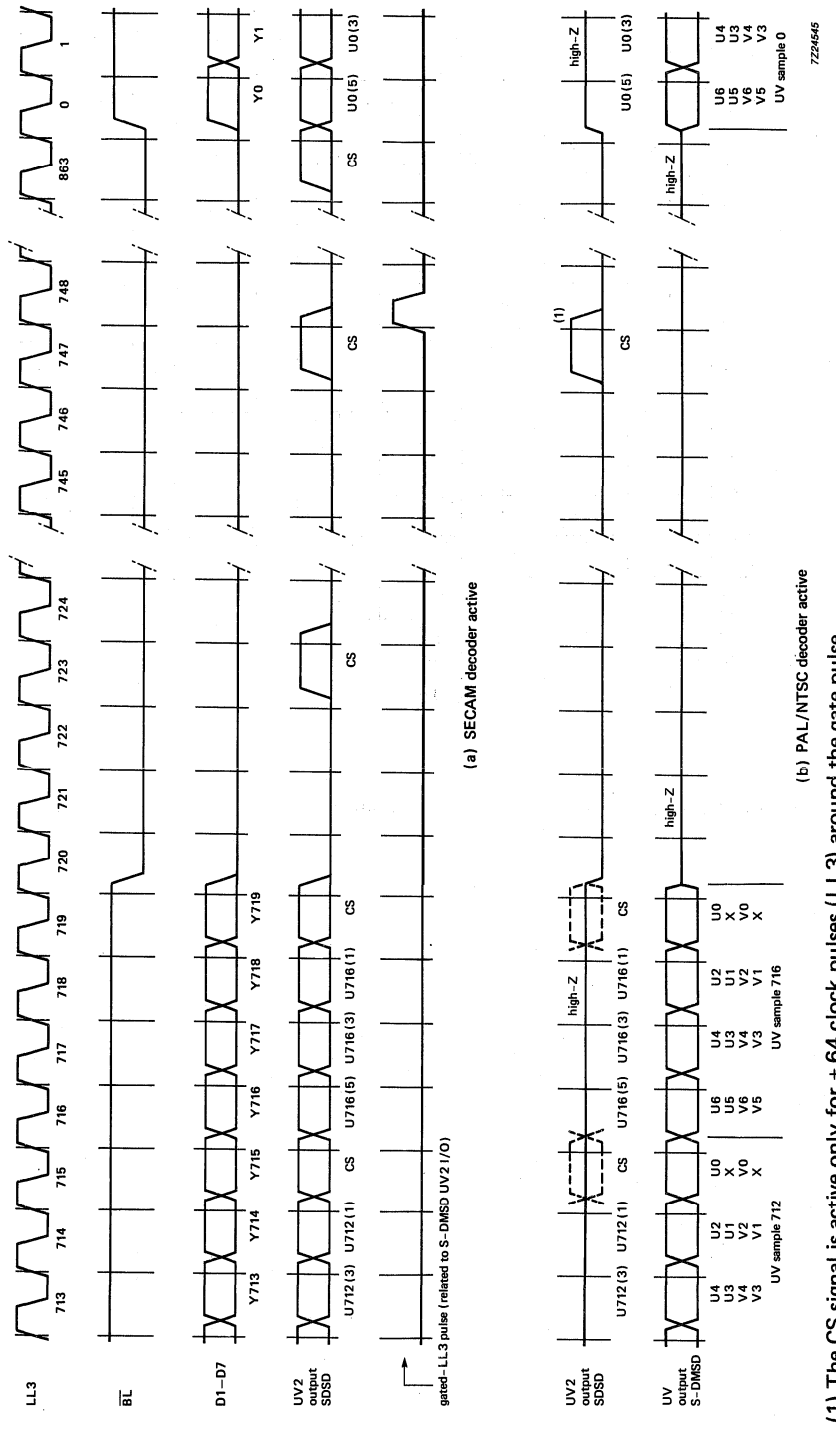


Fig. 5 Frequency response of the de-emphasis and base-band filter for the colour difference signals.

DEVELOPMENT DATA



(1) The CS signal is active only for ± 64 clock pulses (LL3) around the gate pulse.

Fig.6 Position of CS signal read by S-DMSD.

I²C-BUS PROTOCOL

Slave receiver organization

Two different slave addresses are programmable with the I²CSA input at pin 8

I²CSA	slave receiver addresses							
	A6	A5	A4	A3	A2	A1	A0	*)
0 or unconnected	1	0	0	0	1	0	1	0 (bin) = 8A (hex)
1	1	0	0	0	1	1	1	0 (bin) = 8E (hex)

*) 0 = receiver mode

Fig. 7 Slave receiver format.

Table 1 Subaddress definition

register function	subaddress (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Main counter start address (MA9..... MA0)	10	MA1	MA0	X	DT4	DT3	DT2	DT1	DT0
	11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2
Burst gate begin	12	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Burst gate end	13	BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0
Standard recognition sensitivity	14	R7	R6	R5	R4	R3	R2	R1	R0
Programmable adaptive filter	15	X	P6	P5	P4	P3	P2	P1	P0
Control register	16	X	X	X	X	X	C2	C1	C0
Reserved	17–1F	X	X	X	X	X	X	X	X

DEVELOPMENT DATA

Notes to Table 1

1. The subaddress is automatically incremented to enable quick initialization by the I²C-bus controller within one transmission.
2. All eight bits of the subaddress are decoded by the device.
3. The subaddresses shown are acknowledged by the device. Subaddresses 00 to 0F (reserved for the Digital Multi-Standard Decoder) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
4. X = don't care.
5. After power-on-reset the control register (subaddress 16) is set to logic 0, all other registers are undefined.

Subaddress 10 and 11 (HEX)

Main counter start address.

Application dependent.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
0	1	1	1	1	1	1	1	1	1	+511	outside central counter range
–										–	
–										–	
–										–	
–										–	
0	1	1	0	1	0	0	0	1	0	+418	
0	1	1	0	1	0	0	0	0	1	+417	417 x 74 ns ≈ +31 μs (maximum positive value)
–										–	
–										–	
–										–	
0	0	0	0	0	0	0	0	0	1	+1	+74 ns
0	0	0	0	0	0	0	0	0	0	0	reference point*

* Reference point position to be fixed.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
1	1	1	1	1	1	1	1	1	1	–1	–74 ns
–										–	
–										–	
–										–	
1	0	0	1	0	0	0	0	1	0	–446	–446 x 74 ns ≈ –33 μs (maximum negative value)
1	0	0	1	0	0	0	0	0	1	–447	outside central counter range
–										–	
–										–	
–										–	
–										–	
1	0	0	0	0	0	0	0	0	0	–512	

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Internal counter range: –446 to +417

Subaddress 12 (HEX)

Burst gate begin (start time)

Application dependent.

BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	1	1	74 ns
–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Subaddress 13 (HEX)

Burst gate end (stop time)

Application dependent.

BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	0	1	74 ns
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

The stop time must be greater than the start time.

The reference point position of the burst gate start/stop time is identical with the main counter zero position.

DEVELOPMENT DATA

Subaddress 14 (HEX)

Standard recognition sensitivity

Application dependent

R7	R6	R5	R4	R3	R2	R1	R0	function
								relationship between the number of line identification errors related to a window of 312 lines
0	0	0	0	0	0	0	0	0 : 312 theoretical highest sensitivity
0	0	0	0	0	0	0	1	1 : 312
0	0	0	1	1	0	0	1	25 : 312
1	1	1	1	1	1	1	1	255 : 312 theoretical lowest sensitivity

For programmed numbers from 0 to approximately 25 (dec) the colour signal is switched off. With the value 25 (dec) the colour signal will be enabled only when extremely good signal quality is present. If the colour signal quality is reduced, i.e. VCR signal source, bad S/N ratio, bad quantization, diminished colour carrier and insufficient IF adaption, the sensitivity should be set lower (higher programmed number up to 255 (dec) in order to prevent excessive switching and thus ensure constant colour.

DEVELOPMENT DATA

Subaddress 15 (HEX)

Programmable adaptive filter PAF (P6–P0)

Application (IF stage) dependent

The programmable adaptive filter, together with the cloche and linear bandpass filter, forms a filter-curve that treats the chrominance frequency spectra with different gain but linear phase. The frequency characteristic is a system of sinusoidal waveforms which are described by:

- Reference "knots" of constant gain (0 dB)
- Frequency points ("tops") with maximum gain
- The amount of maximum gain
  (There is also a switchable pre-amplifier in another stage of the bandpass filter).

The components of the PAF can be programmed via the I^2C-bus by using device address 8A (or 8E) and subaddress 15 thereby producing 57 different transfer functions. An example of some transfer functions is given in Figure 8 (a) to (d).

MSB	P6	P5	P4	P3	P2	P1	P0	function			
								maximum gain at tops			
–	X	X	X	X	1	1	1	19 dB			
–	X	X	X	X	1	1	0	14 dB			
–	X	X	X	X	1	0	1	9.5 dB			
–	X	X	X	X	1	0	0	6 dB			
–	X	X	X	X	0	1	1	3.5 dB			
–	X	X	X	X	0	1	0	2 dB			
–	X	X	X	X	0	0	1	1 dB			
–	X	X	X	X	0	0	0	0 dB			
								position of tops and knots (MHz)			
								top	knot	top	Figs 8a–d
–	X	1	1	1	X	X	X	3.375	4.5	5.625	+ A/dB (d)
–	X	1	1	0	X	X	X	4.5	5.625	6.75	–A/dB (d)
–	X	1	0	1	X	X	X	4.219	5.063	5.906	–A/dB (c)
–	X	1	0	0	X	X	X	3.375	4.219	5.063	+ A/dB (c)
–	X	0	1	1	X	X	X	4.05	5.4	6.75	–A/dB (b)
–	X	0	1	0	X	X	X	2.7	4.05	5.4	+ A/dB (b)
–	X	0	0	1	X	X	X	2.89	3.86	4.82	+ A/dB (a)
–	X	0	0	0	X	X	X	3.86	4.82	5.79	–A/dB (a)
								additional pre-amplification			
–	1	X	X	X	X	X	X	times two			
–	0	X	X	X	X	X	X	times one			
*	X	X	X	X	X	X	X	* MSB not used			

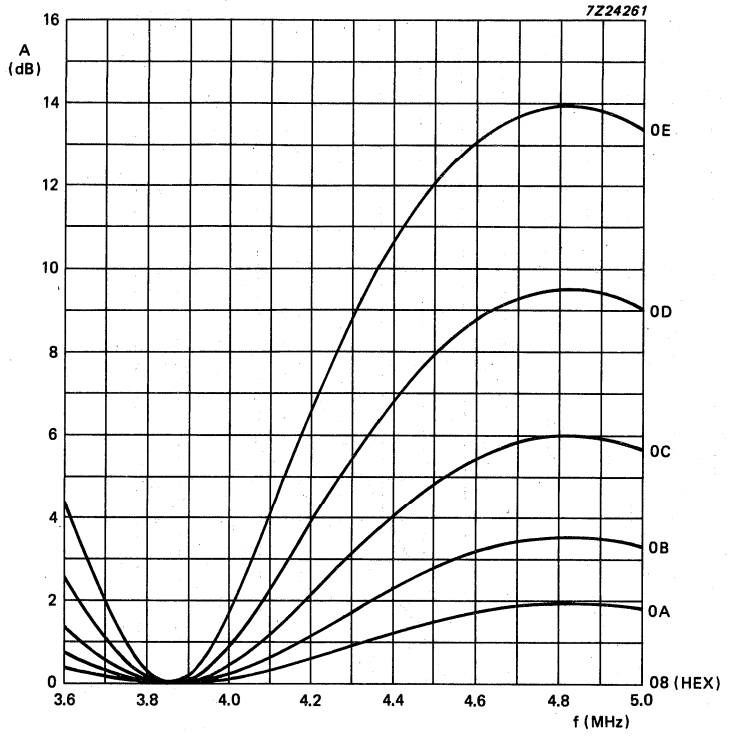


Fig. 8(a) Examples of frequency response for the programmable adaptive filter; from 08 to 0E (HEX).

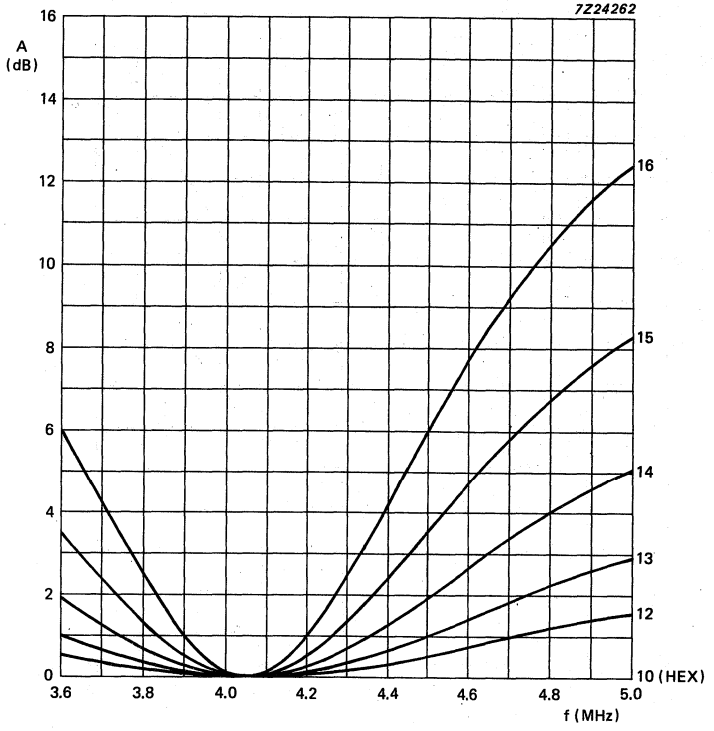


Fig. 8(b) Example of frequency response for the programmable adaptive filter; from 10 to 16 (HEX).

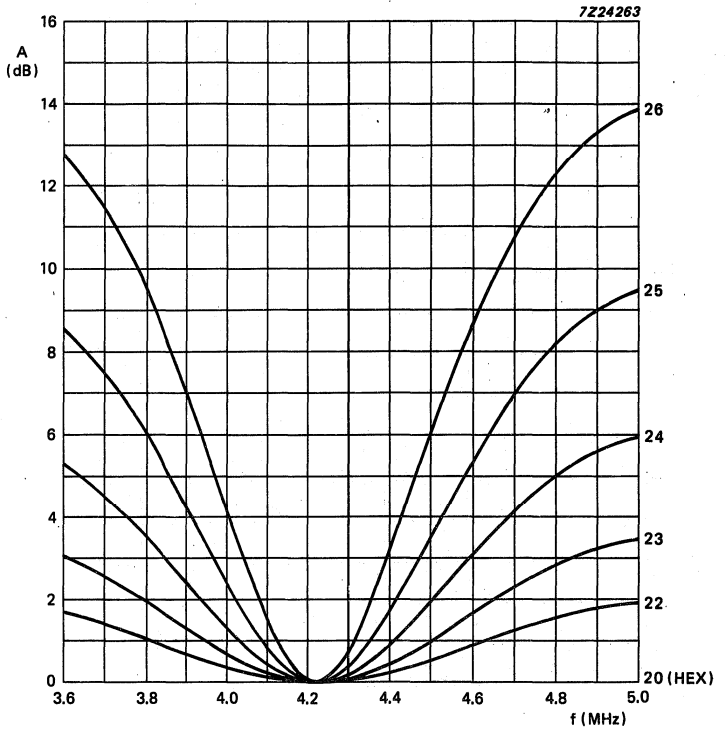


Fig. 8(c) Example of frequency response for the programmable adaptive filter; from 20 to 26 (HEX).

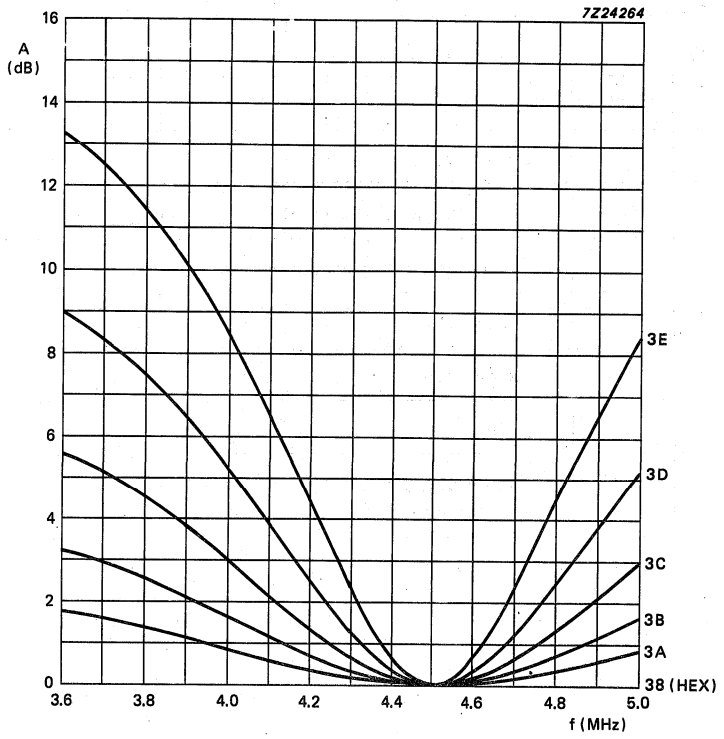


Fig. 8(d) Example of frequency response for the programmable adaptive filter; from 38 to 3E (HEX).

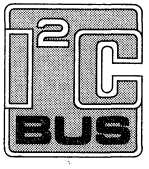
Subaddress 16 (HEX)

DSD control 3 register

C2	C1	C0	UV-output
X	0	1	active zero whole line
X	1	0	colour enable (if CS flag then colour on)
X	1	1	colour forced on (independent of CS flag)
0	X	X	positive UV
1	X	X	negative UV
0	0	0	3-state
1	0	0	UV2-output active during horizontal blanking period (CS-bit* transmission); high impedance in active line negative UV

After power-on reset the control register is set to logic 0.

* The position of the CS transmission is dependent on the start value of the main counter (Reg 10 and 11).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	7.0	V
Voltage input		V_I	−0.5	7.0	V
Voltage output	I_{max} = 20 mA	V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.2	W
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−65	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current (f_{nom})	V_{DD} = 5.5 V					
Inputs LOW; outputs with maximum load		I_{DD}	–	–	180	mA
Inputs						
Input voltage LOW (clock data) pins 2, 16, 17 to 21; and 24 to 27		V_{IL}	0	–	0.8	V
Input voltage LOW (I^2C) pins 1 and 28		V_{IL}	0	–	1.5	V
Input voltage HIGH (data) pins 2, 17 to 21; and 24 to 27		V_{IH}	2	–	V_{DD}	V
Input voltage HIGH (LL3) pin 16		V_{IH}	2.4	–	V_{DD}	V
Input voltage HIGH (I^2C) pins 1 and 28		V_{IH}	3	–	V_{DD}	V
Input leakage current pins 1, 2, 12 to 21; and 24 to 27		I_{LI}	−10	–	+ 10	μA
Input current pins 8 and 11		I_I	−10	–	+ 60	μA
Input capacitance (data) pins 2, 18 to 21; and 24 to 27		C_I	2	–	7.5	pF
Input capacitance (clock) pin 16		C_I	5	–	10	pF
Input capacitance (reset) pin 17		C_I	2	–	10	pF
Outputs						
Output voltage LOW pins 3 to 5; 8 to 15	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW SDA pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH pins 3 to 5; 8 to 15	I_{OL} = −0.5 mA	V_{OH}	2.4	–	V_{DD}	V
Capacitive load of outputs in high impedance pins 12 to 15		C_Z	2	–	15	pF

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Clock timing (LL3)						
Cycle time	note 1	t_{C3}	69	–	80	ns
Duty factor		δ	43	–	57	%
Rise time	note 2	t_r	–	–	6	ns
Fall time	note 2	t_f	–	–	6	ns
Input timing						
Data set up time		t_{SU}	12	–	–	ns
Data hold time	note 3	t_{IH}	5	–	–	ns
Output timing						
Data load capacitance		C_L	7.5	–	50	pF
Data hold time	V_{IH}(CLK) = 3 V	t_{OH}	5	–	–	ns
Data delay time	C_L = 25 pF	t_{OD}	–	–	45	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Static deviation = ±2%; dynamic deviation = ±7% for signal path CVBS-DCVBS (this is required for the running-in of the DMSD sync processor).
2. The rising and falling edges of the clock signal are assumed to be smooth due to roll-off low-pass filtering.
3. Matches to SAA9058 for V_{IH}(LL3) ⩾ 3 V.

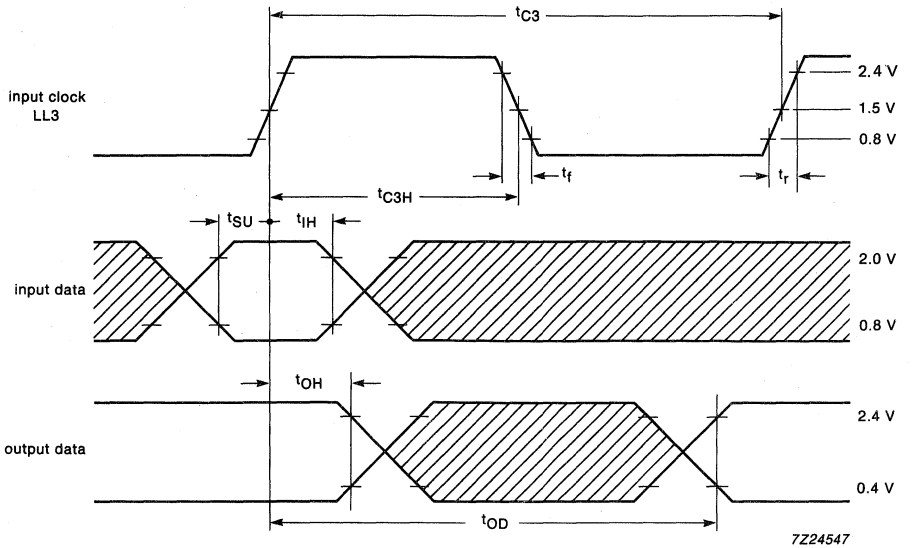


Fig. 9 Timing diagram.

CLOCK SIGNAL GENERATION CIRCUIT (CGC) FOR A DIGITAL TV SYSTEM

GENERAL DESCRIPTION

The SAA9057A is a clock signal generation circuit (CGC) which generates all clock signals required for a digital TV system utilizing the SAA90XX family of devices. The circuit operates in either the phase-locked-loop mode (PLL) or voltage controlled oscillator mode (VCO).

Features

- PLL mode generates clock signals at 2, 3 and 4 times the LFCO frequency (line frequency control)
- PLL frequency multiplier
- Skew control for temperature and load independent phase relationship between the clock signals
- Skew sense inputs
- Power failure detection circuit
- 3-state outputs
- VCO mode (bypassing the PLL)

Applications

- Digital TV system
- Digital TV with feature box and picture memories
- VCO, frequency divider and buffer

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Digital supply voltage		V_{DDD}	4.5	5.0	5.5	V
Analog supply voltage range		V_{DDA}	5.0	–	5.5	V
Digital supply current		I_{DD}	–	–	60	mA
Analog supply current		I_{DDA}	6	–	18	mA
Total power dissipation		P_{tot}	–	–	1.1	W
Operating ambient temperature range		T_{amb}	0	–	+70	°C

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

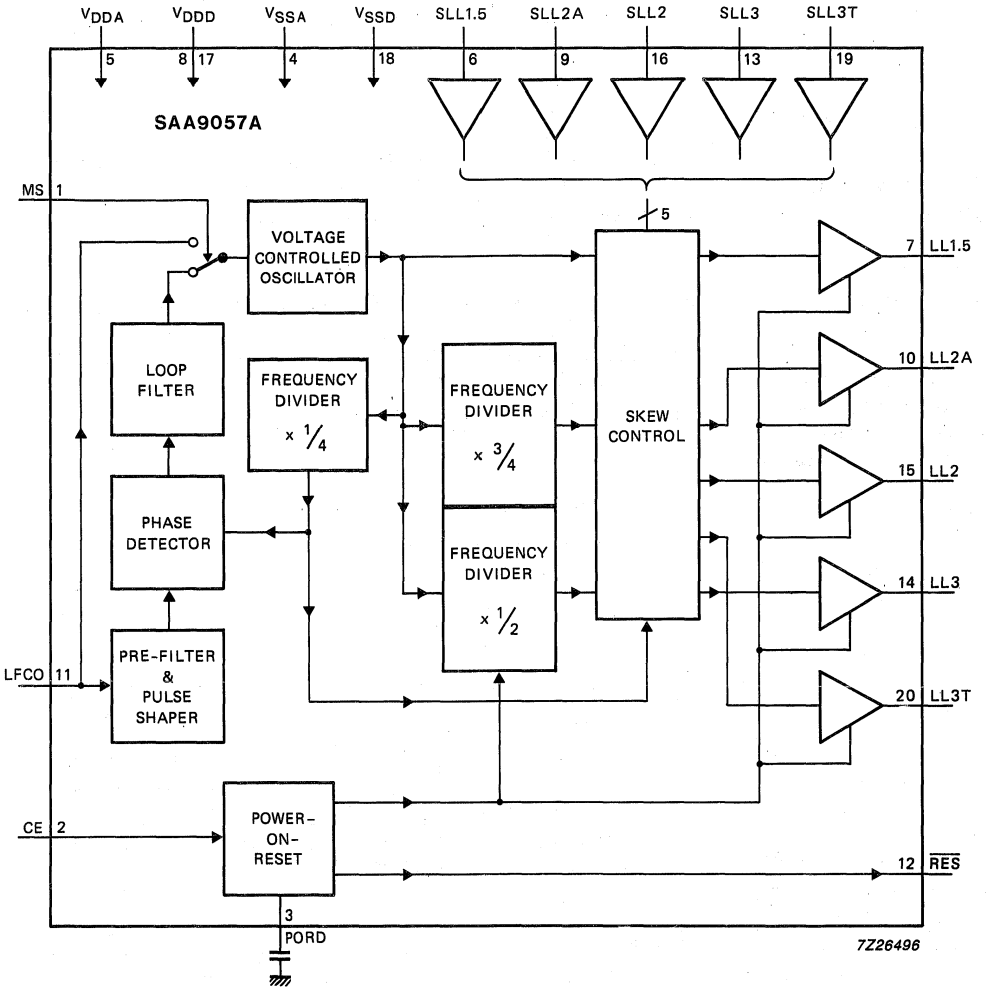


Fig.1 Block diagram.

PINNING

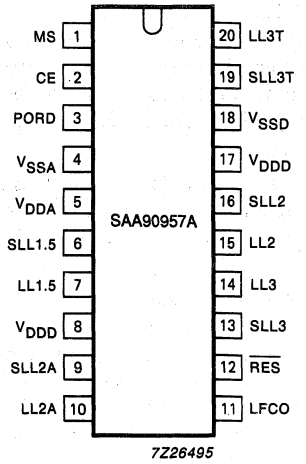


Fig.2 Pinning diagram.

DEVELOPMENT DATA

pin no.	mnemonic	description
1	MS	Mode select input. PLL mode (MS = LOW), the CGC generates clock signals using the LFCO as reference frequency. VCO mode (MS = HIGH), the PLL is disabled and the LFCO is connected to the control input of the VCO. In this mode the device operates as a VCO, frequency divider and buffer.
2	CE	Chip enable input. A HIGH level at CE enables the output buffers. A LOW level disables the buffers (HIGH impedance 3-state). The VCO operates from an internally generated frequency.
3	PORD	Power-ON reset delay. An external capacitor at this pin determines the duration of the reset state.
4	V_{SSA}	Analog ground.
5	V_{DDA}	Analog power supply.
6	SLL1.5	SLL1.5 senses if the LL1.5 output requires skew control. If no external clock driver is utilized, SLL1.5 must be connected to LL1.5. If an external buffer is utilized, SLL1.5 senses the clock signal at the buffer output.
7	LL1.5	LL1.5 is a line-locked clock signal of 4 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor.
8	V_{DDD}	Digital power supply.
9	SLL2A	SLL2A senses if the LL2A output requires skew control. If no external clock driver is utilized, SLL2A must be connected to LL2A. If an external buffer is utilized, SLL2A senses the clock signal at the buffer output.

PINNING (continued)

pin no.	mnemonic	description
10	LL2A	LL2A is a line-locked clock signal of 3 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor. This output is the reference frequency for the internal control loops and should be used as the clock signal for an analog-to-digital converter.
11	LFCO	Line frequency control input. This signal, received from the SAA9050/SAA9051, is a multiple of the line frequency (6.75 MHz). It is the reference frequency for all clock signals generated by the CGC.
12	$\overline{RES}$	RESET output (active LOW). This output indicates the reset state (HIGH or LOW). After a power-ON or power failure $\overline{RES}$ goes LOW and remains in this state for a period that is determined by the external capacitor connected to the pin PORD. If the supply voltage, slowly or rapidly, decreases below the operating range (power failure)*, $\overline{RES}$ goes LOW. After the power supply returns within the operating range and the POR delay is completed, $\overline{RES}$ goes HIGH. This signal can be used to reset the entire digital TV system. When CE is LOW, the $\overline{RES}$ output will be disabled (HIGH impedance state). C_L at $\overline{RES}$ should be < 100 nF.
13	SLL3	SLL3 senses if the LL3 output requires skew control. If no external clock driver is utilized, SLL3 must be connected to LL3. If an external buffer is utilized, SLL3 senses the clock signal at the buffer output.
14	LL3	LL3 is a line-locked clock signal of 2 times the LFCO input frequency. The clock signal is for general use and is rectangular with a 50% duty factor.
15	LL2	LL2 is a line-locked clock signal of 3 times the LFCO input frequency. The clock signal is for general use and is rectangular with a 50% duty factor.
16	SLL2	SLL2 senses if the LL2 output requires skew control. If no external clock driver is utilized, SLL2 must be connected to LL2. If an external buffer is utilized, SLL2 senses the clock signal at the buffer output.
17	V_{DDD}	Digital power supply.
18	V_{SSD}	Digital ground.
19	SLL3T	SLL3T senses if the LL3T output requires skew control. If no external clock driver is utilized, SLL3T must be connected to LL3T. If an external buffer is utilized SLL3T senses the clock signal at the buffer output.
20	LL3T	LL3T is a line-locked clock signal of 2 times the LFCO input frequency. The clock signal is rectangular with a 50% duty factor.

* See section "APPLICATION INFORMATION"; Fig. 4, reset waveform.

FUNCTIONAL DESCRIPTION

The SAA9057A generates all clock signals required for a digital TV system utilizing the SAA90XX family of devices. Optional extras (feature box etc.) can be driven via external buffers, this is advantageous for a digital TV system based on display standard conversion concepts. The frequency of the reference signal LFCO, a 6.75 MHz triangular waveform from the SAA9050/SAA9051, is multiplied by the PLL to 27 MHz (LL1.5). This clock signal is frequency divided to produce LL2 and LL3, using ratios of 3:4 and 1:2 respectively.

To achieve temperature and load independent phase relationship between the clock signals, each output is skew controlled. All clock signals are rectangular waveforms with a 50% duty factor. If no external clock buffers are used, the skew controls are connected to the clock signal outputs.
If external buffers are used, the skew controls check the clock signal at the buffer outputs. The clock signal output lines go HIGH during an internal power-ON reset period, see Fig.4.

The $\overline{\text{RES}}$ output signal indicates the reset state (HIGH or LOW). This output can be used to drive other power-ON reset circuits and provides the SAA9057A with a capability to reset a entire digital TV system. The reset time is determined by the external capacitor connected to pin PORD. It is important that a signal, within the specified ranges, is applied to LFCO before $\overline{\text{RES}}$ goes HIGH.

The SAA9057A will operate as an oscillator and frequency divider, if the phase detector and the loop filter of the PLL are disabled (MS = HIGH) and the control input for the VCO is connected to the pin LFCO.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DDD}/V_{DDA}	−0.5	7.0	V
Input voltage		V_I	−0.5	7.0	V
Output voltage	I_{OM} = 20 mA	V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	−	1.1	W
Storage temperature range		T_{stg}	−65	+150	°C
Operating ambient temperature range		T_{amb}	0	+70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DDA} = 5 V to 5.5 V; V_{DDD} = 4.5 V to 5.5 V; f_{LFCO} = 6.25 MHz to 7.25 MHz;
T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Digital supply voltage range		V_{DDD}	4.5	–	5.5	V
Digital supply current	note 1	I_{DDD}	–	–	60	mA
Analog supply voltage range		V_{DDA}	5.0	–	5.5	V
Analog supply current range		I_{DDA}	6	–	18	mA
Inputs						
Input leakage current	except LFCO	I_{IL}	–	–	10	μA
Input capacitance	except LFCO	C_I	–	–	5	pF
LFCO input capacitance		C_{LFCO}	–	–	10	pF
CE input voltage						
LOW		V_{IL}	0	–	0.8	V
HIGH		V_{IH}	2.4	–	V_{DDA}	V
LFCO input voltage		V_{LFCO}	0	–	V_{DDA}	V
Input signal LFCO amplitude (peak-to-peak value)		$V_{LFCO(p-p)}$	1	–	V_{DDA}	V
LFCO input frequency		f_{LFCO}	6.25	–	7.25	MHz
Outputs						
Output leakage current	note 2; CE = LOW	I_{OL}	−10	–	10	μA
$\overline{RES}$ output voltage HIGH	I_{OH} = −0.5 mA	V_{OH}	2.4	–	V_{DDD}	V
$\overline{RES}$ output voltage LOW	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
$\overline{RES}$ delay time	note 3; see Fig.4	t_d	20	–	200	ms

Notes to the characteristics

1. With 40 pF load at all outputs.
2. All outputs in 3-state.
3. Measured with a 100 nF capacitor at pin 3.

TIMING CHARACTERISTICS (see Fig.3)

T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
LL1.5, LL2, LL2A, LL3, LL3T						
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	0	–	0.6	V
Output voltage HIGH	I_{OH} = –0.5 mA	V_{OH}	2.6	–	V_{DDD}	V
Output frequency						
LL1.5		$f_{LL1.5}$	–	–	$4f_{LFCO}$	MHz
LL2		f_{LL2}	–	–	$3f_{LFCO}$	MHz
LL2A		f_{LL2A}	–	–	$3f_{LFCO}$	MHz
LL3		f_{LL3}	–	–	$2f_{LFCO}$	MHz
LL3T		f_{LL3T}	–	–	$2f_{LFCO}$	MHz
Composite rise time	notes 1 and 2	t_{comp}	–	–	9	ns
Duty factor	note 1					
LL1.5			40	–	60	%
LL2			40	–	60	%
LL2A			43	–	57	%
LL3			43	–	57	%
LL3T			43	–	57	%

Notes to the timing characteristics

1. f_{LFCO} = 7.0 MHz, with a 40 pF output load (typically 6.75 MHz).
2. The composite rise time is the time duration from all clocks = LOW to all clocks = HIGH (within 0.6 V to 2.6 V, includes rise time, skew and jitter).

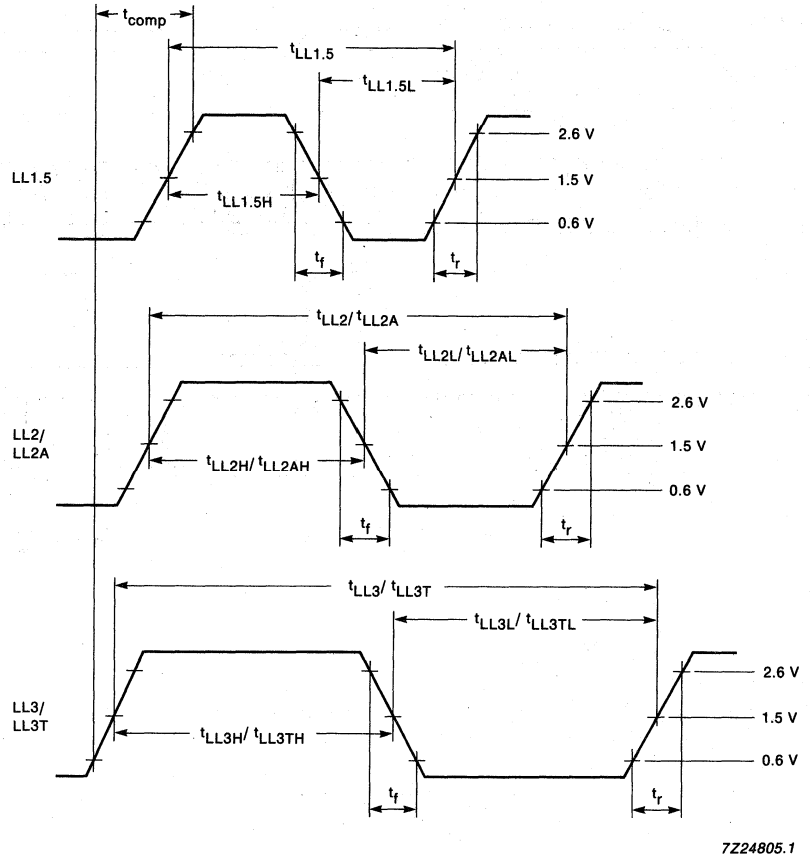


Fig.3 Timing waveform.

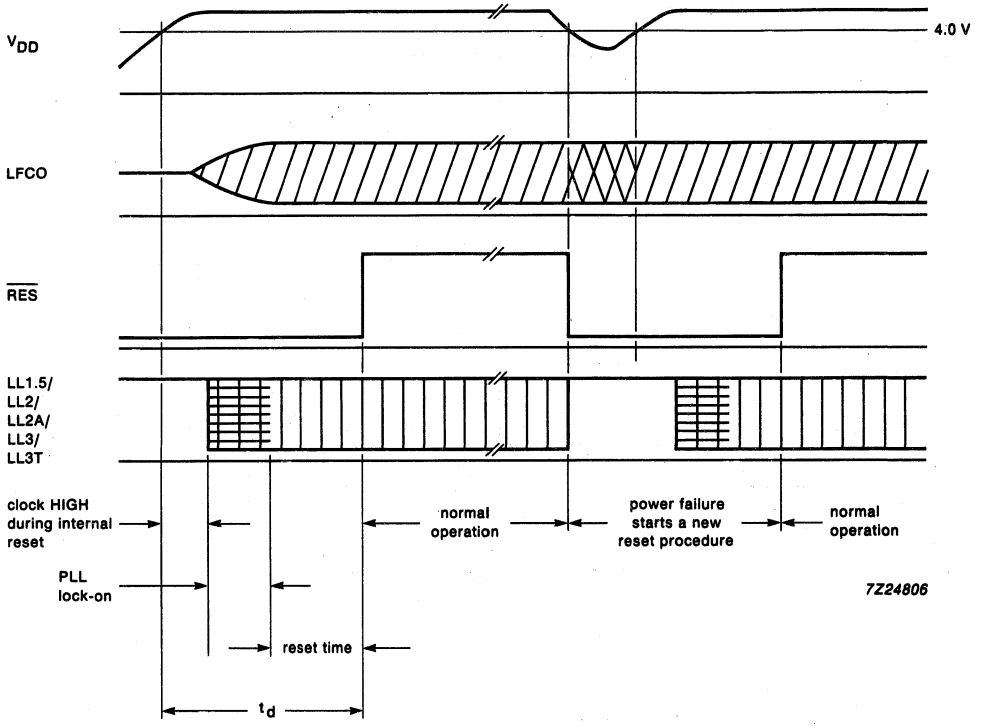


Fig.4 Reset waveform.

INTERNAL PIN CONFIGURATIONS

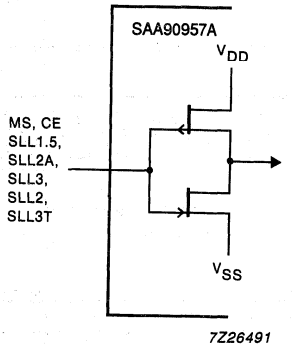


Fig.5 MS, CE, SLL2A, SLL3, SLL2 and SLL3T inputs.

DEVELOPMENT DATA

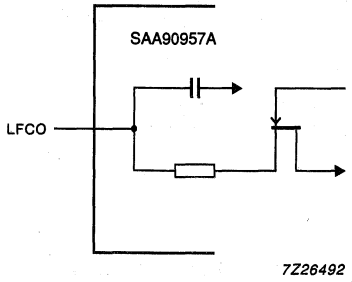


Fig.6 LFCO input.

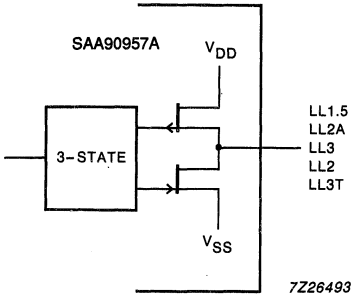


Fig.7 LL1.5, LL2A, LL2, LL3 and LL3T outputs.

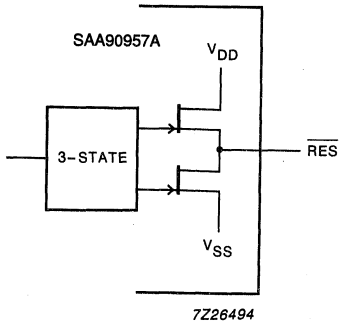


Fig.8 RES output.

APPLICATION INFORMATION

PLL

Table 1 Characteristics

parameter	symbol	typ.*	unit
Natural frequency	ω_n	6×10^5	1/s
Damping coefficient	δ	1	
Jitter		1.7	ns
Lock-in range	Δf	2 to 8	MHz
Rise and fall time (0.8 V to 2.0 V)	t_r, t_f	3	ns

Supply

To obtain optium performance from the SAA9057A, the following points should be taken into consideration:

- Supply pins must be connected to ground via a ceramic capacitor.
- Ground connections should be as inductance-free as possible. Therefore, a ground-plane layout would be preferable.
- Analog supply must be decoupled to avoid ripple over from another supply.
- LFCO signal and analog supply voltage must refer to the V_{SSA} pin.
  However, a separation of the digital and analog ground is not essential.

* Typical values are measured on a sample basis and are not guarenteed for the complete voltage and temperature range.

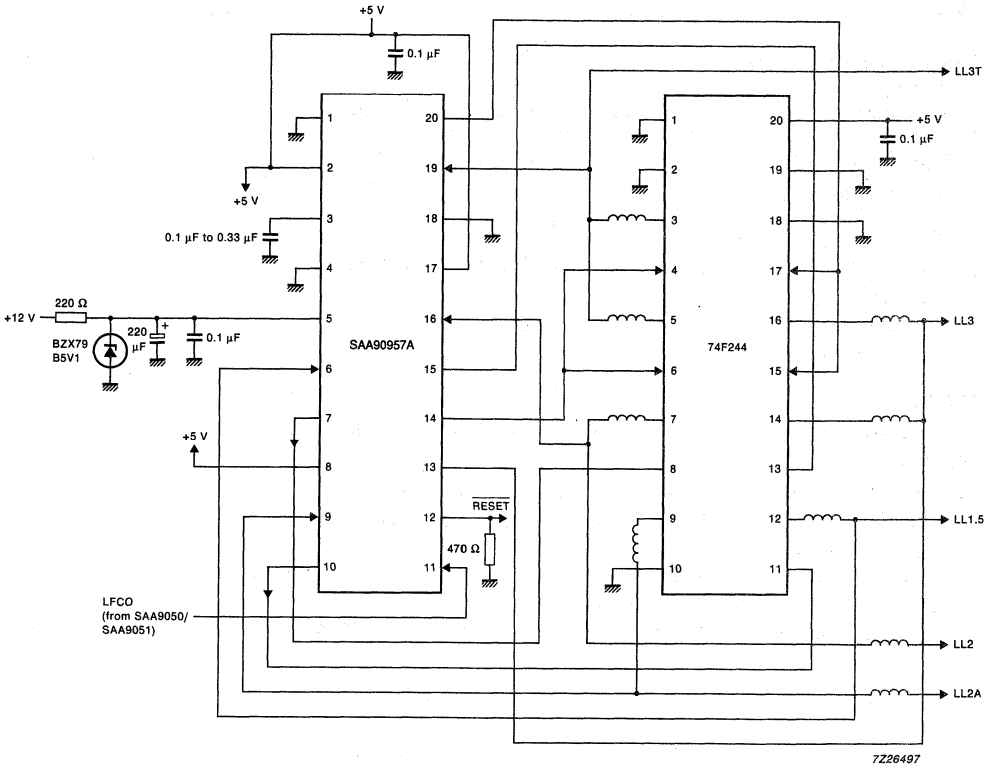


Fig.9 Application diagram; to prevent RF reflections it is recommended that the coils shown are of the square-loop ferrite core type.

SAMPLE-RATE CONVERTER

GENERAL DESCRIPTION

The SAA9058 sample-rate converter (SRC) is for use in digital TV receiver applications. It converts the sampling rate of digital signals by a factor of 2/3, e.g. from 20,25 to 13,5 MHz, using a phase-linear, finite impulse response (FIR) filter with time-varying coefficients. Only two clocks are required; the data format is two's complement, and the word length at both input and output is seven bits.

The FIR filter creates a filter-algorithm to interpolate digitized composite video signals (DCVBS) into a slower sample rate that is suitable for video decoding. The circuit gives low attenuation of colour subcarrier, gives high rejection of aliasing components and has unity DC gain.

It is intended for use with the 7-bit analogue-to-digital converter PNA7509 and the digital multistandard decoder SAA9050, with DCVBS in PAL, NTSC or SECAM. Other applications are digital anti-aliasing filtering, rejection of harmonics caused by analogue-to-digital conversion and data reduction.

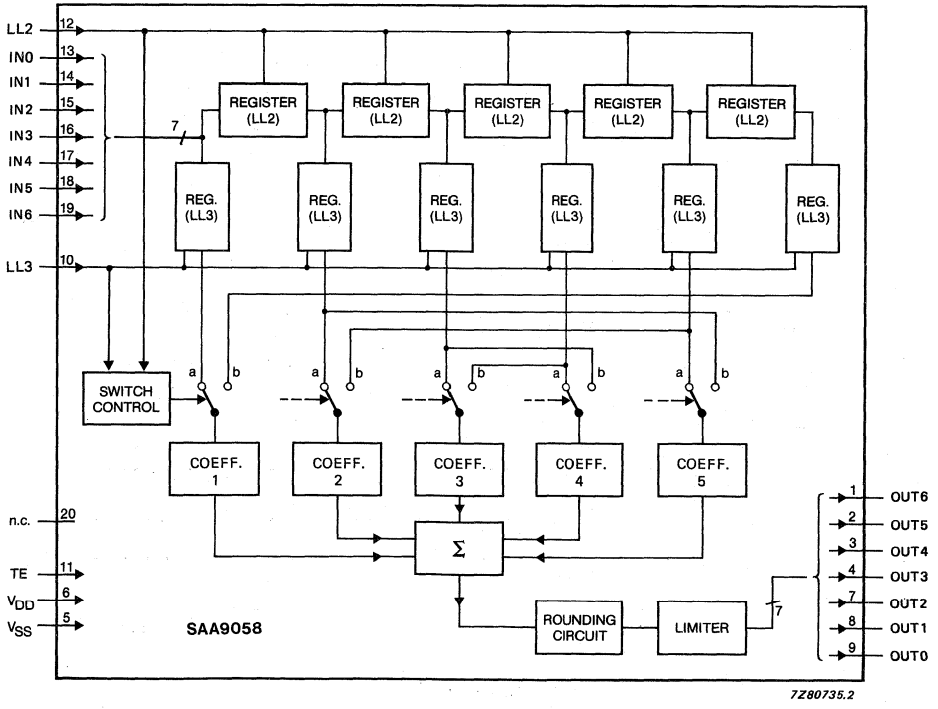


Fig. 1 Block diagram (see Fig. 3 for switch timing).

PACKAGE OUTLINE

20-lead DIL; plastic (SOT146).

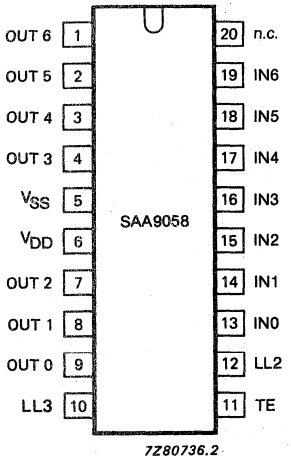


Fig. 2 Pinning diagram.

PINNING

1	OUT6	output data
2	OUT5	
3	OUT4	
4	OUT3	
5	V_{SS}	ground (0 V)
6	V_{DD}	positive supply voltage (+5 V)
7	OUT2	output data
8	OUT1	
9	OUT0	
10	LL3	output clock
11	TE	production test input; V_{SS} for all applications
12	LL2	input clock
13	IN0	input data
14	IN1	
15	IN2	
16	IN3	
17	IN4	
18	IN5	
19	IN6	
20	n.c.	not connected

OPERATION

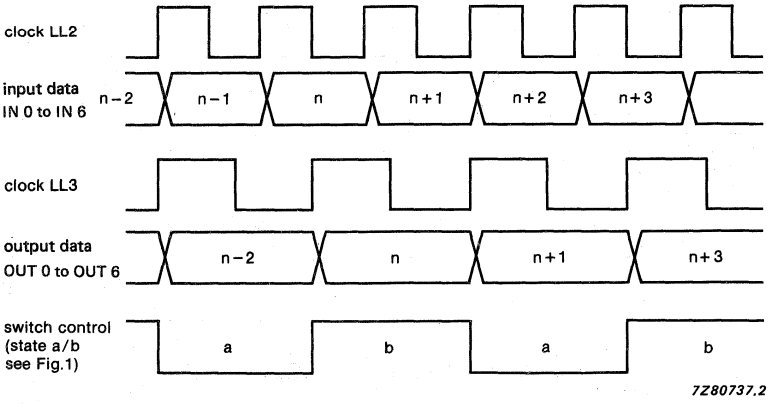


Fig. 3 Relationship of inputs to outputs.

Frequency response

The virtual frequency response in the 2 x LL2 (40,5 MHz) domain is interpreted as the characteristic of the interpolation filter directly before conversion to the LL3 (13,5 MHz) sample rate and the spectral components beyond LL3/2 are aliased into the baseband.

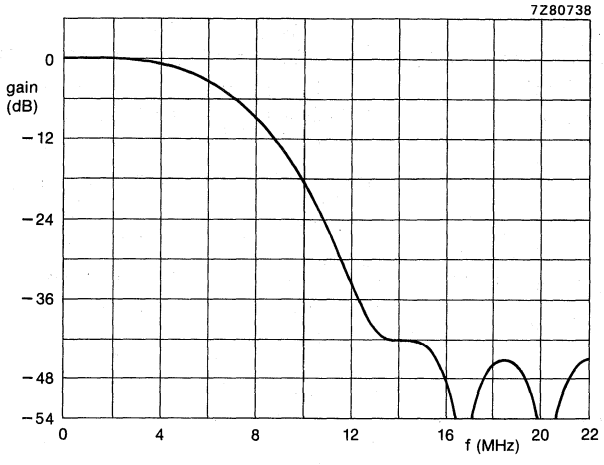


Fig. 4 Frequency response.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7 V
Input voltage range	V_I	−0,5 to + 7 V
Output voltage range to $I_{O\,max}$ = 20 mA	V_O	−0,5 to + 7 V
Maximum power dissipation	P_{tot}	0,5 W
Operating ambient temperature range	T_{amb}	0 to + 70 °C
Storage temperature range	T_{stg}	−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage range	V_{DD}	4,5	5,0	5,5	V
Supply current at V_{DD} = 5,5 V, data outputs not connected, data inputs LOW and frequency nominal	I_{DD}	–	< 100*	65	mA
Inputs					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH (except LL2, LL3)	V_{IH}	2,0	–	V_{DD}	V
Input voltage HIGH (LL2, LL3)	V_{IH}	2,4	–	V_{DD}	V
Input leakage current	I_I	–	–	10	μA
Input capacitance (LL2)	C_I	–	–	10	pF
Input capacitance (LL3)	C_I	–	–	10	pF
Input capacitance (D0 to D6)	C_I	–	–	5	pF
Outputs					
Output voltage HIGH at I_{OH} = −0,5 mA	V_{OH}	2,4	–	V_{DD}	V
Output voltage LOW at I_{OH} = 2,0 mA	V_{OL}	0	–	0,6	V
Timing (Fig. 5)					
LL2 cycle time	t_{C2}	46	–	53	ns
LL2 duty factor t_{C2H}/t_{C2}	–	45	–	55	%
LL2 rise and fall time	t_r, t_f	–	–	6**	ns
LL3 cycle time	t_{C3}	69	–	80	ns
LL3 duty factor t_{C3H}/t_{C3}	–	45	–	55	%
LL3 rise and fall time	t_r, t_f	–	–	6**	ns
Skew time	t_{skew}	−2	–	+ 2	ns
Input data set-up time	t_{SU}	12	–	–	ns
Input data hold time	t_{HD}	3	–	–	ns
Output data load capacitance	C_L	7,5	–	15	pF
Output data hold time	t_{OH}	3	–	–	ns
Output data delay time	t_{OD}	–	–	33	ns

* For digital TV application.

** Difference between t_r, t_f of LL2 and t_r, t_f of LL3 shall be less than 2 ns. Rising and falling edges of clocks are assumed to be smooth due to low pass filtering.

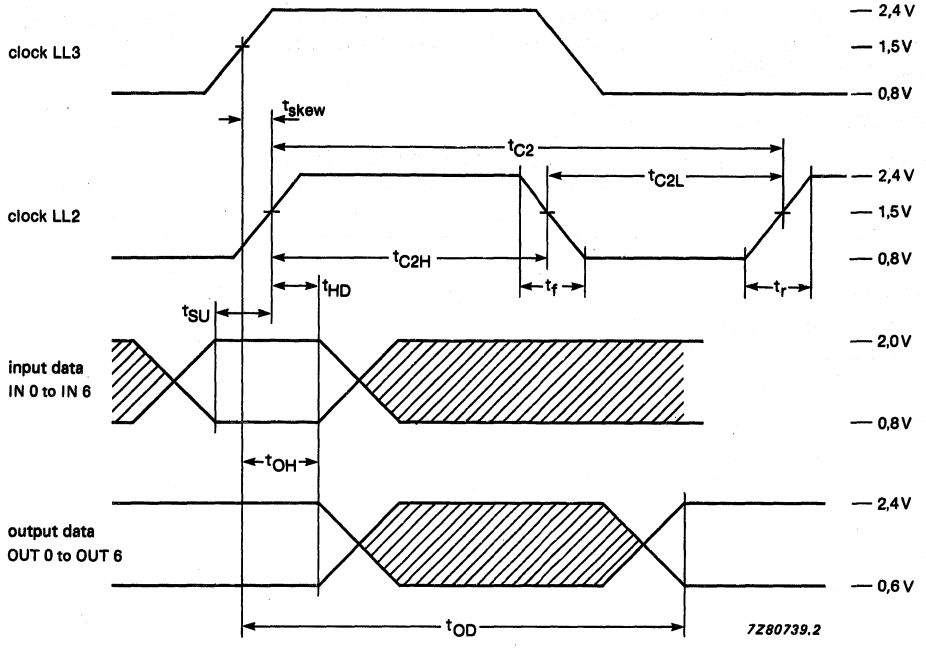


Fig. 5 Timing diagram.

VIDEO PROCESSOR WITH DACs (VDA)

GENERAL DESCRIPTION

The SAA9060 is a video processor with DACs (VDA), which converts the digital luminance and chrominance data into analogue information for a RGB controller. The SAA9060 forms part of a chip-set for digital TV systems.

Features

- Single scan or double scan applications
- Parallel data input
- 7-bit D/A conversion of the colour difference signals
- 8-bit D/A conversion of the luminance signal

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Input current		I_{DD}	–	170	250	mA
Power dissipation		P_{tot}	–	–	1.4	W
Back-bias voltage			−3	–	0	V
Operating ambient temperature range		T_{amb}	0	–	+ 70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

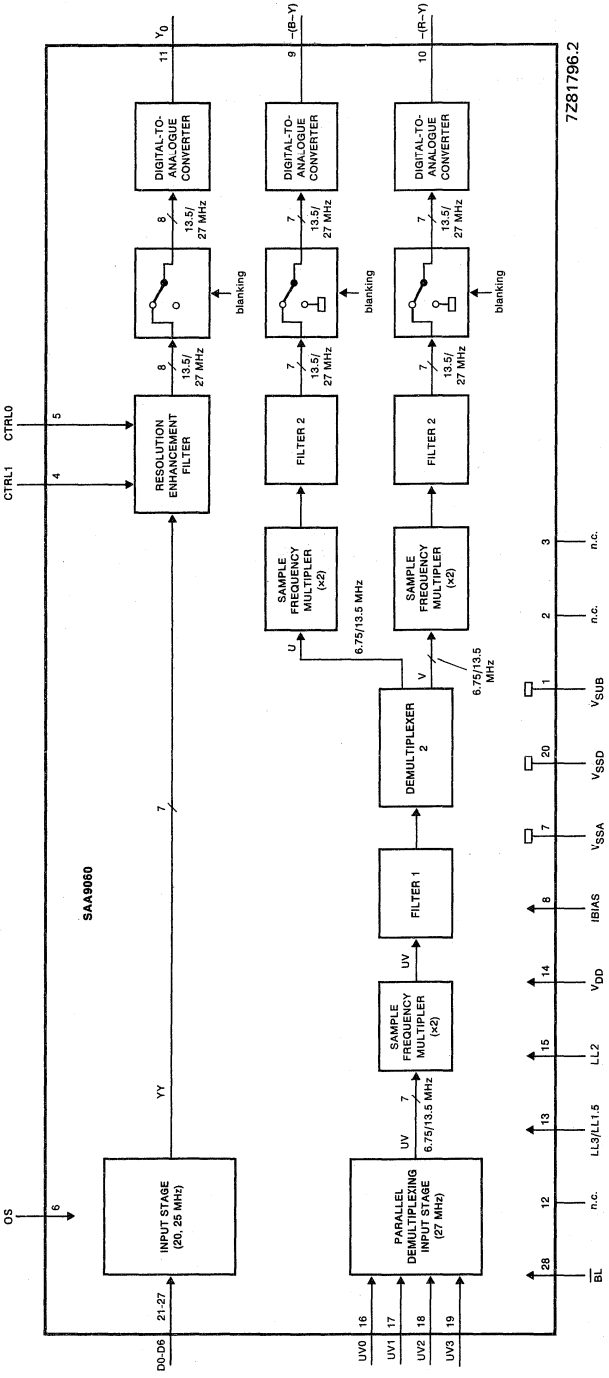


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

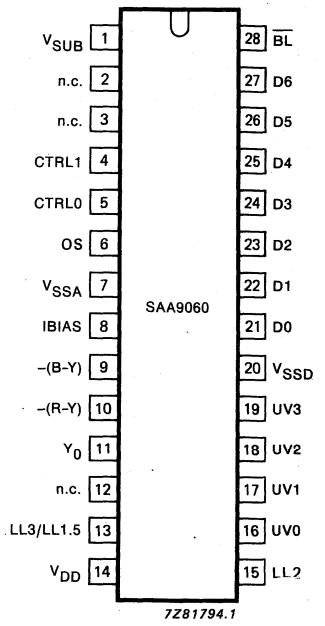


Fig.2 Pinning diagram.

1	V_{SUB}	Substrate pin for external capacitor, smooths internally generated voltages
2, 3	n.c.	Not connected
4	CTRL1	Control input for resolution enhancement filter
5	CTRL0	Control input for resolution enhancement filter
6	OS	Data format switch-over (from serial to parallel) at inputs DO...D6, UVO...UV3, BLN
7	V_{SSA}	Analogue ground
8	IBIAS	Reference current for the DACs
9	–(B-Y)	Chrominance analogue output; inverted colour difference signal B-Y
10	–(R-Y)	Chrominance analogue output; inverted colour difference signal R-Y
11	Y_O	Luminance analogue output
12	n.c.	Not connected
13	LL3/ LL1.5	Clock input: single scan parallel mode, f = 13.5 MHz double scan parallel mode, f = 27 MHz

PINNING (continued)

14	V_{DD}	Supply voltage
15	LL2	(Clock input for data word D0...D6) for serial data format only*/ f = 20.25 MHz; low-level version Do not connect pin when selecting parallel data format
16	UV0	Digital chrominance input; f = 13.5 MHz or 27 MHz
17	UV1	
18	UV2	
19	UV3	
20	V_{SSD}	Digital ground (0 V)
21	D0	Digital 7-bit luminance input; f = 13.5 MHz or 27 MHz
22	D1	
23	D2	
24	D3	
25	D4	
26	D5	
27	D6	
28	$\overline{BL}$	Format input; indicates the start of a transmission of a data line

FUNCTIONAL DESCRIPTION (see Fig. 1)

The VDA, DMSD/S-DMSD and a RGB controller form the video channel of a digital TV system. The VDA receives the luminance and chrominance data from the DMSD/S-DMSD and converts this data into an analogue output for a RGB controller.

Chrominance data signal

The chrominance data consist of alternating UV samples with a sample frequency of 3.375 MHz (single scan), the sample frequency is increased to 13.5 MHz by using two cascaded interpolation filters. The 7-bit chrominance data is then converted to an analogue signal (inverted colour difference signals B-Y and R-Y) for use in a RGB controller.

Luminance data signal

The luminance data frequency is clocked at 13.5 MHz or 27 MHz into the resolution enhancement filter (controlled by CTRL0 and CTRL1), this improves the quantization noise behaviour in areas with small variation and produces an 8-bit data output. The 8-bit data is converted into an analogue signal for use in a RGB controller.

$\overline{BL}$ signal (see Fig. 3)

The $\overline{BL}$ signal is used to indicate the active video length within the line and synchronizes the demultiplexing of the UV data.

Operating modes

There are two operating modes:

- parallel data transmission (single scan); LL3/LL1.5 = 13.5 MHz
- parallel data transmission (double scan), LL3/LL1.5 = 27 MHz.

Output signals

The output signals are AC-coupled to a RGB controller. During the horizontal synchronization gap the luminance and chrominance signals are blanked (black and no colour difference respectively) and the RGB controller clamps the input signals.

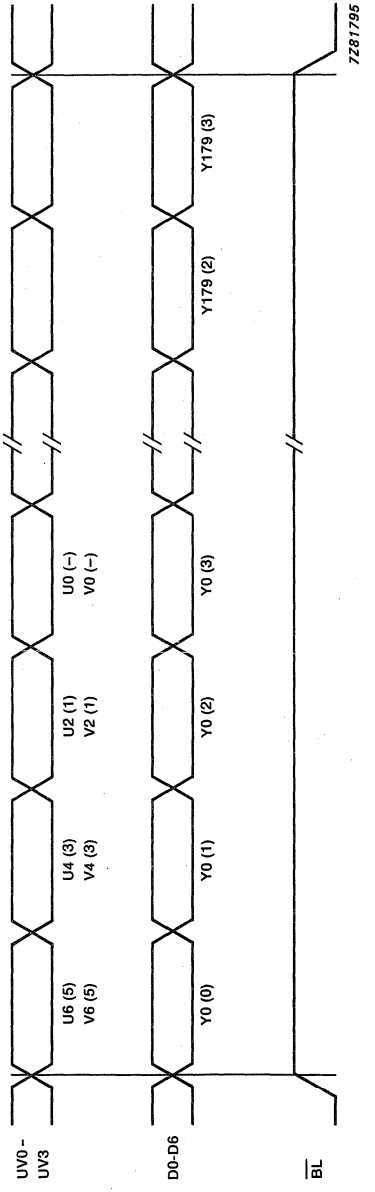


Fig.3 Data format.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.3	6.0	V
Input voltage		V_I	−0.5	6.0	V
Back-bias voltage		V_{BIAS}	−3	0	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	0	+ 70	°C

THERMAL RESISTANCE

Junction to ambient	$R_{th\,j\text{-}a}$	50 K/W

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all values referred to V_{SS}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current		I_{DD}	*	170	250	mA
Voltage on pin 1	with clock	V_{SUB}	−3.0	−2.5	−2.0	V
Current on pin 1	without clock	I_{SUB}	−	0.2	40	μA
Voltage ripple on pin 1		V_{ripple}	−	−	10	mV
Inputs						
LL3 input signal	note 1; see Fig. 4					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL3 time period	f_{nom} = 13.5 MHz	t_{LL3}	69	74	80	ns
Duty factor		t_{PH}/t_{LL3}	43	50	57	%
LL1.5 input signal	note 2; see Fig. 5					
Input voltage HIGH		V_{IH}	2	−	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	−	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	−	−	10	pF
LL1.5 time period	f_{nom} = 27 MHz	$t_{LL1.5}$	35	37	40	ns
Duty factor		$t_{PH}/t_{LL1.5}$	43	50	57	%

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{BL}$ input signal	note 3; see Figs 6 and 7					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
Pulse width HIGH		t_{PH}	–	720	–	*
Pulse width LOW	NTSC/PAL	t_{PL}	–	138/144	–	*
LL3 set-up time		t_{SU}	12	–	–	ns
D0-D6 and UV0 to UV3	note 2; see Fig. 8					
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	−0.5	–	0.8	V
Input capacitance (pin 20)	V_I = 0 V	C_I	–	–	10	pF
Input current HIGH		I_{IH}	–	–	1	μA
Input current LOW		I_{IL}	–	–	100	μA
LL1.5 set-up time		t_{SU}	13	–	–	ns
LL1.5 hold time		t_{HD}	3	–	–	ns
CTRL0 and CTRL1 input signals	note 4					
Input voltage HIGH	note 5	V_{IH}	2	–	V_{DD}	V
Input voltage LOW	note 5	V_{IL}	V_{SS}	–	0.8	V
Input capacitance**	V_I = 0 V	C_I	–	–	10	pF
IBIAS input signal	Fig. 9					
Input current	note 6	I_{IBIAS}	–	100	–	μA
Bias resistance	note 7	R_{IBIAS}	–	39	–	kΩ
Input voltage	note 7	V_{IBIAS}	–	V_{DD}	–	V
Potential difference across R_{IBIAS}	note 8	U_{IBIAS}	–	1.5	–	V

* Clock periods of LL3.
** Referred to pin 20.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
Y signal output	note 9					
Resolution			–	8	–	bits
Nominal range	max. 255		14	–	230	
Output current	max. 2.55	I_O	0.14	–	2.3	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	10	–	μA
Load on pin 11		R_L	–	180	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	47	–	nF
Total output capacitance (pin 11)	note 10	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L$ ($C_S + C_D + C_E$)	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			–0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			–1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS} = 0$		–0.5	–	+ 0.5	LSB
Glitch			–0.5	–	+ 0.5	LSB
–(B-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		13	–	114	
Output current		I_O	0.26	–	2.28	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 9		R_L	–	750	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 9)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L$ (C_S + C_D + C_E)	t_C	–	50	–	ns

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	$\Delta I_{IBIAS}=0$		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB
−(R-Y) signal output	note 10					
Resolution			–	7	–	bits
Nominal range	max. 127		10	–	117	
Output current	max. 2.55		0.2	–	2.34	mA
Resolution per step	I_{IBIAS} = 100 μA	Res	–	20	–	μA
Load on pin 10		R_L	–	560	–	Ω
Coupling capacitance to RGB controller	see Fig. 10	C_{OC}	–	10	–	nF
Total output capacitance (pin 10)	including pin capacitance and wiring	C_O	–	7	–	pF
Conversion time		t_{DAC}	–	–	30	ns
Time constant	$\approx R_L (C_S + C_D + C_E)$	t_C	–	50	–	ns
Output voltage range		V_O	$V_{DD}-2$	–	V_{DD}	V
Differential non-linearity			−0.5	–	+ 0.5	LSB
Equality of converter output normalized to maximum level			−1	–	+ 1	LSB
Temperature dependency	ΔI_{IBIAS}		−0.5	–	+ 0.5	LSB
Glitch			−0.5	–	+ 0.5	LSB

Notes to the characteristics

1. 25/30 Hz picture frequency with interlace.
2. 50/60 Hz picture frequency, parallel data transmission.
3. 25/30 Hz picture frequency, f = 20.25 MHz.
4. Static input signal; input HIGH by means of an internal pull-up resistor of 100 kΩ.
5.

CTRL1	CTRL0	filter function
0	0	bypass (min.)
1	1	lowpass (max.)

6. When I_{IBIAS} = 100 μA the quantization steps of the Y output DAC is 10 μA and −(B-Y), −(R-Y) outputs are 20 μA. The maximum voltage at R_L is 2 V. If R_{IBIAS} is used, the temperature coefficients of I_{BIAS} and the DACs are compensated.
7. Effective voltage noise is ⩽ 1 mV.
8. U_{IBIAS} = 1.2 V + I_{IBIAS} x 3 kΩ.
9. Values measured from the Y output DAC.
10. Values measured from the −(B-Y) output DAC.

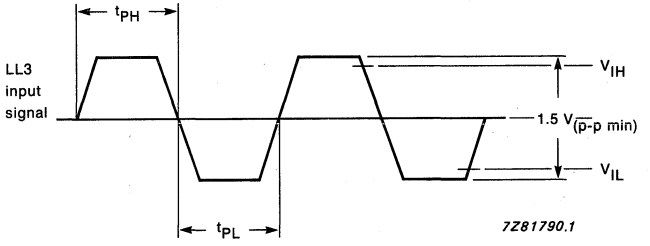


Fig. 4 LL3 timing waveform; 25/30 Hz picture frequency with interlace.

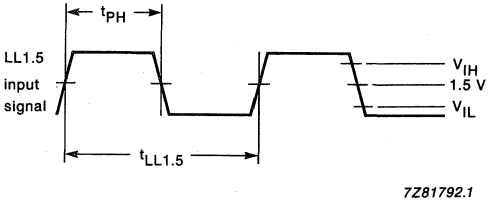


Fig. 5 LL1.5 timing waveform; 50/60 Hz picture frequency, parallel data transmission.

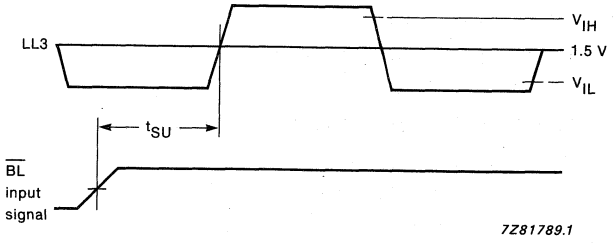


Fig. 6 $\overline{BL}$ timing waveform; 25/30 Hz picture frequency; f = 13.5 MHz.

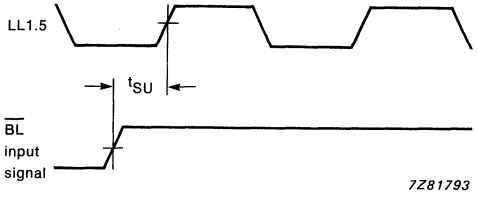


Fig. 7 $\overline{BL}$ timing waveform; 50/60 Hz picture frequency; f = 27 MHz.

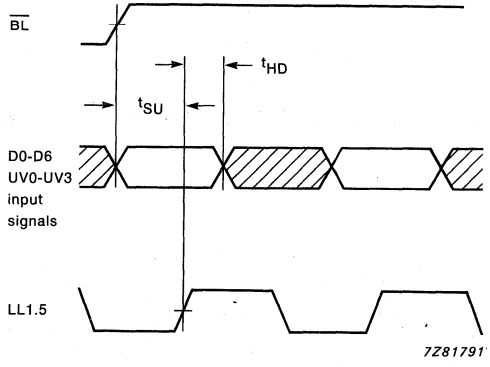


Fig. 8 D0 to D6 and UV0 to UV3 timing waveform; 50/60 Hz picture frequency, f = 27 MHz.

APPLICATION INFORMATION

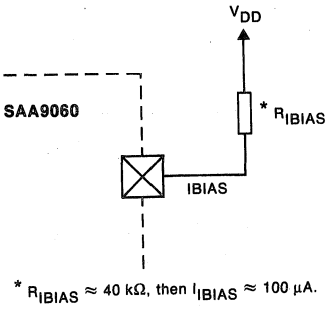
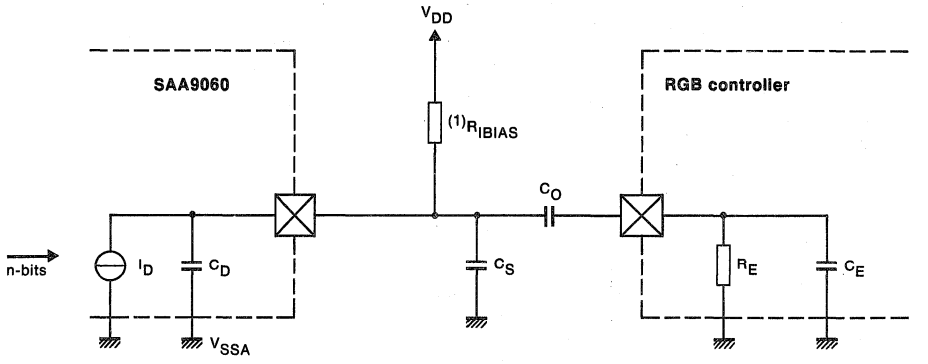


Fig. 9 IBIAS input circuit.



(1) $R_{IBIAS} = R_L$ (Y output), R_L (B-Y output), R_L (R-Y output)

Fig. 10 Application of the DACs.

Philips Components

Data sheet	
status	Objective specification
date of issue	July 1990

SAA9065P

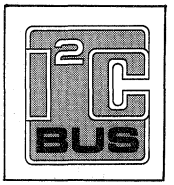
Video enhancement and digital-analog processor

GENERAL DESCRIPTION

The digital video signal processing system is based on the Digital Multistandard Decoder (DMSD) SAA7151 and the 'Video Enhancement and Digital-Analog processor' (VEDA) SAA9065. The decoder provides a reference signal for generating a line-locked clock which in turn allows simple application of memory based features.
The VEDA is the back end for the digital processing path which includes decoding and feature processing. The system supports a digital YUV bus for selection of different video signal sources.

The data rate supported by the bus is:
13.5 MHz = 858 x fh (NTSC) or
864 x fh (PAL/SECAM) and
27 MHz = 1716 x fh (NTSC) or
1728 x fh (PAL/SECAM).
The support organization is : 7 and 8 bit.
The number of active samples per line is : 720 on the YUV bus.
The system provides a line locked clock (LL27) of 27 MHz.

The YUV bus and the VEDA data input are fully synchronous with respect to the clock signal LL27. A line reference signal HREF, for timing control purposes, is provided by the decoder which controls the system timing independent of active signal sources or desired functions.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD(d)}$	digital supply voltage	4.5	5.5	V
$V_{DD(a)}$	analog supply voltage	4.5	5.5	V
T_{amb}	operating ambient temperature range	0	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9065P	44	PLCC	plastic	SOT187AA,AGA

FUNCTIONAL DESCRIPTION

The VEDA will be produced in a CMOS process. The device operates at a frequency of either 13.5 MHz or 27.0 MHz (in progressive scan applications). 7 and 8 input signal wordwidths for luminance Y and colour difference signals U and V are supported.
The data formats on the external YUV data bus must correspond to the specified formats given in Tables 1 and 2.
For processing functions the VEDA contains (see Fig.1);

- a **formatter** unit at the digital input, to convert the supported data formats into a processable internal data stream
- a **timing control** block, which generates the necessary clock and synchronization signals for the internal processing
- an **I²C-bus** interface, which decodes the external control information into internal control switches
- an **H-peaking** unit, which performs horizontal peaking on the luminance information
- an **interpolation** filter for 4:1:1 and 4:2:2 formats in the chrominance path, to increase the data rate of the colour difference signals up to 13.5 (27.0) MHz in front of the digital-to-analog conversion
- a **DCTI** (Digital Colour Transition Improvement) block to increase the sharpness of colour transitions.

Prior to the digital-to-analog conversion, depending upon the connected RGB processor;

- it is possible to change the polarity of the colour difference components
- the data is matched to a unipolar DAC
- the digital outputs are clamped during the horizontal blanking period.

Table 1 The 4:2:2 signal format

BUS SIGNAL						
Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0
bus clock	0	1	2	3	4	5
time frame	0		1		2	

Data rate: 13.5 MHz

Sample frequency:

- Y = 13.5 MHz
- U = 6.75 MHz
- V = 6.75 MHz

The quoted frequencies are valid on the YUV bus if the bus clock is 13.5 MHz.
The time frames are controlled by the HREF signal.

Table 2 The 4:1:1 signal format

BUS SIGNAL								
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV4	V6	V4	V2	V0	V6	V4	V2	V0
bus frame	0	1	2	3	4	5	6	7
time frame	0				1			

Data rate: 13.5 MHz

Sample frequency:

- Y = 13.5 MHz
- U = 3.375 MHz
- V = 3.375 MHz

The quoted frequencies are valid on the YUV bus if the bus clock is 13.5 MHz.
The time frames are controlled by the HREF signal.

Video enhancement and digital-analog processor

SAA9065P

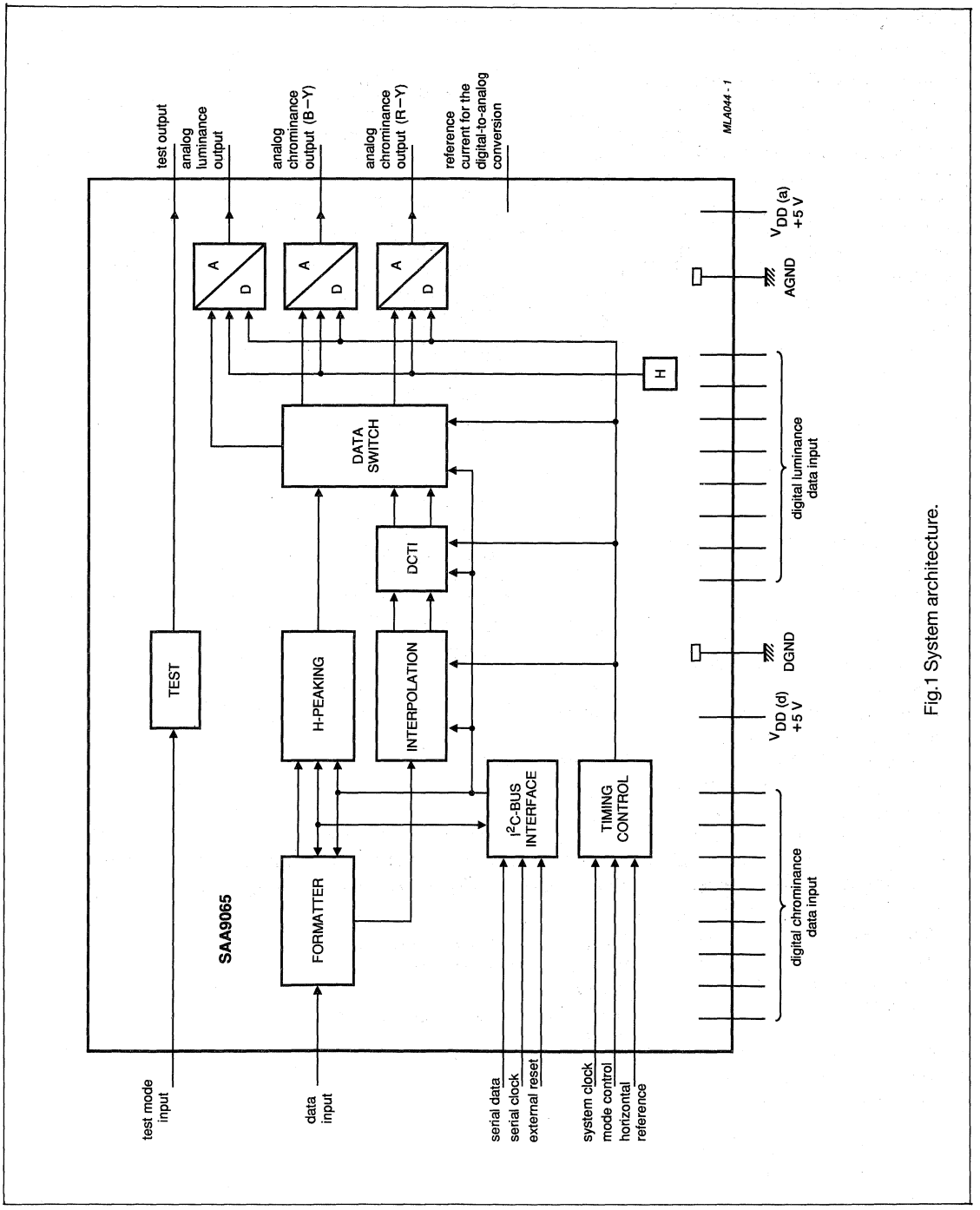


Fig.1 System architecture.

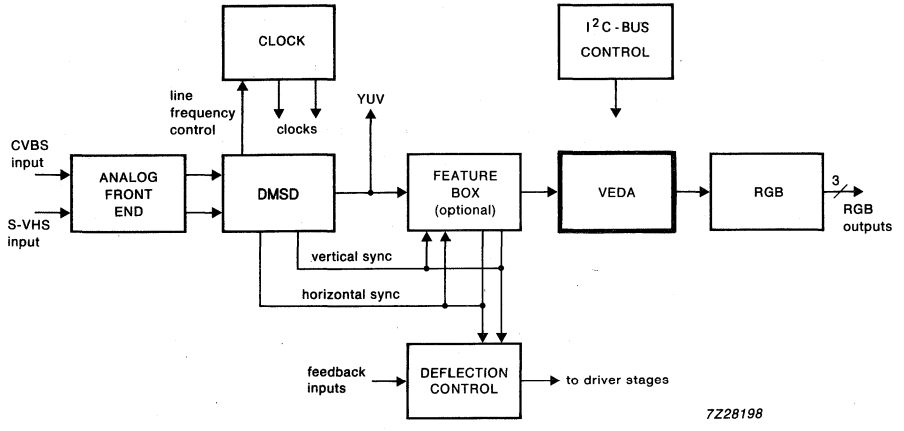


Fig.2 VEDA block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The SAA9079 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

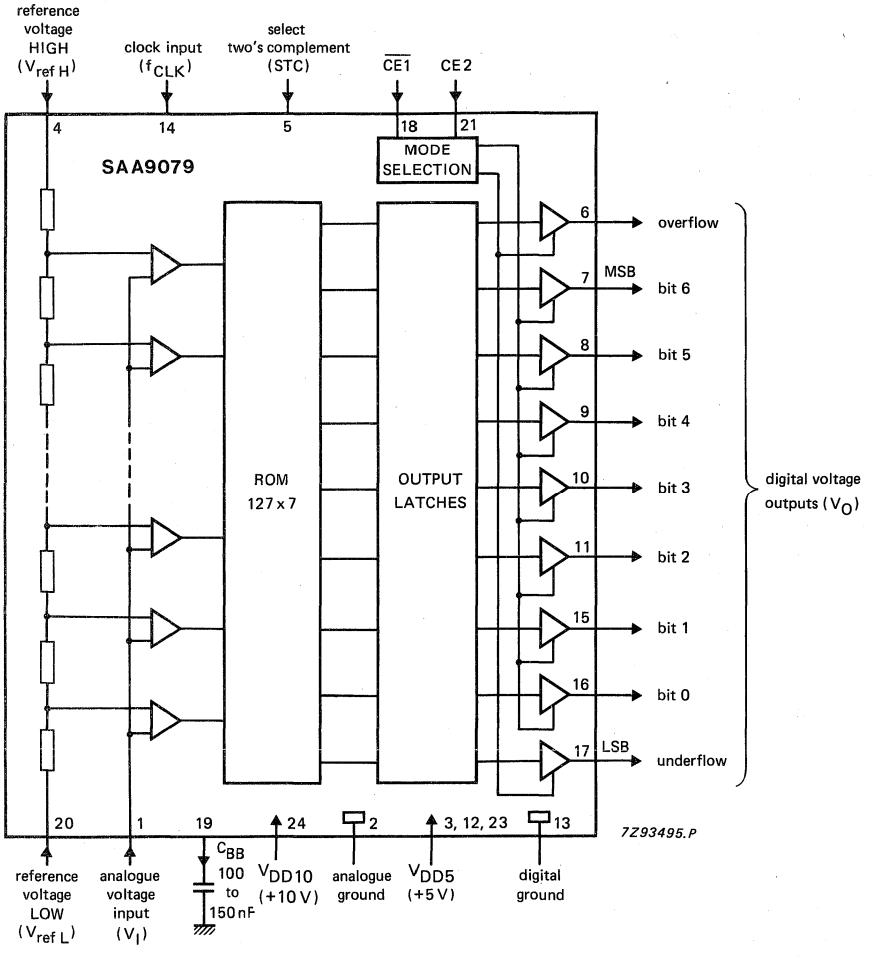
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)		V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)		V_{refH}	5.0	5.1	5.2	V
Non-linearity	f_i = 1.1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
–3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).
24-lead mini-pack; plastic (SO24; SOT137A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

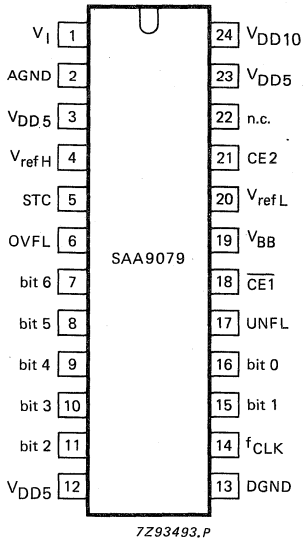


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0.5	+ 7.0	V
Supply voltage range (pin 24)	V_{DD10}	−0.5	+ 12.0	V
Input voltage range	V_I	−0.5	+ 7.0	V
Output current	I_O	−	5	mA
Total power dissipation	P_{tot}	−	1	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ to 10.5 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4.5	–	5.5	V
Supply voltage (pin 24)	V_{DD10}	9.5	–	10.5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2.4	2.5	2.6	V
Reference voltage HIGH (pin 4)	V_{refH}	5.0	5.1	5.2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0.3	–	0.8	V
Input voltage HIGH (note 1)	V_{IH}	3.0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2.6	–	V
Input capacitance (note 3)	C_{1-2}	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5.0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0.4	V
Output voltage HIGH at $-I_O$ = 0.5 mA	V_{OL}	2.4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2.50 V; V_{refH} = 5.08 V)

step	V_{1-2} note 1	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0	
underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1	
.	.	.	.	. . . .	. . . .	steps
.	.	.	.	. . . .	. . . .	2-125
.	.	.	.	. . . .	. . . .	
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0	
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1	
overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1	

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE1}$	CE2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

DEVELOPMENT DATA

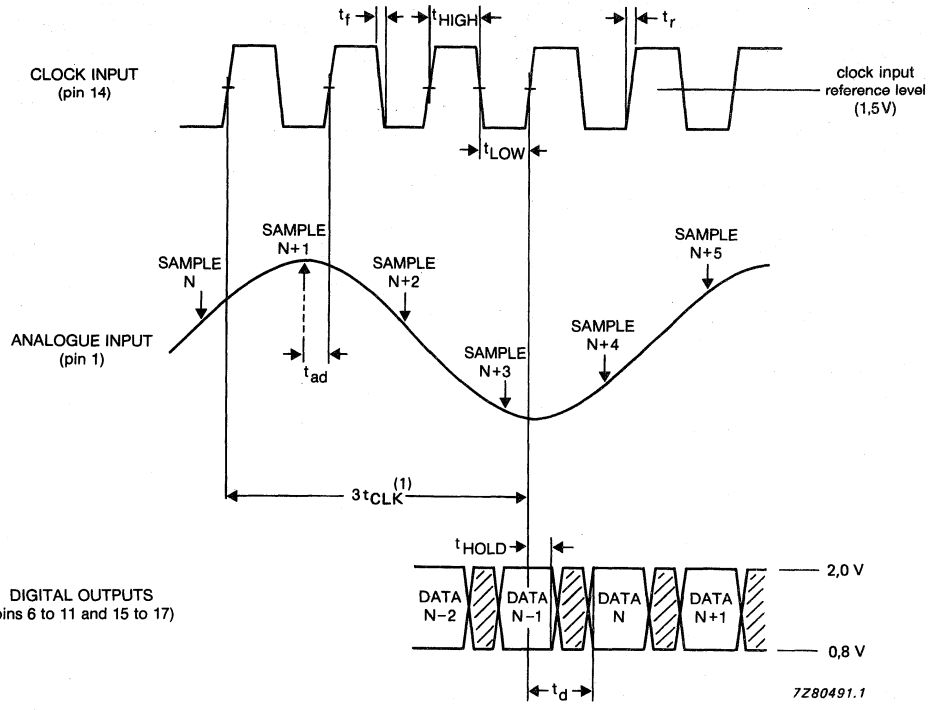
CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 4.5$ V to 5.5 V; $V_{DD10} = V_{24-2} = 9.5$ V to 10.5 V; $V_{refL} = 2.5$ V; $V_{refH} = 5.1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C

parameter	symbol	min.	max.	unit
Timing characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	5	ns
fall time	t_f	–	5	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise)		–	3	LSB
Harmonics (full scale)				
fundamental	f_0	–	0	dB
RMS (2nd and 3rd harmonic)	$f_{2.3}$	–	–28	dB
RMS (4th + 5th + 6th + 7th harmonic)	f_{4-7}	–	–35	dB
Digital outputs (notes 1 and 2)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at $C_L = 15$ pF	t_d	–	38	ns
Output delay time at $C_L = 50$ pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at $f_i = 1.1$ kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5 V.



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION INFORMATION

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; $V_{DD5} = 5$ V, $V_{DD10} = 10$ V, $T_{amb} = 22$ °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1.5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB
Duty factor (20.25 MHz)		50 ± 10	%

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching).
Even a spike duration of less than 1 μs can destroy the device.

DEVELOPMENT DATA

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Fig. 5 and 6).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.

After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.

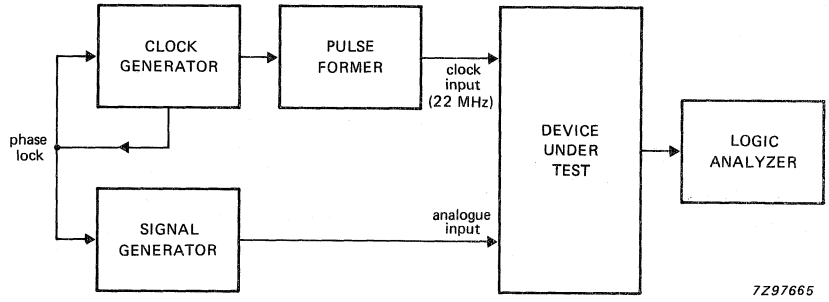
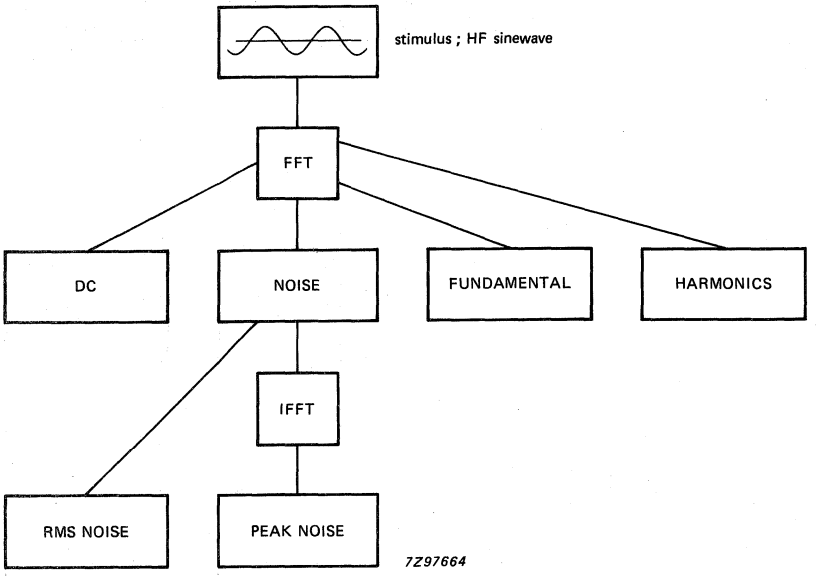


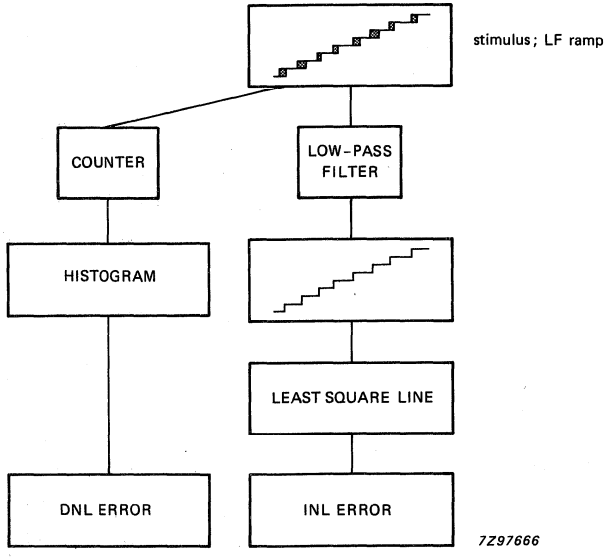
Fig. 4 Analogue-to-digital converter testing with locked signal source.

APPLICATION INFORMATION (continued)



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 6 Low frequency ramp test; linearity.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 16)	V_{P1}	typ.	12 V
(pin 22)	V_{P2}	typ.	13 V
(pin 17)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 16)	I_{P1}	typ.	32 mA
(pin 22)	I_{P2}	typ.	0,1 mA
(pin 17)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	400 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

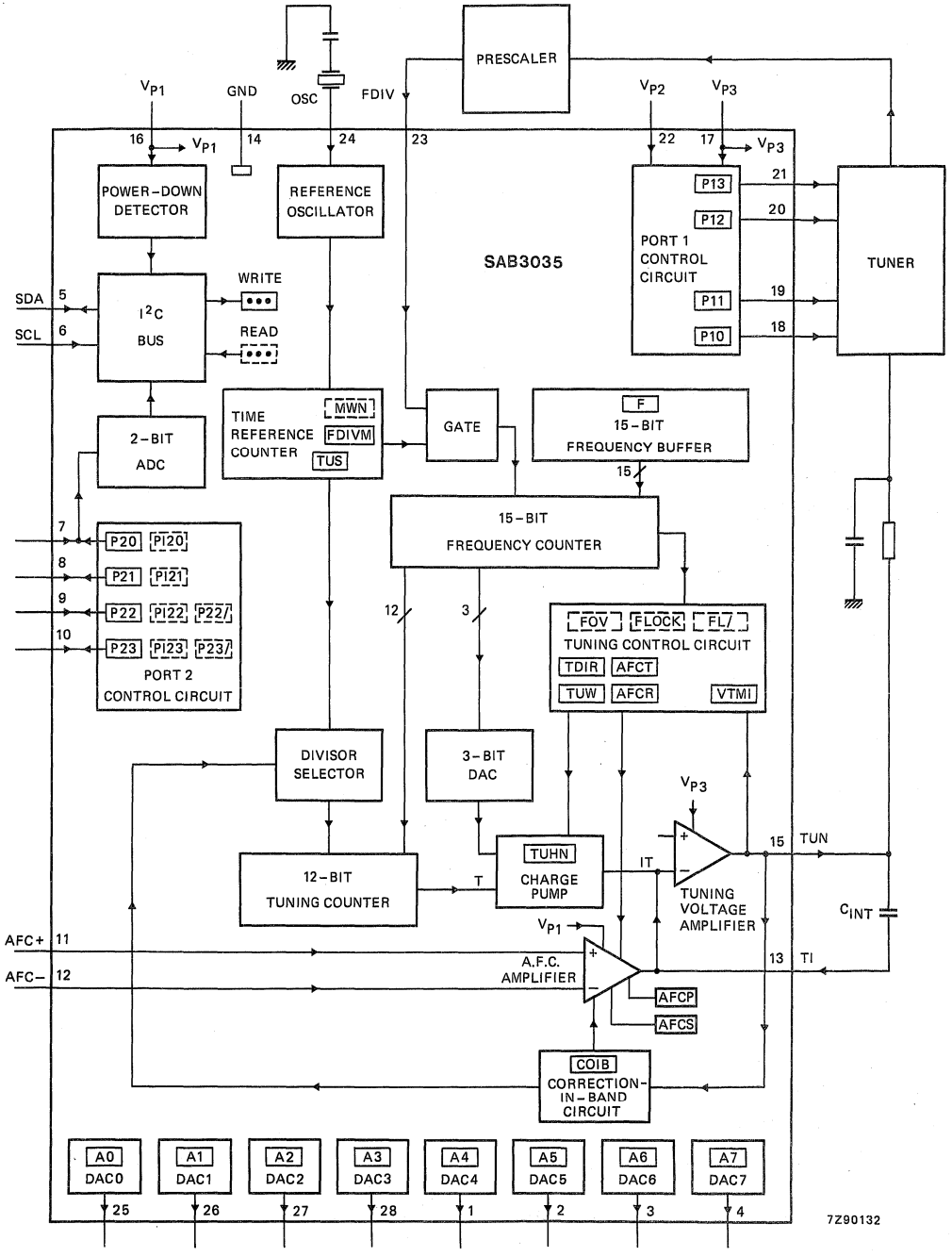


Fig. 1 Block diagram.

DEVELOPMENT DATA

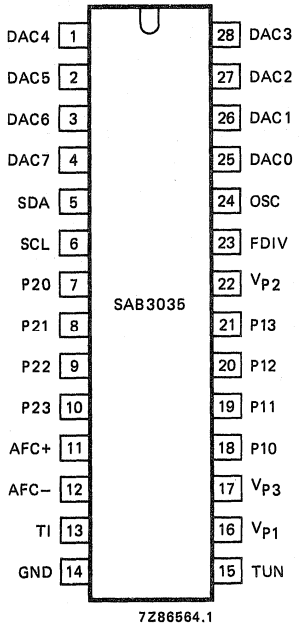


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC–	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

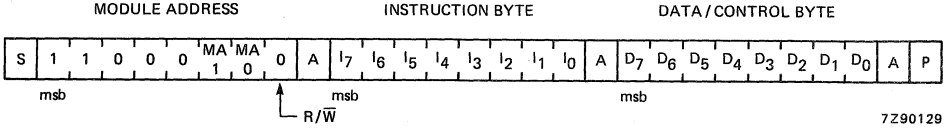


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at $\Delta f = 50$ kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at $\Delta f = 50$ kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

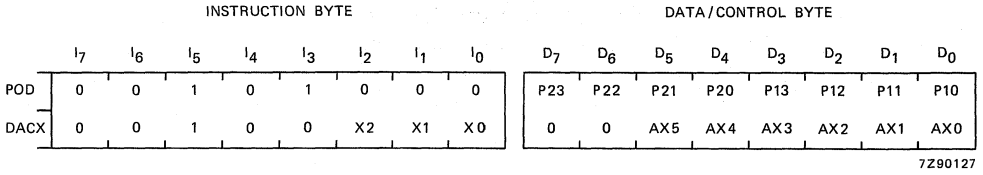


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

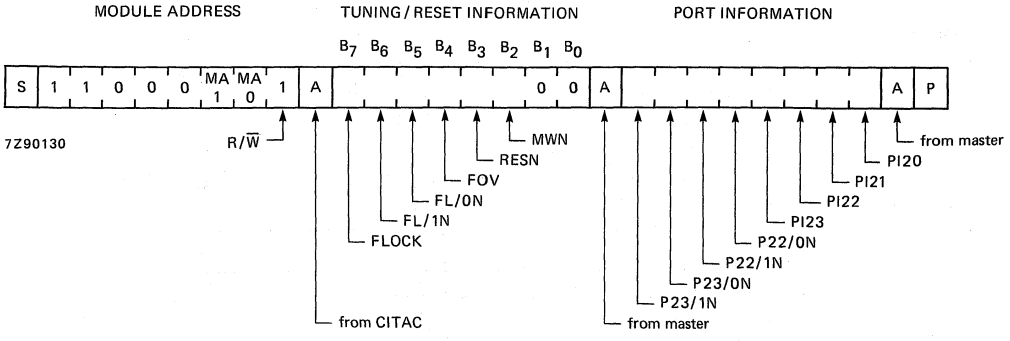


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

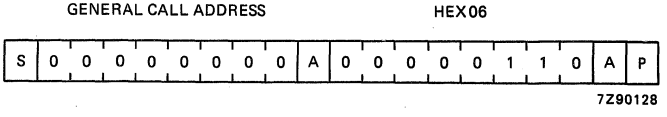


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0,3 to +18	V
(pin 22)	V_{P2}	−0,3 to +18	V
(pin 17)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0,3 to +18	V
(pin 6)	V_{SCL}	−0,3 to +18	V
(pins 7 to 10)	V_{P2X}	−0,3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 13)	V_{TI}	−0,3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0,3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

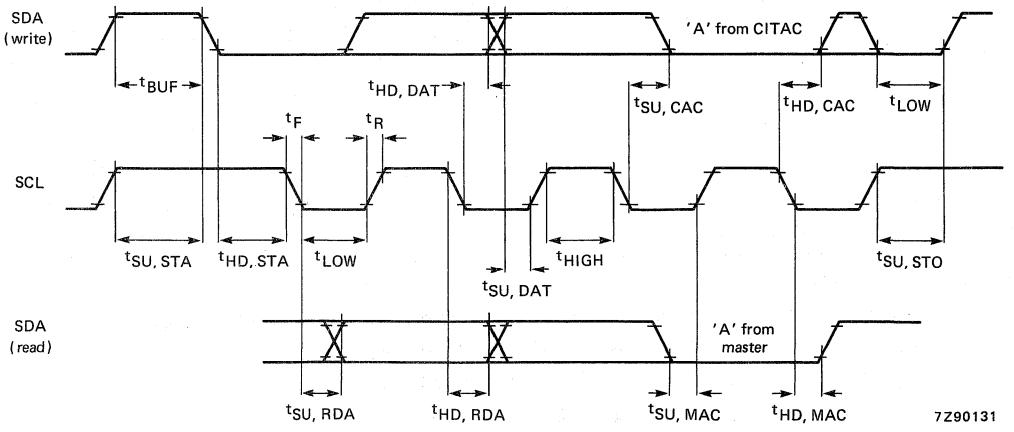


Fig. 8 I²C bus timing SAB3035.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I²C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I²C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0,1 mA
(pin 9)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

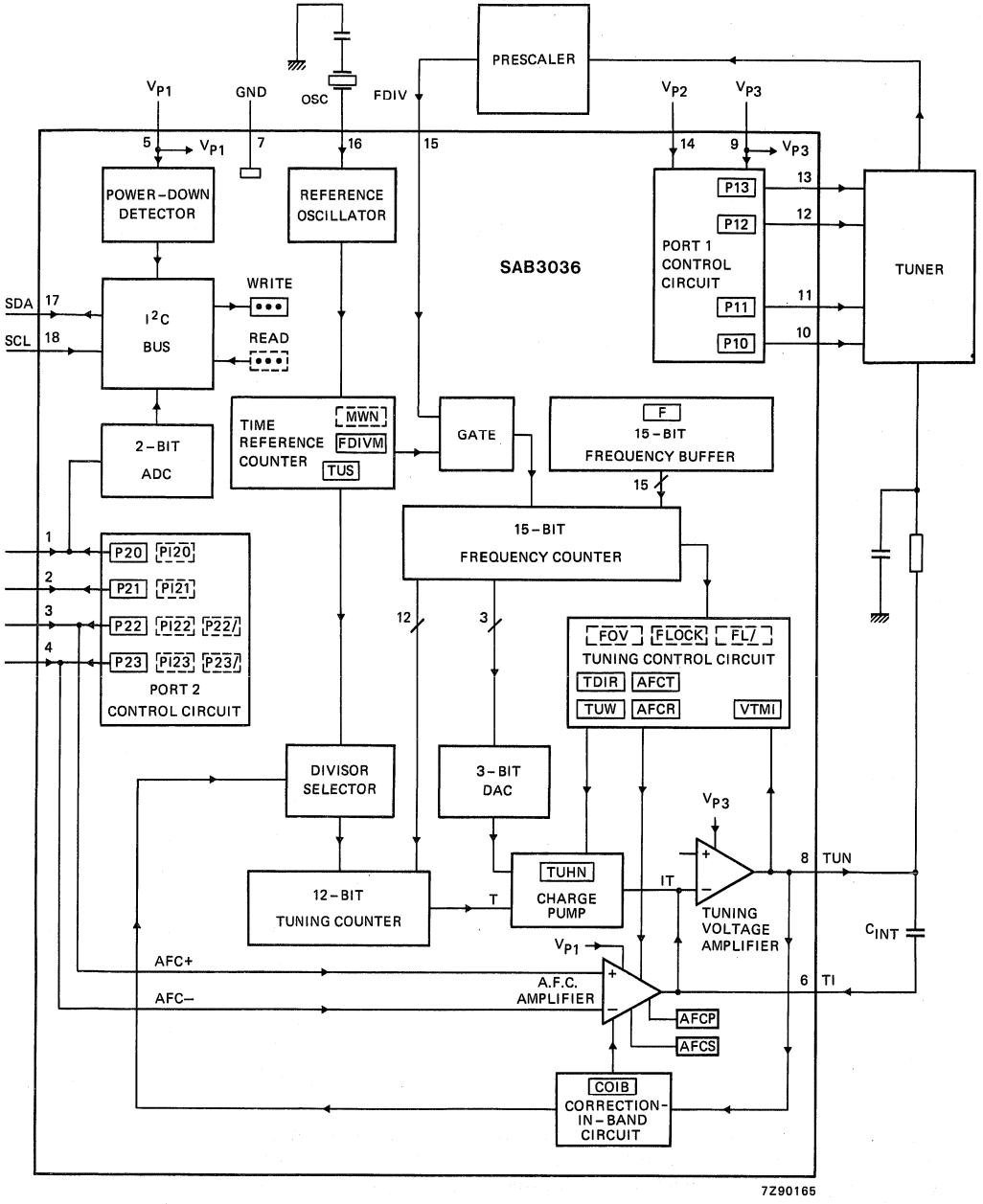


Fig. 1 Block diagram.

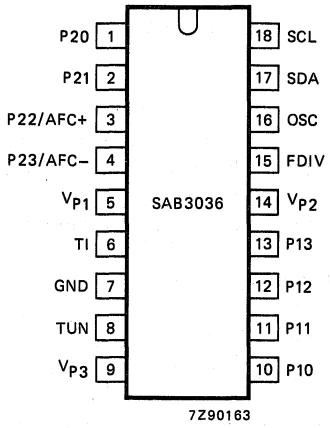


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC–	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I²C bus
18	SCL	serial clock line, I²C bus

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC− inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I²C bus; the I²C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

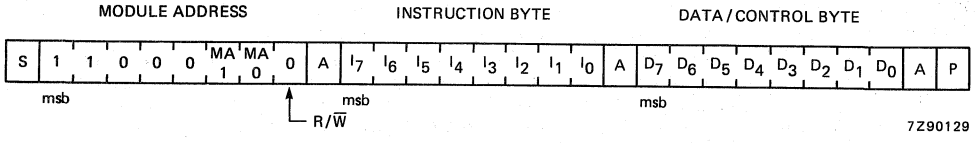


Fig. 3 I²C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at $\Delta f = 50$ kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at $C_{INT} = 1\ \mu F$ μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

DEVELOPMENT DATA

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	|Δf| (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as |Δf| is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	|Δf| (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

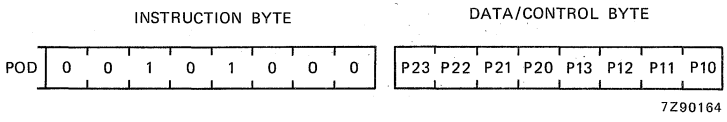


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

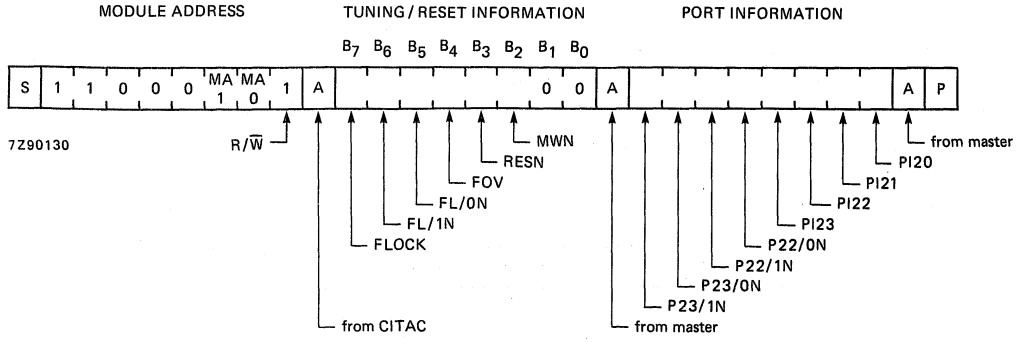


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

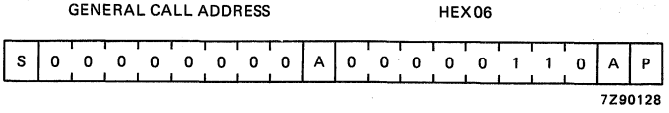


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0,3 to + 18 V
(pin 14)	V_{P2}	−0,3 to + 18 V
(pin 9)	V_{P3}	−0,3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0,3 to + 18 V
(pin 18)	V_{SCL}	−0,3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0,3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0,3 to V_{P1}* V
(pin 6)	V_{TI}	−0,3 to V_{P1}* V
(pin 8)	V_{TUN}	−0,3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0,3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0,3 to V_{P1}* V
(pin 16)	V_{OSC}	−0,3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

DEVELOPMENT DATA

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

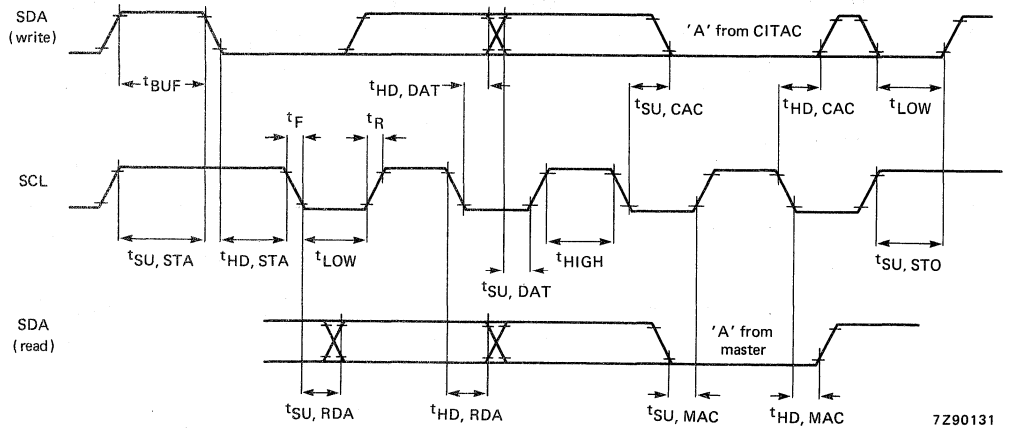


Fig. 8 I²C bus timing SAB3036.

COMPUTER INTERFACE FOR TUNING AND CONTROL (CITAC)

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue converters (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 13)	V_{P1}	typ.	12 V
(pin 19)	V_{P2}	typ.	13 V
(pin 14)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 13)	I_{P1}	typ.	30 mA
(pin 19)	I_{P2}	typ.	0,1 mA
(pin 14)	I_{P3}	typ.	0,6 mA
Total power dissipation	P_{tot}	typ.	380 mW
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT 101A).

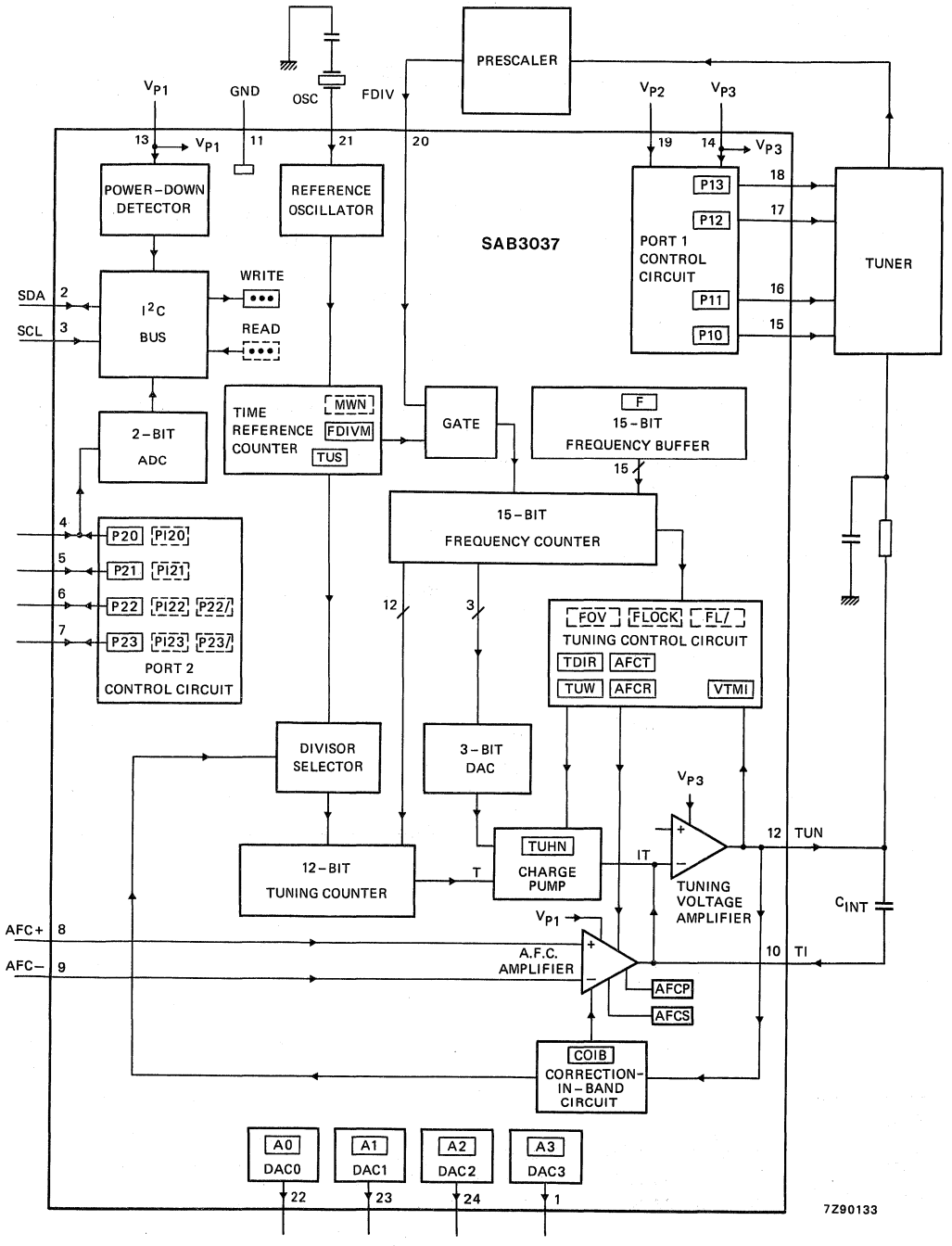


Fig. 1 Block diagram.

DEVELOPMENT DATA

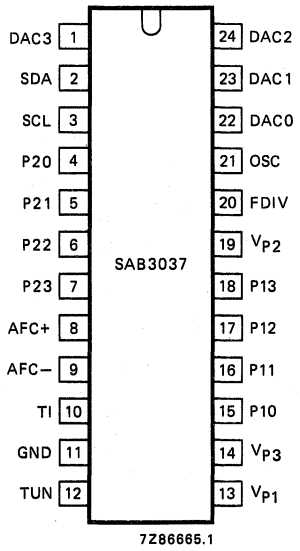


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC +	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6,4 ms (or 2,56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at $\Delta f = 50$ kHz equals 250 μA μs (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50$ kHz equals $2^6 \times 2^3 \times 250$ μA μs (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8,5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

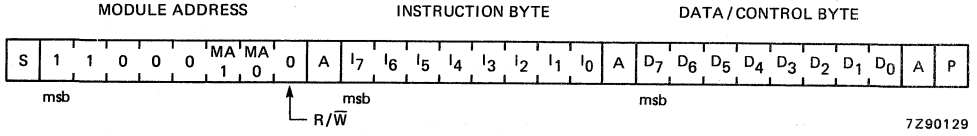


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8,5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0,25*	0,25*
0	0	1	0,5	0,5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

DEVELOPMENT DATA

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0,25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6,4*	5,12*
1	64	2,56	1,28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

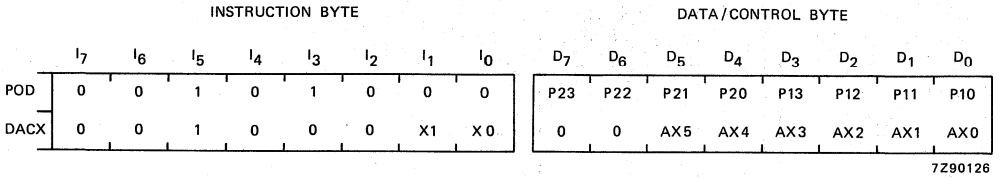


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

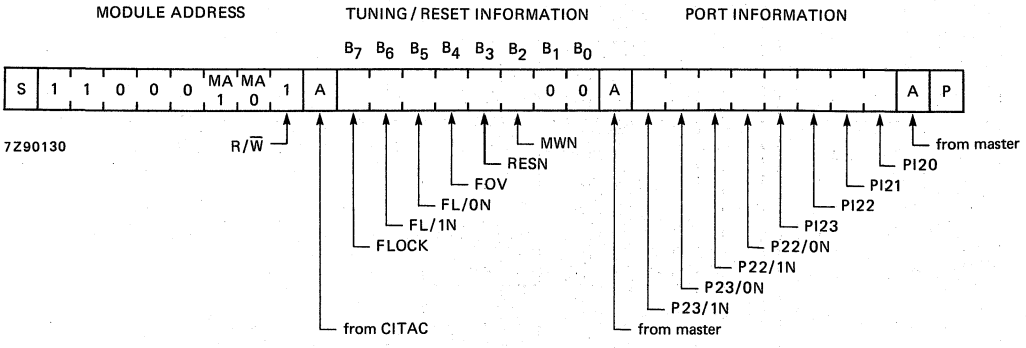


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1,28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

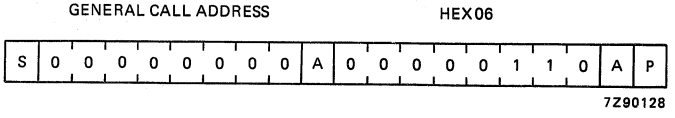


Fig. 7 Reset programming.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0,3 to +18	V
(pin 19)	V_{P2}	−0,3 to +18	V
(pin 14)	V_{P3}	−0,3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0,3 to +18	V
(pin 3)	V_{SCL}	−0,3 to +18	V
(pins 4 to 7)	V_{P2X}	−0,3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0,3 to V_{P1}*	V
(pin 10)	V_{TI}	−0,3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0,3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0,3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0,3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0,3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0,3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10,5	12	13,5	V
	V_{P2}	4,7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0,1	mA
	I_{P3}	0,2	0,6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0,2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0,3	–	1,5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2,5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 1,5$ mA	V_{TUN}	$V_{P3}-1,6$	–	$V_{P3}-0,4$	V
Minimum output voltage at $I_{load} = \pm 1,5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2,5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0,4	1	1,7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1,7	3,5	5,1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0,6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0,4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0,1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14,5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11,5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0,1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0,5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7,5	–	9,5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0,3	–	16	V
0 1	V_{VA01}	−0,3	–	0,8	V
1 0	V_{VA10}	2,5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0,3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I^2C BUS TIMING (Fig. 8)

I^2C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1,5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0,3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I^2C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

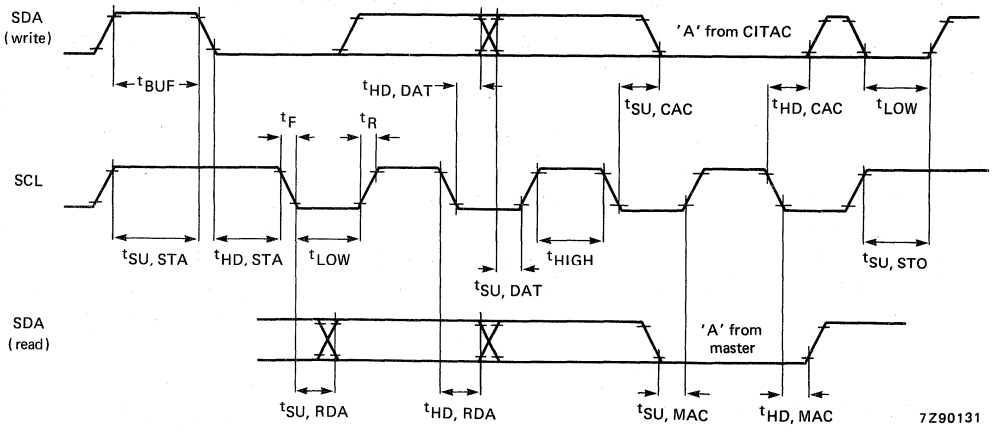


Fig. 8 I^2C bus timing SAB3037.

SENSITIVE 1 GHz DIVIDE-BY-64/DIVIDE-BY-256 SWITCHABLE PRESCALER

GENERAL DESCRIPTION

The SAB6456/SAB6456T is a prescaler for UHF/VHF tuners. It can be switched to divide-by-64 or divide-by-256 by the mode-control (MC) pin. The circuit has an input frequency range of 70 MHz to 1 GHz, has high input sensitivity and good harmonic suppression.

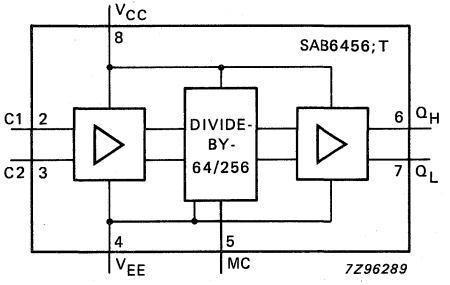


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	4,5	5,0	5,5	V
Supply current	pin 8	I_{CC}	–	21	–	mA
Input frequency range	pins 2 and 3	f_i	70	–	1000	MHz
Sensitivity to input voltage (r.m.s. value)		$V_{i(rms)}$	–	–	10	mV
Output voltage (peak-to-peak value)	pins 6 and 7	$V_{o(p-p)}$	–	1	–	V
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINES

SAB6456 : 8-lead DIL; plastic (SOT97).
SAB6456T: 8-lead mini-pack (SO8; SOT96A).

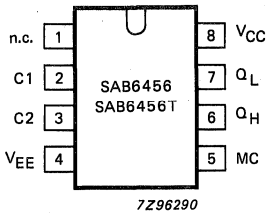


Fig. 2 Pinning diagram.

PINNING

1.	n.c.	not connected
2.	C1	differential inputs
3.	C2	
4.	V_{EE}	ground (0 V)
5.	MC	mode control
6.	Q_H	complementary outputs
7.	Q_L	
8.	V_{CC}	positive supply voltage

FUNCTIONAL DESCRIPTION

The circuit comprises an input amplifier, a divider stage with selectable division ratio and an output stage.

The input amplifier is driven by a sinusoidal signal from the local oscillator of a television tuner. The inputs (C1, C2) are differential and are biased internally to permit capacitive coupling. When driven asymmetrically the unused input should be connected to ground via a capacitor.

The mode-control (MC) input to the divider stage is intended for static control of the division ratio, selection is made as follows:

divide-by-64 : MC pin open-circuit

divide-by-256: MC pin connected to ground

The divider stage may oscillate during no-signal conditions but this oscillation is suppressed when input signals are received.

Two complementary signals (Q_H, Q_L) are provided by the output differential amplifier stage. The voltage-edges of the output signals are slowed internally to reduce harmonics in the television intermediate frequency band.

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection according to specification MIL-883C, class B.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC-134)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 8 to pin 4	V_{CC}	–	–	7,0	V
Input voltage		V_i	–	–	V_{CC}	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Junction temperature		T_j	–	–	+150	°C

THERMAL RESISTANCE

From junction to ambient

8-lead DIL; plastic (SOT-97A) $R_{th\ j\text{-}a}$ 120 K/W

8-lead mini-pack (SO-8; SOT-96A)

on printed circuit board $R_{th\ j\text{-}a}$ 260 K/W

on ceramic substrate $R_{th\ j\text{-}a}$ 170 K/W

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} −0,8	V
Supply current		I_{CC}	–	21	28	mA
Mode-control (MC)						
Input voltage LOW (divide-by-256)		V_{IL}	0	–	0,2	V
Input current LOW		$-I_L$	–	25	60	μA
Input voltage HIGH (divide-by-64)	pin 5 open-circuit	V_{IH}	1,4	–	3,0	V

A.C. CHARACTERISTICS

V_{CC} = 4,5 to 5,5 V; V_{EE} = 0 V; T_{amb} = 0 to +80 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity to input voltage (r.m.s. value)	50 Ω system					
	f_i = 70 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 150 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 300 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 500 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 900 MHz	$V_{i(rms)}$	–	–	10	mV
	f_i = 1000 MHz	$V_{i(rms)}$	–	–	10	mV
Input overload voltage (r.m.s. value)	50 Ω system; f_i = 70 MHz to 1000 MHz	V_i	300	–	–	mV
Input parallel resistance	f_i = 70 MHz	R_i	–	560	–	Ω
	f_i = 1000 MHz	R_i	–	30	–	Ω
Input capacitance	f_i = 70 MHz	C_i	–	5	–	pF
	f_i = 1000 MHz	C_i	–	1,5	–	pF
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC} –0,8	V
Output voltage swing (peak-to-peak value)	f_i = 70 MHz	$V_{o(p\text{-}p)}$	0,8	1,0	1,2	V
	f_i = 1000 MHz; R_L = 820 Ω; C_L = 60 pF	$V_{o(p\text{-}p)}$	0,17	–	–	V
Attenuation of third harmonic at output	f_i = 800 MHz; R_L = 820 Ω; C_L = 60 pF		–15	–23	–	dB
Output unbalance	see Fig. 3	ΔV_o	–	–	0,1	V
Output resistance		R_o	–	500	–	Ω

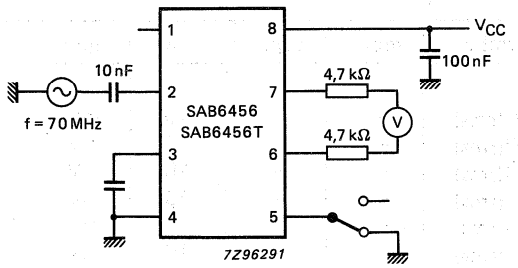


Fig. 3 Test circuit for output unbalance measurement.

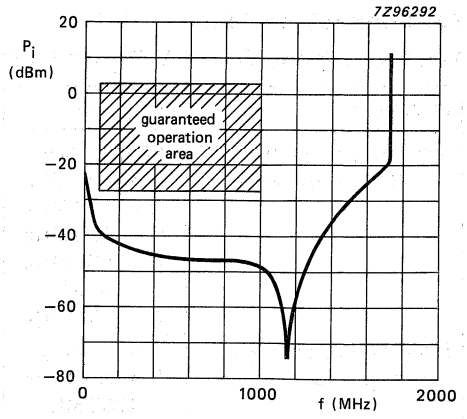


Fig. 4 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

DEVELOPMENT DATA

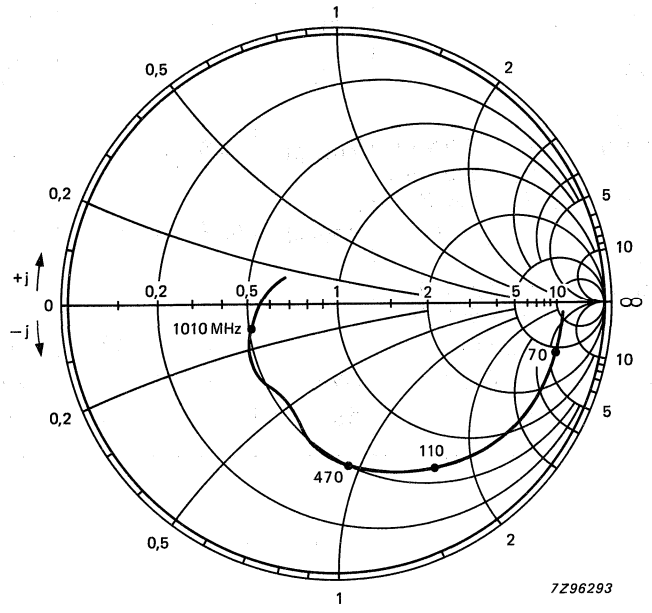


Fig. 5 Smith chart of typical input impedance: $V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

SENSITIVE 2.6 GHz DIVIDE-BY-2 PRESCALER

GENERAL DESCRIPTION

The SAB8726 is a prescaler for satellite television applications. It has an input frequency range of 1 GHz to 2.6 GHz with high input sensitivity.

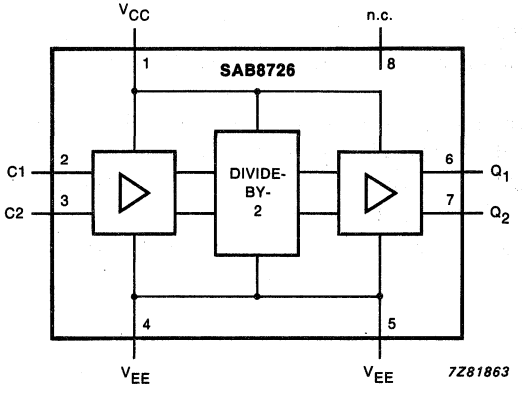


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 1 to pins 4, 5	V_{CC}	4.5	5.0	5.5	V
Supply current	pin 1	I_{CC}	–	35	–	mA
Input frequency range	pins 2 and 3	f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)		$V_{i(rms)}$	–	–	70	dBm/mV
Output voltage (RMS value)	pins 6 and 7	$V_{o(rms)}$	–	90	–	dBm/mV
Operating ambient temperature range		T_{amb}	0	–	80	°C

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

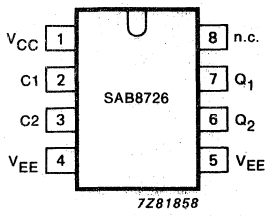


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply voltage
2	C1	differential inputs
3	C2	
4	V_{EE}	ground (0 V)
5	V_{EE}	ground (0 V)
6	Q_1	complementary outputs
7	Q_2	
8	n.c.	not connected

FUNCTIONAL DESCRIPTION

This IC is designed to be driven by a sinusoidal 1 GHz to 2.6 GHz signal from the local-oscillator of a satellite TV tuner.

The inputs (C1, C2) are differential and are internally biased to permit capacitive coupling (Fig. 5a). When driven asymmetrically the unused input should be connected to ground via a capacitor (Fig. 5b).

The divider stage will oscillate without an input signal but this oscillation will be suppressed when an input signal within the specified range is applied.

Two complementary signals (Q_1, Q_2) are provided by the output differantial amplifier stage (Fig. 5c).

For asymmetrical output, the unused output should be connected to ground via a 50 Ω resistor and a capacitor (Fig. 5d).

ELECTROSTATIC DISCHARGE PROTECTION

Inputs and outputs have electrostatic discharge protection in accordance with specification MIL-STD-883C, class A.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (DC)	V_{CC}	–	7.0	V
Input voltage	V_i	0	V_{CC}	V
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 80	°C
Junction temperature	T_j	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 120 K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{CC} = 5 V ± 10%; V_{EE} = 0 V; T_{amb} = 0 to 80 °C; test IC mounted in a test socket or on a printed circuit board; measurements taken after thermal equilibrium is established; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply current		I_{CC}	–	35	45	mA
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}−0.4	V

AC CHARACTERISTICS

V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 80 °C; f_{in} = 1 to 2.6 GHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Input						
Input frequency range		f_i	1	–	2.6	GHz
Input sensitivity						
Input voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	–	–	–10/70	dBm/mV
Input overload voltage (RMS value)	50 Ω system					
	f_i = 1 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
	f_i = 2.6 GHz	$V_{i(rms)}$	7/500	–	–	dBm/mV
Output						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW		V_{OL}	–	–	V_{CC}–0.4	V
Output voltage level	V_i = 0 dBm; f_i = 2 GHz; R_L = 50 Ω	V_o	–	–8/90	–	dBm/mV
Output resistance		R_o	–	50	–	Ω

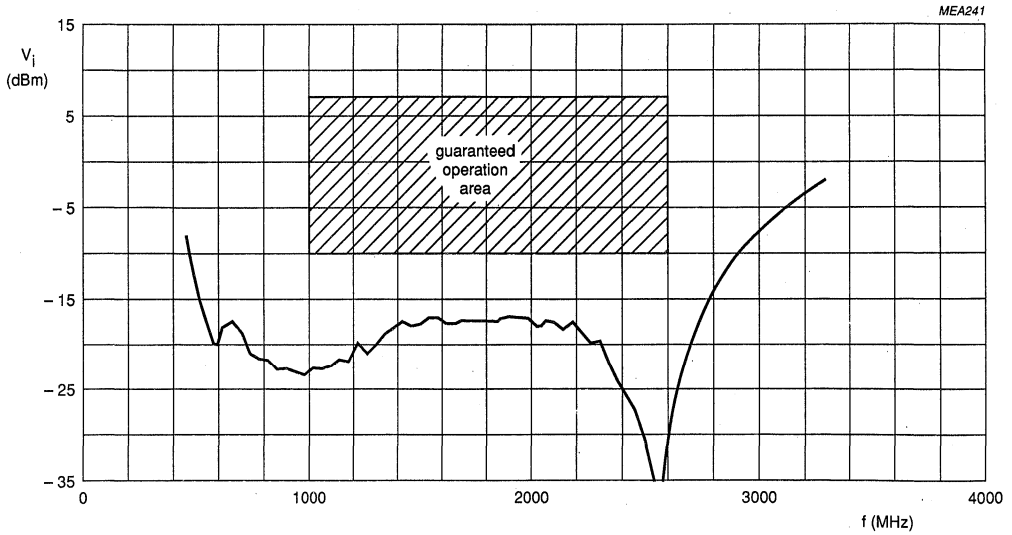


Fig.3 Typical input sensitivity curve: V_{CC} = 5 V; T_{amb} = 25 °C.

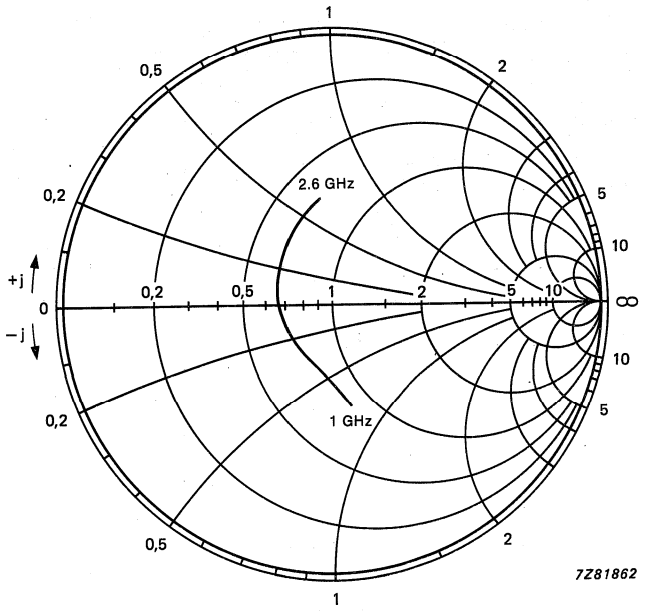
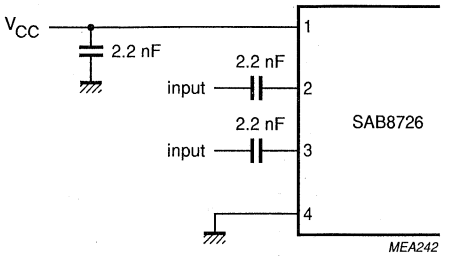
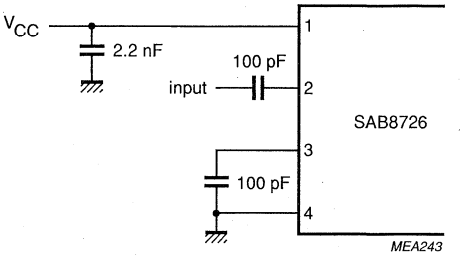


Fig. 4 Smith chart of typical input impedance: input level = −10 dBm; V_{CC} = 5 V; reference value = 50 Ω.

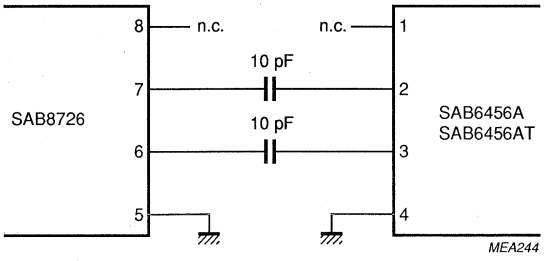
APPLICATION INFORMATION



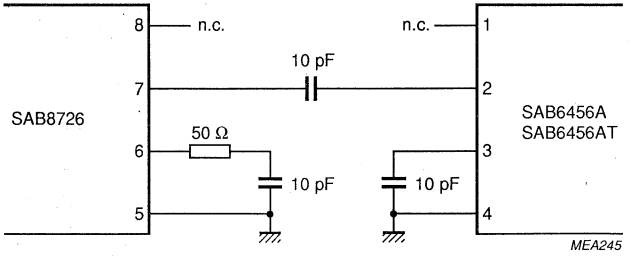
(a) Symmetrical input.



(b) Asymmetrical input.



(c) Symmetrical output.



(d) Asymmetrical output.

Fig. 5 Pin configurations for symmetrical/asymmetrical input and output.

Note to Fig. 5

To minimize possible harmonics the symmetrical output is preferred.

UNIVERSAL DAC (UDAC)

GENERAL DESCRIPTION

The SAD1009 is intended as a peripheral to a microcontroller-based servo system in video cassette recorders. The device relieves the microcontroller of some of the real time functions. These functions include; generation of programmable pulse width signals (duty factor etc.) and accurate measurement of time period signals (tacho signal etc.). The SAD1009 has nine programmable output ports. All functions of the UDAC are programmable. Commands and data from the microcontroller are loaded via a bidirectional bus using a 16-bit format. Data from the time period measurement is transferred to the microcontroller via the same bidirectional bus, also using a 16-bit format. The clock signal for this device is provided by the quartz oscillator of the microcontroller.

Features

- Generation of programmable pulse width signals
- Measurement of time period signals
- All functions are programmable

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Inputs						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
Outputs						
Output voltage						
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD} −0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA

PACKAGE OUTLINES

SAD1009P: 24-lead DIL; plastic (SOT101A).
SAD1009T: 24-lead mini-pack; plastic (SO24; SOT137A).

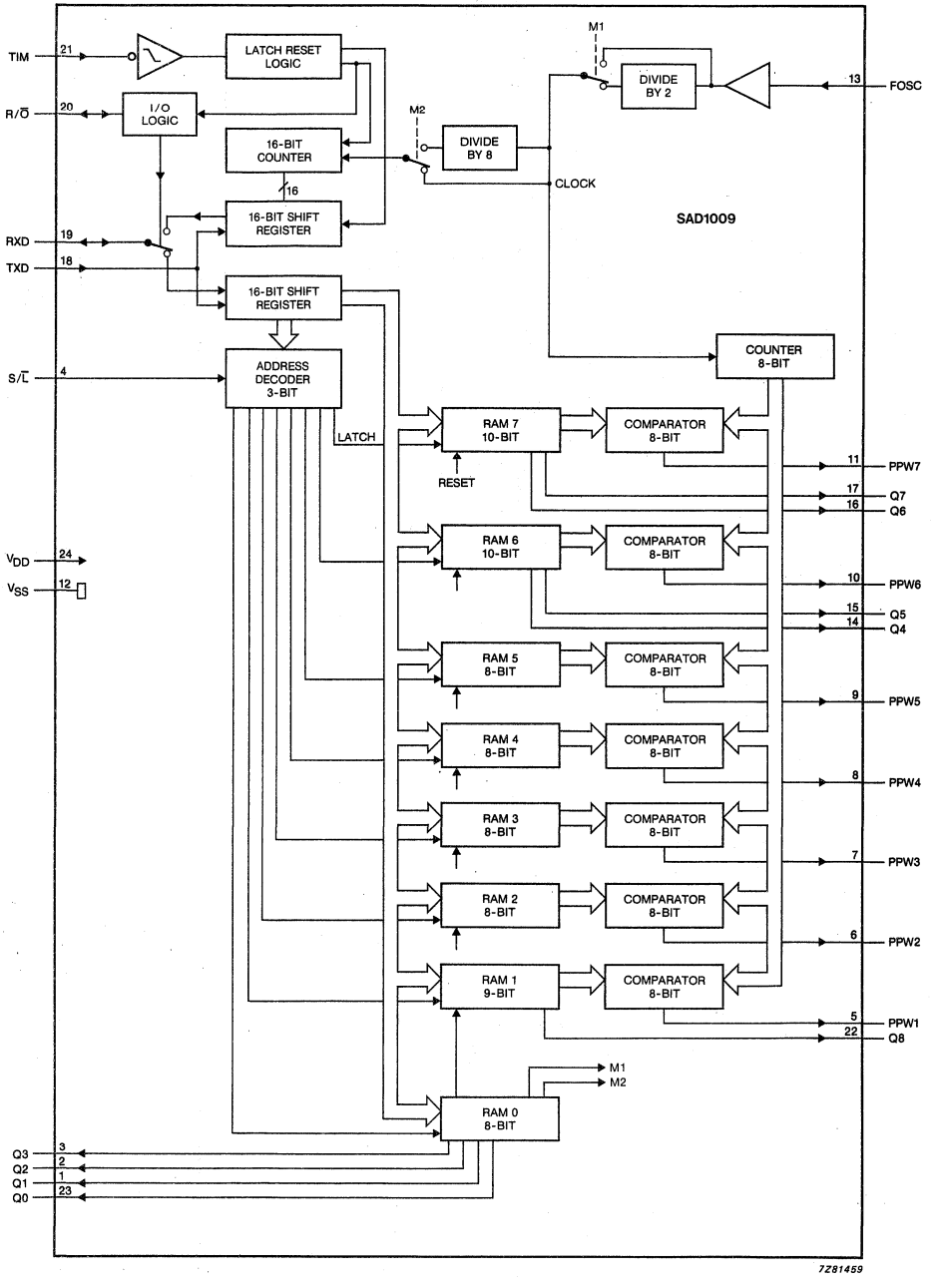


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

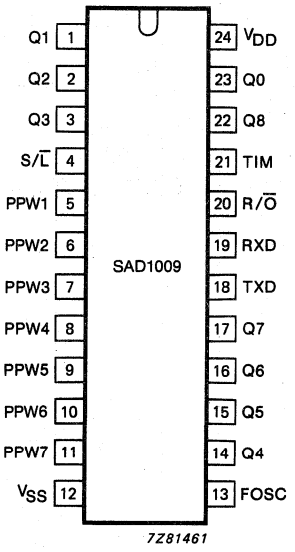


Fig. 2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (+5 V)
V_{SS}	ground (0 V)

Inputs

S/$\overline{L}$	shift/$\overline{\text{latch}}$ input
FOSC	oscillator input
TXD	serial clock

Special inputs

TIM	timer input

Outputs

Q0 to Q8	programmable output ports
PPW1 to PPW7	programmable pulse width outputs

Input/outputs

RXD	serial data
R/$\overline{O}$	handshake

FUNCTIONAL DESCRIPTION

Loading data

All commands and data are loaded into the SAD1009 via the bidirectional bus (TXD, RXD). The bidirectional bus is compatible with the serial interface of the '8051' microcontroller, using mode 0.

A 16-bit word is used to program a function of the UDAC. The first 3-bits received from the RAM constitute the address and the remaining 13-bits are data (LSB first, MSB last). None of the functions require all 13-bits of data, therefore, 16-bit words contain a number of immaterial bits (x). The programming format is shown in Table 1.

To shift a program word into the input buffer of the UDAC the S/$\overline{L}$ line (shift/latch not) must be HIGH. The contents of the input buffer are transferred to the appropriate RAM on the HIGH-to-LOW transition of the S/$\overline{L}$ signal. When S/$\overline{L}$ is LOW the input buffer is disabled and cannot accept new incoming information. Fig. 3 illustrates the program reception cycle.

Table 1 Programming format

bit	status	PPW1	PPW2	PPW3	PPW4	PPW5	PPW6	PPW7
1	L	H	L	H	L	H	L	H
2	L	L	H	H	L	L	H	H
3	L	L	L	L	H	H	H	H
4	$\overline{\text{RESET}}$	Q8	X	X	X	X	Q4	Q6
5	X	X	X	X	X	X	Q5	Q7
6	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X
8	X	X	X	X	X	X	X	X
9	Q0	D8	D8	D8	D8	D8	D8	D8
10	Q1	D7	D7	D7	D7	D7	D7	D7
11	Q2	D6	D6	D6	D6	D6	D6	D6
12	Q3	D5	D5	D5	D5	D5	D5	D5
13	X	D4	D4	D4	D4	D4	D4	D4
14	X	D3	D3	D3	D3	D3	D3	D3
15	M1	D2	D2	D2	D2	D2	D2	D2
16	M2	D1	D1	D1	D1	D1	D1	D1

Where:

X : don't care
D1 to D8: data for programming pulse width, D1 = MSB and D8 = LSB

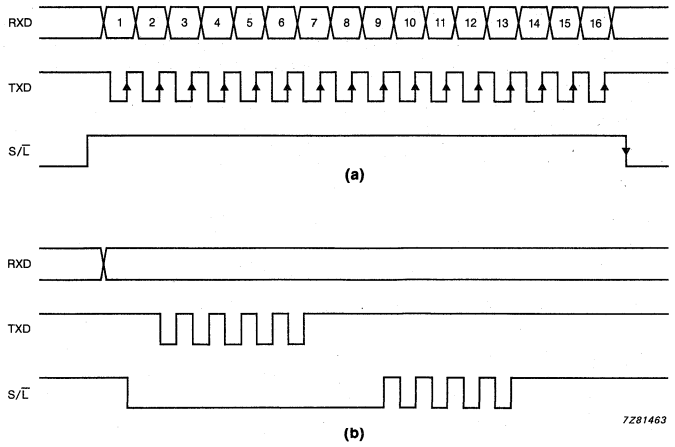


Fig. 3 Program reception cycle: a) normal reception cycle; b) no information is loaded into the input buffer, the RAMs contents remain unchanged.

DEVELOPMENT DATA

Pulse width modulated outputs

The UDAC has seven pulse width modulated outputs (PPW1 to PPW7). The output PPW1 is slightly different to outputs PPW2 to PPW7, the difference is explained below. Each output produces a pulse width modulated signal with a duty factor programmable in steps of 1/256 and has a repetition frequency of approximately 23 kHz. These pseudo analogue signals are used to control the capstan and reel drives. Motor control can be performed in the following ways:

- convert the pulse width modulated signal into an analogue signal using filtering and analogue power amplification
- by feeding the pulse width modulated signal to the motor via a power switch and a switch mode filter

To conserve power use the second method for control of the capstain and reel motors. For the scanner control two outputs are available, so that by weighted addition a higher resolution can be achieved.

PPW1 is also an 8-bit programmable output, with a repetition frequency of 23 kHz. The difference is the low frequency contents of the signal are reduced by changing the distribution of the HIGH and LOW level portions. This redistribution means that a filter with two poles; each at 43 μs, is sufficient to reduce the peak-to-peak ripple to less than 1 LSB. This output is for use in applications where long filter delays are not tolerated.

Clock frequency

The clock signal of the UDAC is derived from the quartz oscillator of the microcontroller. The clock frequency should not exceed 6 MHz. The device also contains a programmable 'divide by two' circuit which allows these frequencies to be doubled, thus 6 MHz or 12 MHz microcontrollers can be used. The FOSC signal can be divided by two using bit M1 of RAM 0 (see Table 2).

Table 2 UDAC adjustment

bit M1	quartz frequency (MHz)
L	12
H	6

Programmable output ports

A total of nine output ports can be programmed to supply a HIGH or LOW level signal. Four of these outputs (Q4 to Q7) are intended to supply information about the breaking and direction of the capstan and reel motors, therefore these output ports must be programmed at the same time as the pulse widths of PPW6 and PPW7. Output port Q8 is programmed at the same time as PPW1. The other four output ports (Q0 to Q3) are programmed by RAM 0.

Measurement of the time period

To facilitate accurate measurement of the time period (falling edge to falling edge) of a signal applied to TIM, the UDAC contains a 16-bit counter and a buffer to store the contents of the previous counter measurement. The counter operates at a frequency of $f_{CLOCK}/2$ or $f_{CLOCK}/16$, the counter can be programmed using bit M2 of RAM 0. This timer can record periods of up to 21,8 ms and 175 ms respectively (see Table 3). When the time period is too long and the timer overflows, the microcontroller is loaded with a hex 'FFFF' when it reads the time period after the next pulse.

Table 3 Counter frequency

M2	division ratio	time period (max.)	frequency	resolution
L	2	21,8 ms	46 Hz	333 ns
H	6	175 ms	5,7 Hz	2,67 μs

Data from the timer can be transferred to the microcontroller via a bidirectional bus when the handshaking signal pin R/$\overline{O}$ is pulled LOW by the microcontroller. The LSB is transferred first and the MSB last. After the data has been transferred pin R/$\overline{O}$ remains in a LOW state (pulled down by the UDAC) until a new measurement of the time period is concluded. Note that each measurement of a time period can only be read once. After the next input pulse the 'data ready' state is signalled to the microcontroller by releasing the R/$\overline{O}$ pin, so that the microcontroller reads a HIGH level on this pin.

Note

During the 'data not ready' state the R/$\overline{O}$ is in a low impedance state and during the 'data ready' state the R/$\overline{O}$ is in a high impedance state (= HIGH). To speed up the transition from LOW-to-HIGH, the high impedance state is preceded by a short period of low impedance HIGH state.

Reset

The device can be reset by software by loading a LOW into the $\overline{RESET}$ bit of RAM 0. The effect of this reset is as follows:

- RAM 0; not influenced
- RAM 1; duty factor = 50%, Q8 = LOW
- RAM 2 to 5; duty factor = 50%
- RAM 6 to 7; duty factor = 0 and Q4 to Q7 = LOW

The reset is de-activated automatically on the next LOW-to-HIGH transition of S/$\overline{L}$. This allows new program information to be loaded and transferred to any RAM without having finished the reset. Due to RAM 0 not being influenced by the reset, the data required after the reset can be loaded along with the reset command.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–	7	V
Input voltage range	note 1	V_I	−0,5	V_{DD} + 0,5	V
Input voltage at S/$\overline{L}$		$V_{4\text{-}12}$	−0,5	V_{DD} + 2,0	V
D.C. current into any input		$\pm I_I$	–	10	mA
D.C. current from any output		$\pm I_O$	–	10	mA
D.C. current into V_{DD}		$\pm I_I$	–	25	mA
D.C. current into V_{SS}		$\pm I_I$	–	25	mA
Total power dissipation	note 2	P_{tot}	–	200	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−20	+70	°C

Notes to ratings

1. Input voltage should not exceed 7 V unless otherwise specified.
2. Diminishes by 5 mW/K from 60 °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 4,75 to 5,25 V; T_{amb} = −20 to 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4,75	5,0	5,25	V
Supply current range	$V_O = V_{DD}$, I_O = 0 mA on all outputs; $V_I = V_{SS}$ on all inputs	I_{DD}	–	100	–	μA
TXD, RXD, S/$\overline{L}$, R/$\overline{O}$						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current	note 1	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF
RXD, R/$\overline{O}$, Q0 to Q7						
Output voltage	note 2					
LOW	I_{OL} = 1,6 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = −1,0 mA	V_{OH}	V_{DD}−0,4	–	–	V
Output sink current		I_O	–	–	1,6	mA
Output source current		$-I_O$	–	–	1,0	mA
FOSC						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,4	–	–	V
Input leakage current		$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	–	7,5	pF

D.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
RXD	used as input					
Input leakage current		$\pm I_I$	–	–	10	μA
TIM						
Input voltage						
LOW		V_{IL}	–	–	$0{,}3 \times V_{DD}$	V
LOW	V_{DD} = 5 V at 20 °C	V_{IL}	–	1,8	–	V
HIGH		V_{IH}	$0{,}7 \times V_{DD}$	–	–	V
HIGH	V_{DD} = 5 V at 20 °C	V_{IH}	–	2,9	–	V
Hysteressis	used as input	V_{hys}	–	730	–	mV
R/$\overline{O}$	used as input					
Output resistance		R_O	500	–	1000	Ω
Input leakage current		$\pm I_I$	–	–	10	μA
R/$\overline{O}$	used as output; open drain output; note 3; see Fig. 7					
Output voltage						
LOW	I_{OL} = 0,4 mA	V_{OL}	–	–	0,8	V
HIGH	I_{OH} = –0,4 mA	V_{OH}	$V_{DD}-0{,}8$	–	–	V
PPW1 to PPW7						
Output voltage						
LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
HIGH	I_{OH} = –4 mA	V_{OH}	$V_{DD}-0{,}4$	–	–	V
Output sink current		I_O	–	–	4	mA
Output source current		$-I_O$	–	–	4	mA

Notes to the d.c. characteristics

1. This value applies to TXD and S/$\overline{L}$, the input leakage current for RXD and R/$\overline{O}$ is shown above.
2. This value applies to RXD and Q0 to Q7, the output voltage for R/$\overline{O}$ is shown above.
3. After a LOW-to-HIGH transition of the R/$\overline{O}$ output, the port is held HIGH for approximately one clock cycle. This low impedance HIGH period is followed by the high impedance OFF-state.

DEVELOPMENT DATA

A.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
RXD, R/$\overline{O}$, Q0 to Q7						
Output transition time	C_L = 50 pF					
LOW-to-HIGH		t_{TLH}	–	–	30	ns
HIGH-to-LOW		t_{THL}	–	–	30	ns
FOSC						
Maximum pulse frequency	M1 = L	f_{max}	–	–	12	MHz
	M1 = H	f_{max}	–	–	6	MHz
Minimum pulse width						
LOW		t_{WL}	20	–	–	ns
HIGH		t_{WH}	20	–	–	ns
TXD						
Pulse frequency		f_{max}	–	–	6	MHz
Pulse width						
LOW		t_{WL}	50	–	–	ns
HIGH		t_{WH}	50	–	–	ns
RXD	used as input; see Fig. 5					
Set-up time RXD to TXD		t_{SURXD}	50	–	–	ns
Hold time RXD to TXD		t_{HDRXD}	50	–	–	ns
RXD	used as output; see Fig. 6					
Propagation delay						
TXD to RXD		t_{PRXD}	–	–	50	ns
R/$\overline{O}$ to RXD		$t_{PR/O}$	–	–	50	ns
S/$\overline{L}$	see Fig. 7					
Pulse width LOW						
Set-up time TXD to S/$\overline{L}$		t_{SUTXD}	50	–	–	ns
Hold time TXD to S/$\overline{L}$		t_{HDTXD}	50	–	–	ns
Propagation delay S/$\overline{L}$ to Q0 - Q7		t_p	–	–	50	ns
TIM						
Pulse width						
LOW	M2 = LOW	t_{WL}	700	–	–	ns
LOW	M2 = HIGH	t_{WL}	5,4	–	–	μs
HIGH		t_{WH}	100	–	–	ns

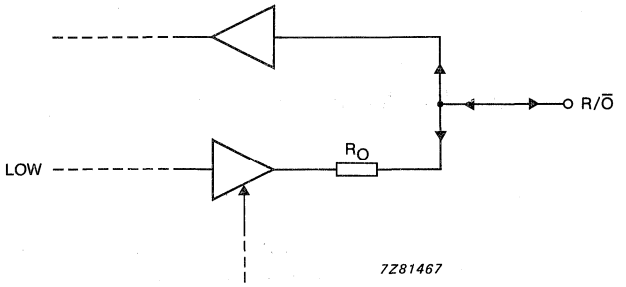


Fig. 4 Equivalent R/$\overline{O}$ output port.

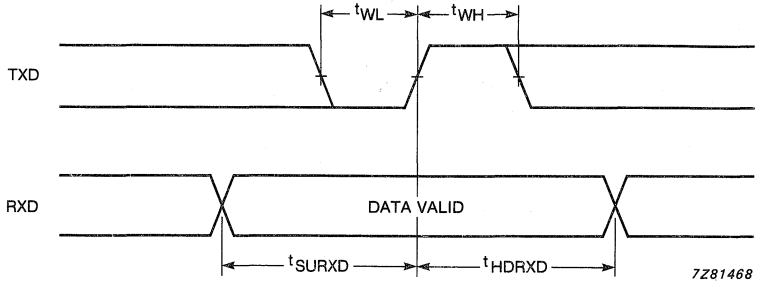


Fig. 5 RXD input waveform.

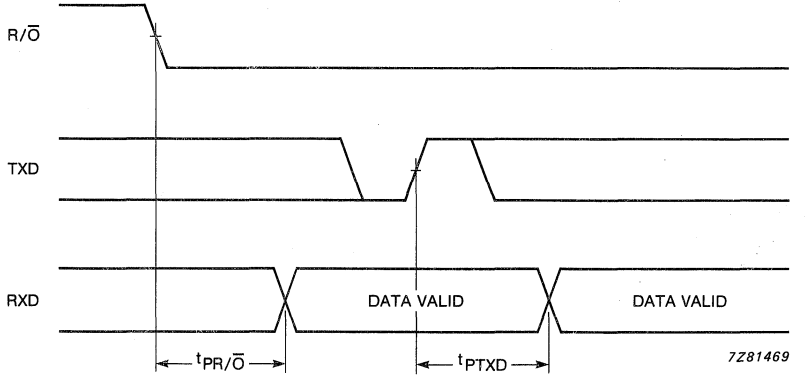


Fig. 6 RXD output waveform.

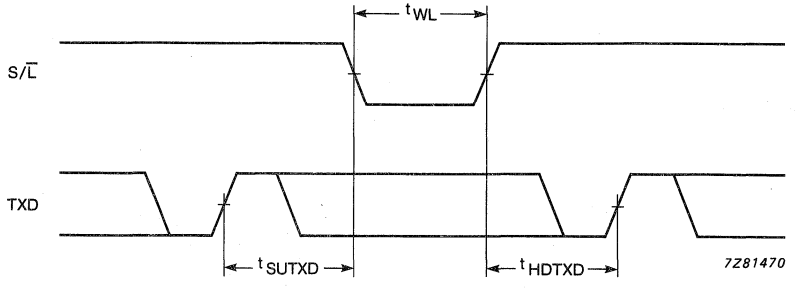


Fig. 7 S/$\overline{L}$ input waveform.

MULTI-NORM PULSE-PATTERN GENERATOR

GENERAL DESCRIPTION

The SAD1019 is part of a frame transfer image sensor camera system which uses the NXA series of frame transfer image sensors. The device provides the vertical transport pulses necessary, for the operation of the frame transfer image sensors and a start-stop signal for the horizontal clock generator. The drive pulses and clock signals for the SAD1019 are provided by the universal sync generator (SAA1043).

Features

- Vertical transport pulses for the image region and storage region of the image sensor during field blanking (ϕ_A and ϕ_B pulses)
- Colour separation and transport of one line of sensor information to the output register during line blanking (ϕ_B, TG and ϕ_C pulses)
- Other additional pulses required for the control and processing in the frame transfer image sensor camera

PACKAGE OUTLINES

SAD1019: 24-lead DIL; plastic (SOT101B).
SAD1019T: 24-lead mini-pack; plastic (SO24; SOT137A).

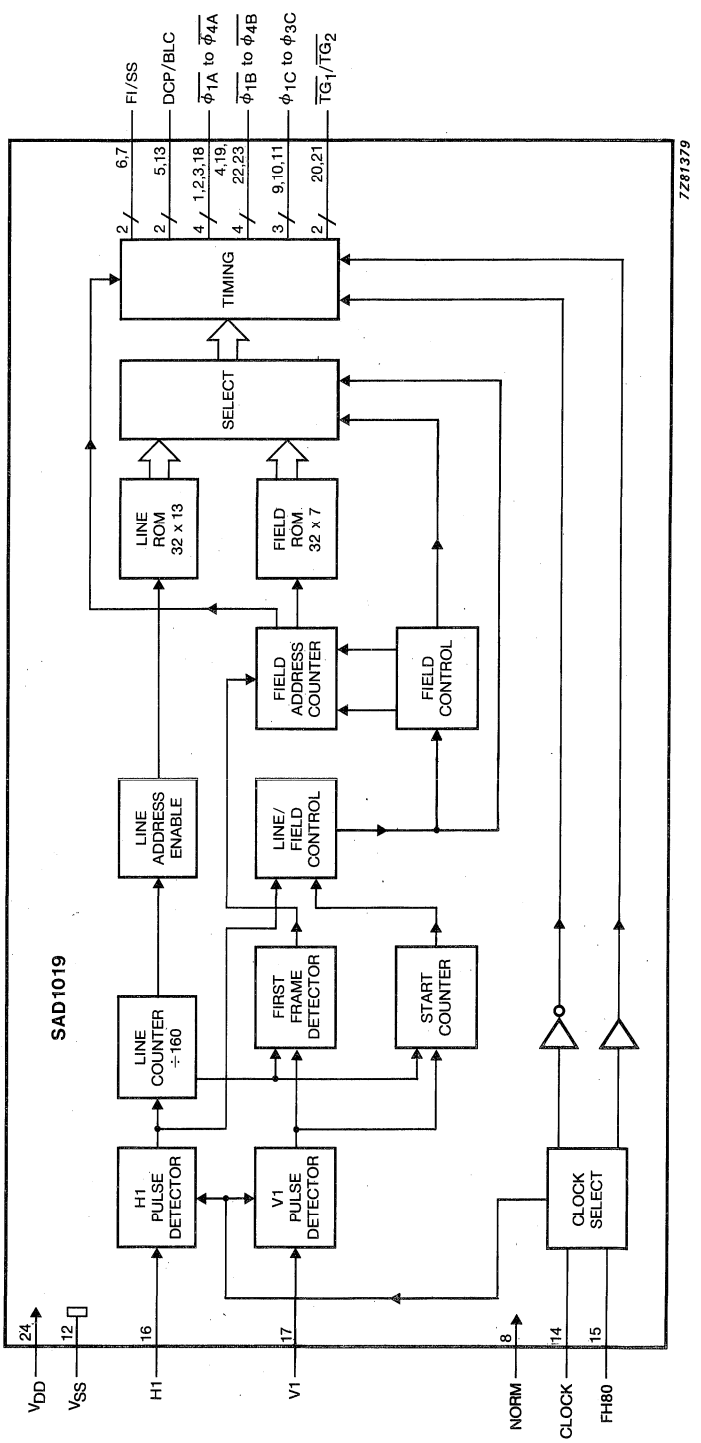


Fig.1 Block diagram.

PINNING

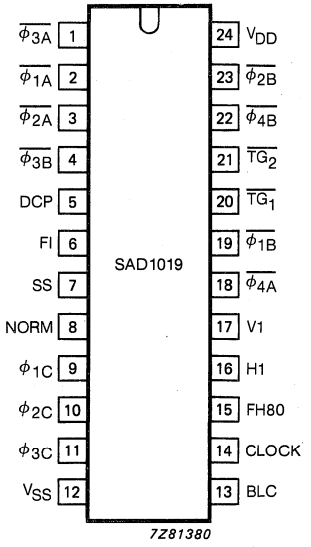


Fig.2 Pinning diagram.

DEVELOPMENT DATA

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (CMOS)

CLOCK	clock input from SAA1043, typ. 2.5 MHz (625 lines) or typ. 2.51748 MHz (525 lines). 5 MHz mode, typ. 5 MHz (625 lines) or 5.03496 MHz (525 lines)
FH80	clock input from SAA1043, typ. 1.25 MHz (625 lines) or 1.25874 MHz (525 lines)
H1	H1 input from SAA1043, typ. 15.625 kHz (625 lines) or typ. 15.734 kHz (525 lines)
V1	V1 input from SAA1043, typ. 50 Hz (625 lines) or 59.94 Hz (525 lines)
NORM	norm-selection input, 625 lines = LOW, 525 lines = HIGH

Outputs (CMOS push-pull)

$\overline{\phi 1A}$ to $\overline{\phi 4A}$	sensor image section control to drivers
$\overline{\phi 1B}$ to $\overline{\phi 4B}$	sensor storage section control to drivers
$\phi 1C$ to $\phi 3C$	low frequency outputs for transport pulses to pixel oscillator
DCP	DC clamp pulse
FI	frame identification
SS	start/stop for pixel generator
BLC	black-level clamping
$\overline{TG_1}$ and $\overline{TG_2}$	transfer gate control to drivers

FUNCTIONAL DESCRIPTION

625 line mode (NORM = LOW, see Figs 3 to 7)

One complete cycle of the multi-norm pulse-pattern generator (MNPPG) occurs after a command from the synchronization pulse generator (SYN). This cycle consists of 294 line cycles which are used to read out the sensor information followed by transport of the integrated information from the image area to the storage area of the sensor. Once this cycle has been completed the device enters into a 'wait' status period which lasts until the device receives a start command from the SYN.

The cycle is restarted with a V-pulse from the SYN. The falling edge of this pulse is detected in the MNPGG and results in a reset of the start counter as well as providing the field information (field 1/2). The start counter counts 11 lines and then the line cycle information is read from the line ROM. The start of the line cycle occurs at line 22 in frame 1 and line 335 in frame 2. The H1 pulse of the SYN controls the position of the line cycle with respect to the SYN pulses. The H1 pulse sets the correct value in the line counter of the MNPPG.

The control counter counts the number of line cycles and switches the line cycle to field cycle after 294 lines (in both fields), then the field cycle information is read from the field ROM. The control counter was reset before the switch over had taken place, it now counts the field cycles. The field cycle lasts for 294 cycles of the $\overline{\phi 4B}$ pulse and then the device enters the wait status period again.

The device will continue to operate in the manner described, until the overall system is switched off.

525 line mode (NORM = HIGH)

The basic operation is identical except for variations in the start points and number of transports (see Figs 8 to 12).

Operating modes

Synchronization generator (SAA1043)

The H1 pulse from the SAA1043, due to internal delays, is out of phase with the MNPPG clock signal. The following method is used to obtain the correct phase relationship between the H1 pulse and the MNPPG output. The H1 pulse and the FH80 are clocked into a flip-flop, at the output of the flip-flop the timing of the H1 and FH80 signals are in phase. The output of the flip-flop is sampled with that of the CLOCK, which is in phase with the FH80. In this way a reliable fixed phase relationship between SYN and MNPPG is obtained.

Other operating modes

- single 2.5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 2.5 MHz clock signal can be used.

  Connect the 2.5 MHz to the CLOCK and with delay circuitry (RC elements, 50 ns approx.) to FH80.
- single 5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 5 MHz clock signal can be used.

  Connect the 5 MHz to the CLOCK and connect FH80 to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0.5	+ 7.0	V
Supply current (pin 24)	I_{DD}	−	50	mA
Supply current (pin 12)	I_{SS}	−	50	mA
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	−	10	mA
Output current	$\pm I_O$	−	10	mA
Total power dissipation per package	P_{tot}	−	500	mW
Power dissipation per output	P_O	−	25	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

* V_{DD} + 0.5 V not to exceed 7.0 V.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current						
Supply current	on all outputs; I_O = 0 mA	I_{DD}	–	–	10	μA
Inputs H1, V1, NORM, CLOCK and FH80						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input voltage LOW	CMOS compatible	V_{IL}	–	–	$0.3V_{DD}$	V
Outputs						
Output voltage HIGH	all outputs except BLC; $-I_O$ = 0.8 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	all outputs except BLC; I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V
Black level clamping (BLC)						
Output voltage HIGH	$-I_O$ = 2.6 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V

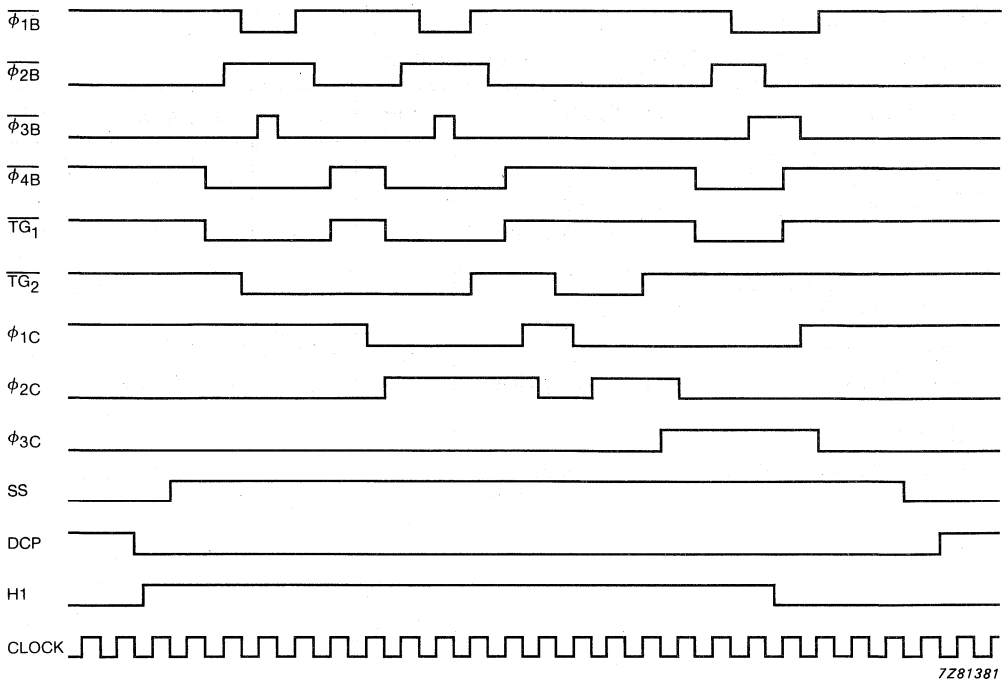
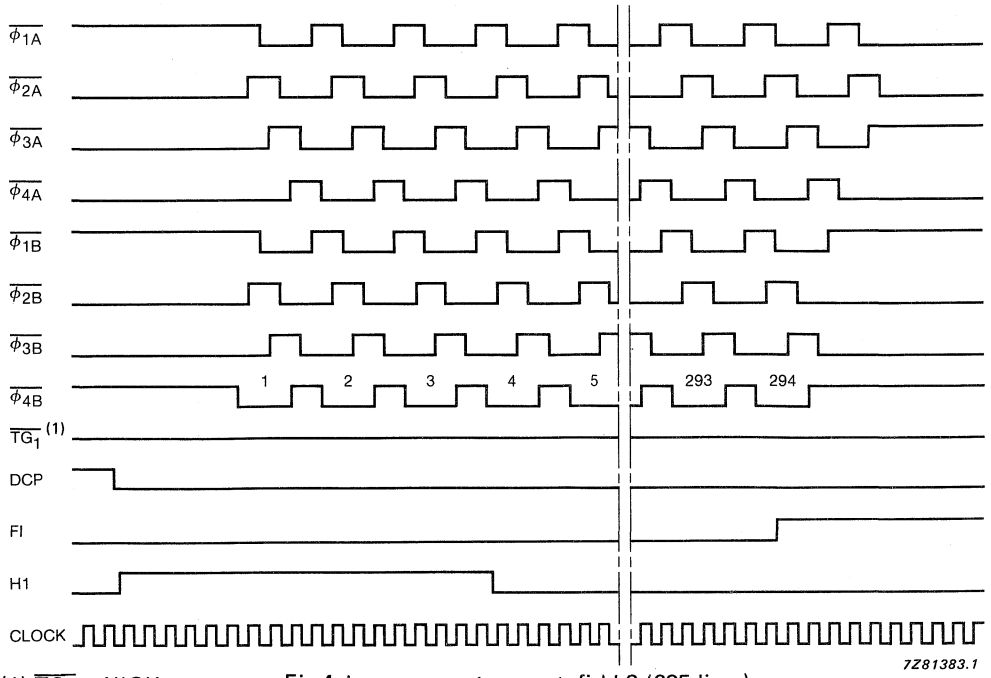
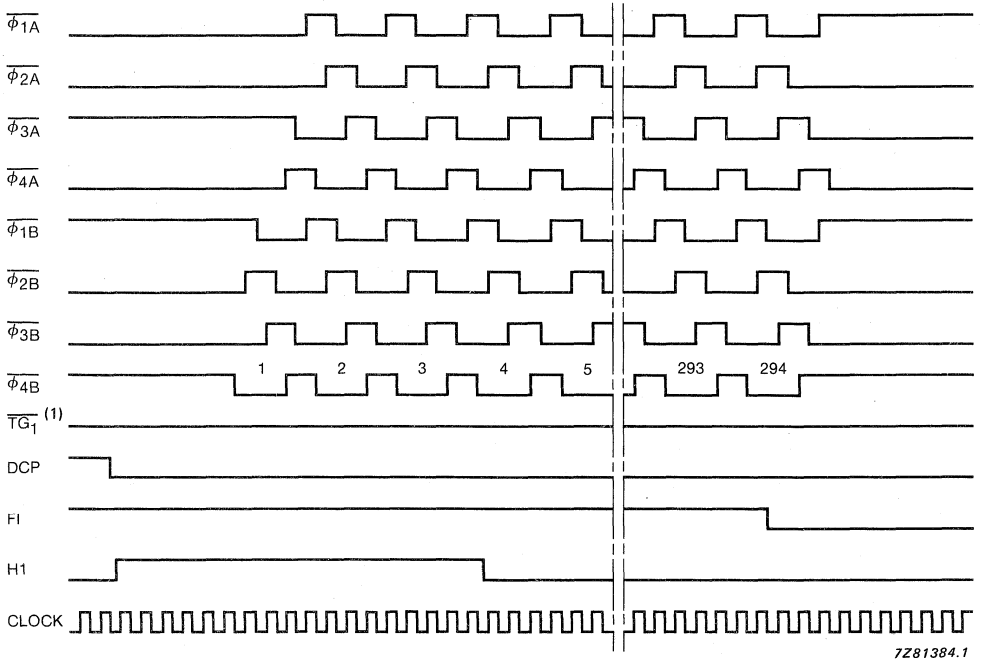


Fig.3 Line transport (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.4 Image sensor transport, field 2 (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.5 Image sensor transport, field 1 (625 lines).

DEVELOPMENT DATA

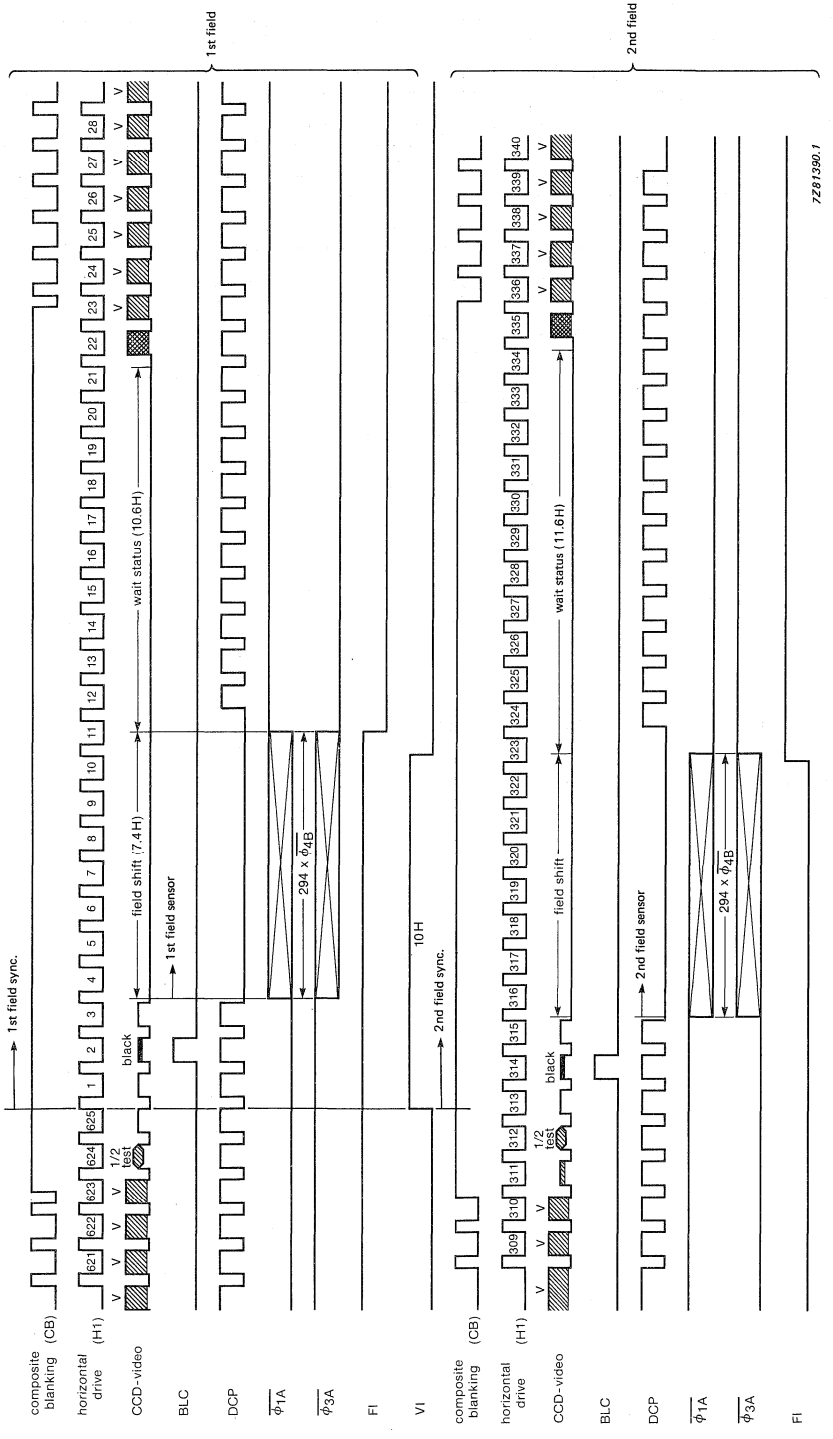


Fig.6 Pulse pattern during field blanking (625 lines).

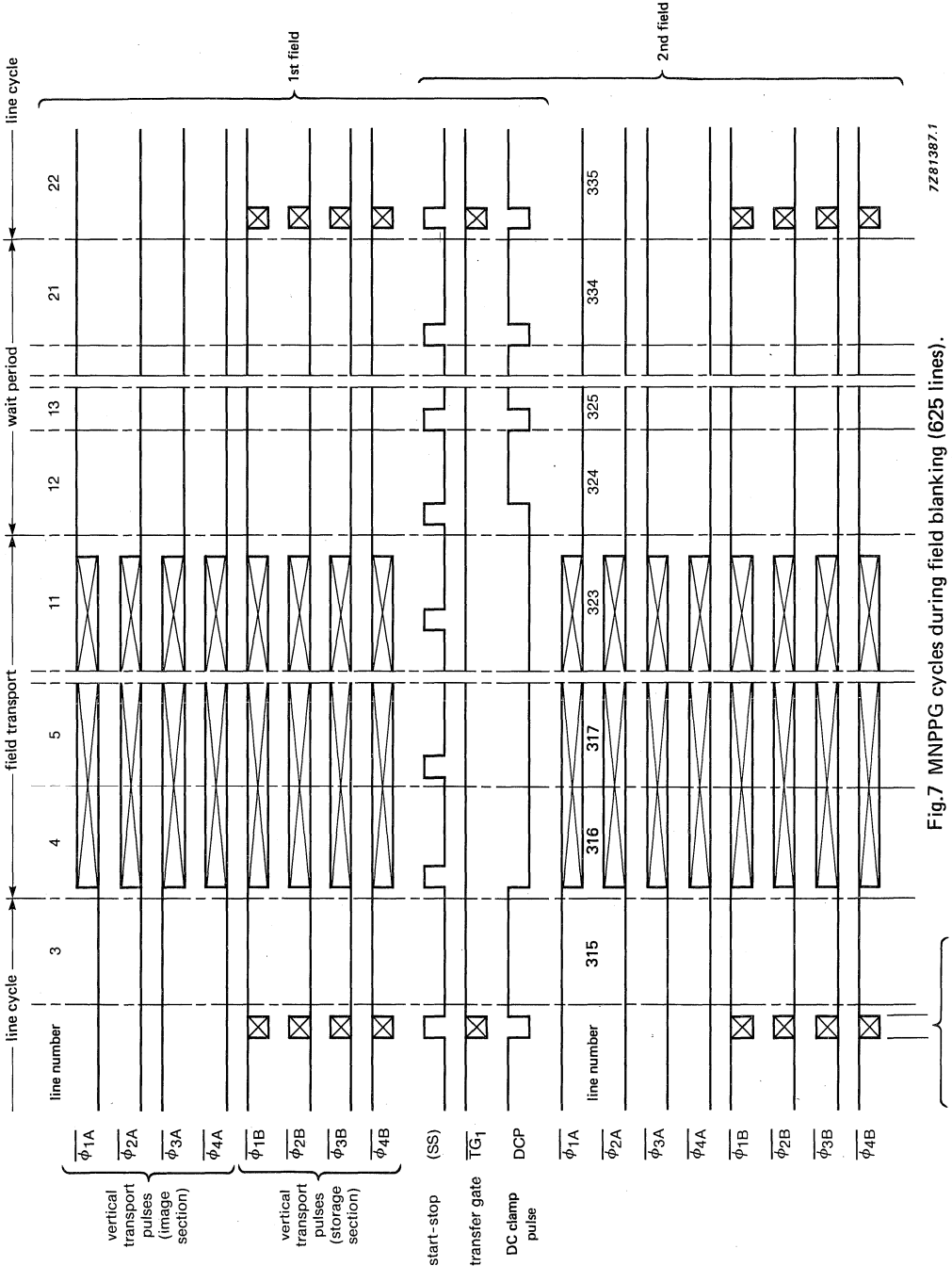


Fig.7 MNPPG cycles during field blanking (625 lines).

DEVELOPMENT DATA

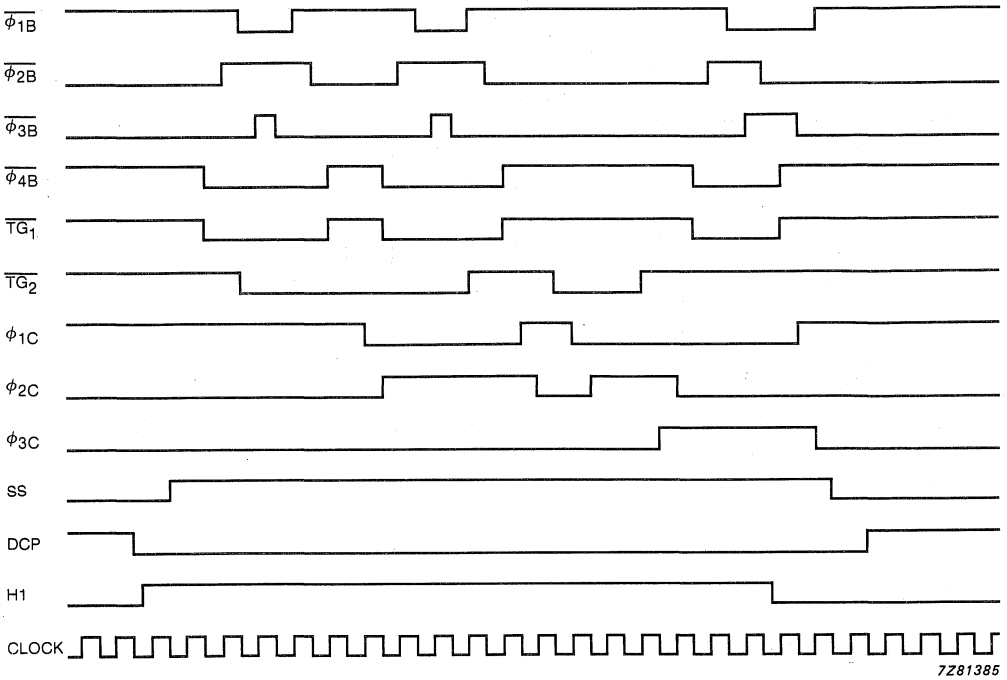
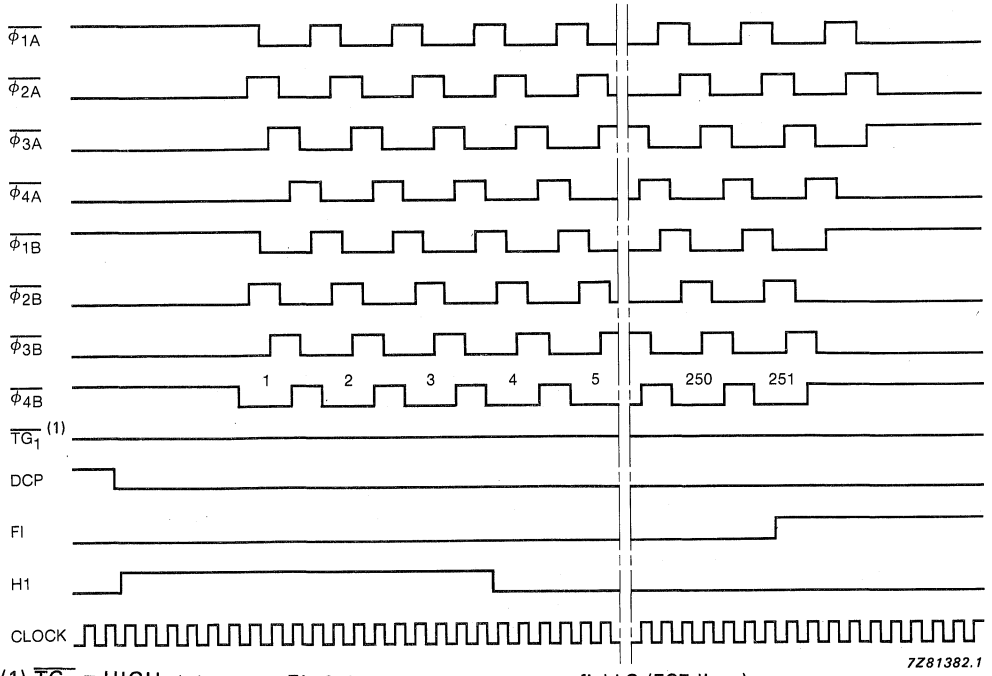
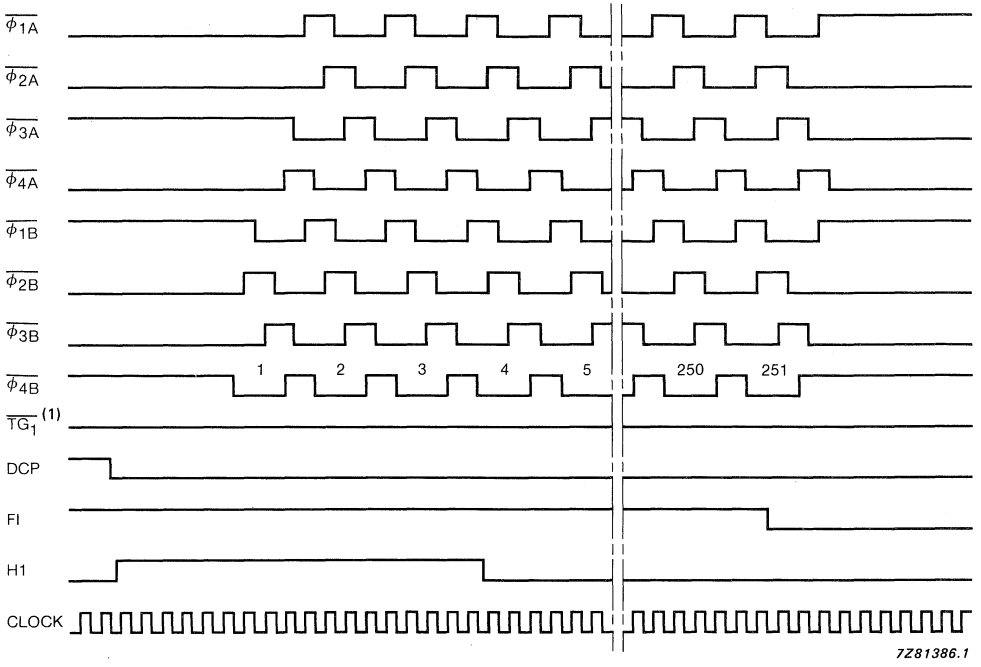


Fig.8 Line transport (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.9 Image sensor transport, field 2 (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.10 Image sensor transport, field 1 (525 lines).

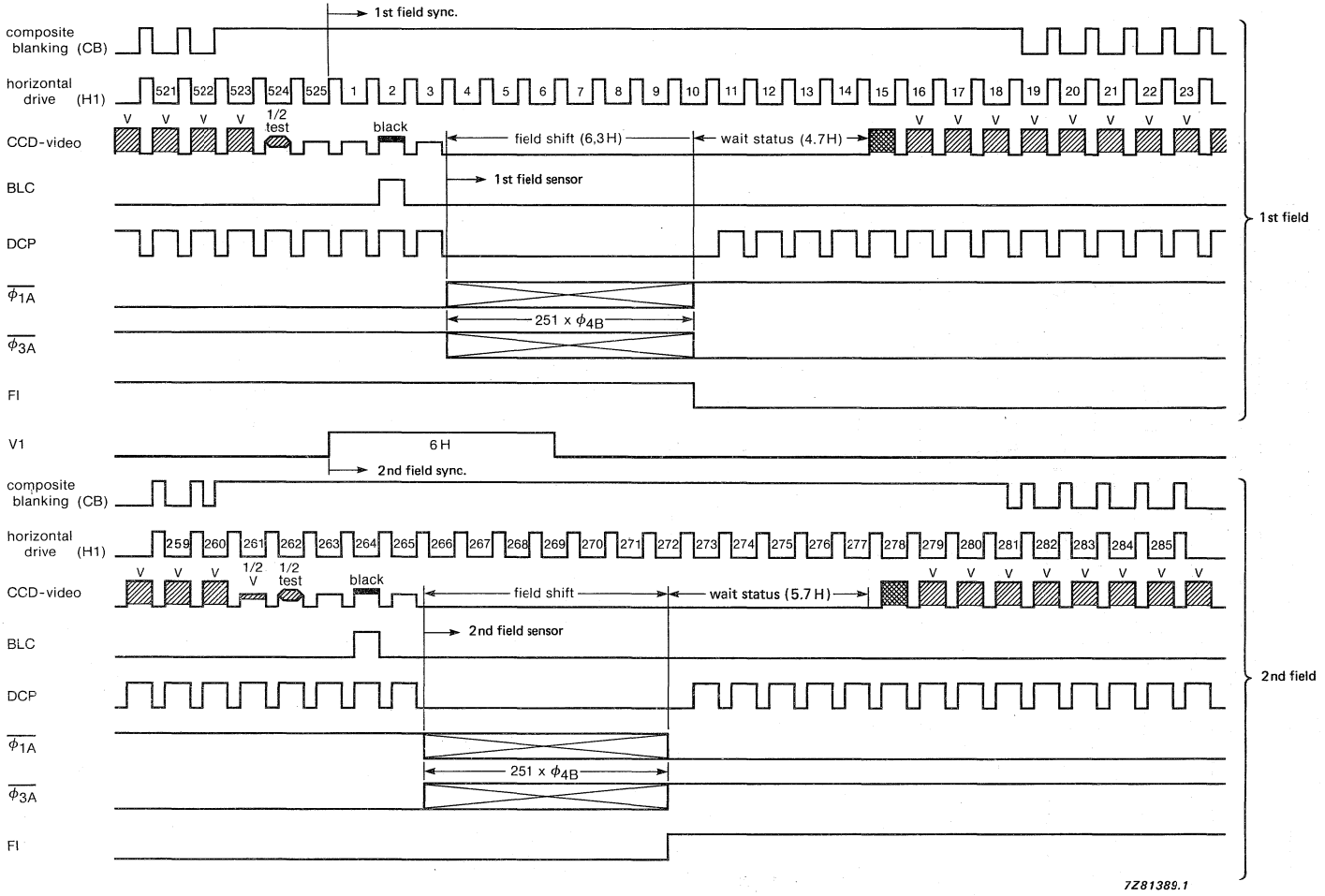


Fig.11 Pulse pattern during field blanking (525 lines

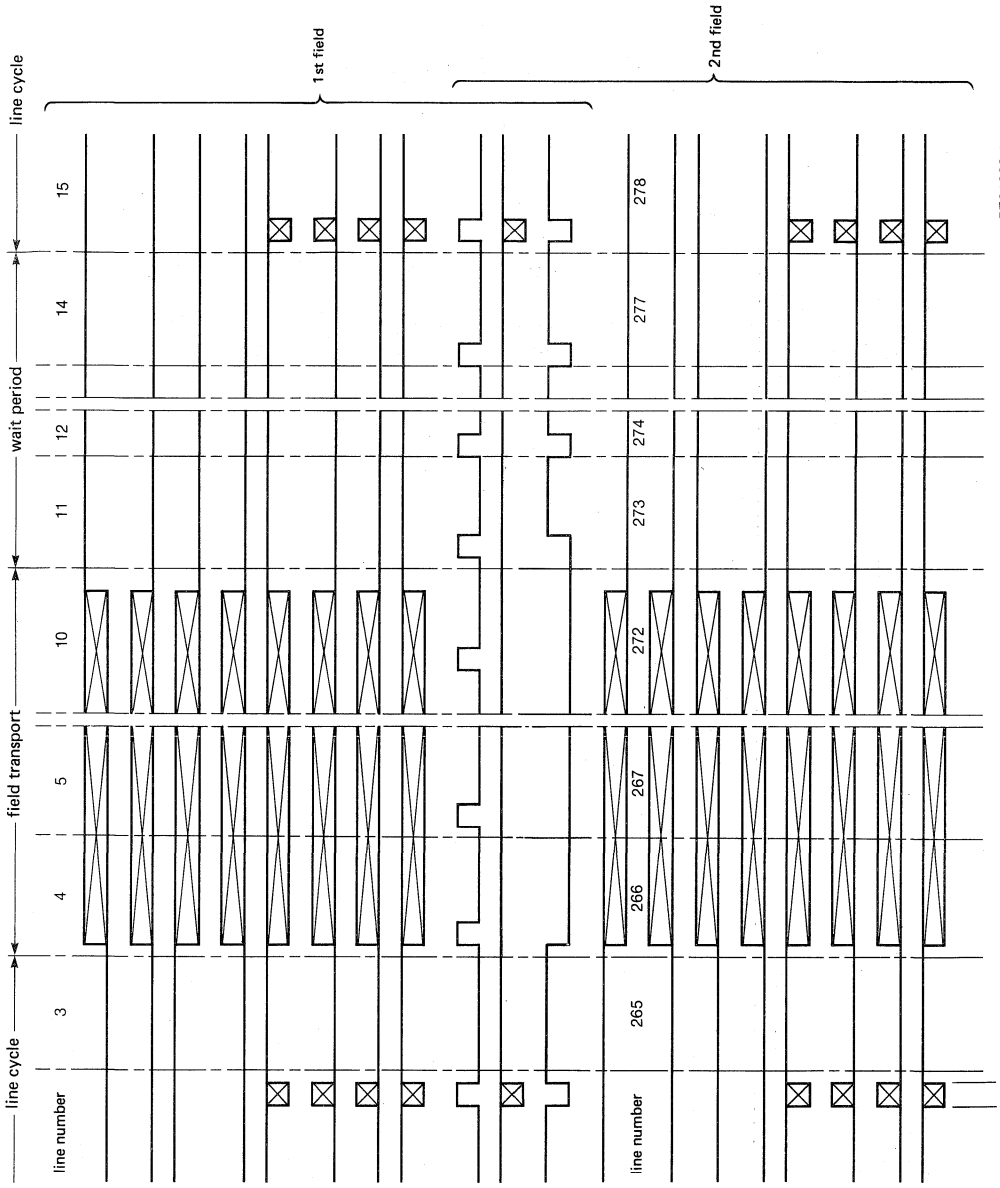


Fig.12 MNPPG cycles during field blanking (525 lines).

DATA LINE DECODER

GENERAL DESCRIPTION

The SAF1135 is a data line decoder, designed in CMOS technology, which operates in conjunction with the data line processor (SAA5235) to form a data line receiver system.

This system receives and decodes binary data that is transmitted in line 16 of every first field of a standard television signal. The decoded information is accessed via the built-in I^2C bus interface. This information can be used to program a video tape recorder to start and stop the recording of a television program at the correct time, regardless of a delay or extension in the transmission time of the required television program.

Valid Video Programming System (VPS) data is transmitted in line 16 only. There is no VPS information in line 329.

The data transmission is biphase modulated and the bit transfer rate is 2,5 Mbit/s.

Features

- Field selection
- Line 16 decoding
- Start code check
- Biphase check
- Storage of data line information
- Generation of data reset pulse
- I^2C bus transmitter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 14)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 14)	I_{DD}	–	1	–	mA
Bit transfer rate at input DLD (pin 8)	BR_{DLD}	–	2,5	–	Mbits/s
Clock frequency at input DLCL (pin 11)	f_{DLCL}	–	5	–	MHz
Storage temperature range	T_{stg}	−65	–	+150	°C
Operating ambient temperature range	T_{amb}	0	–	70	°C

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

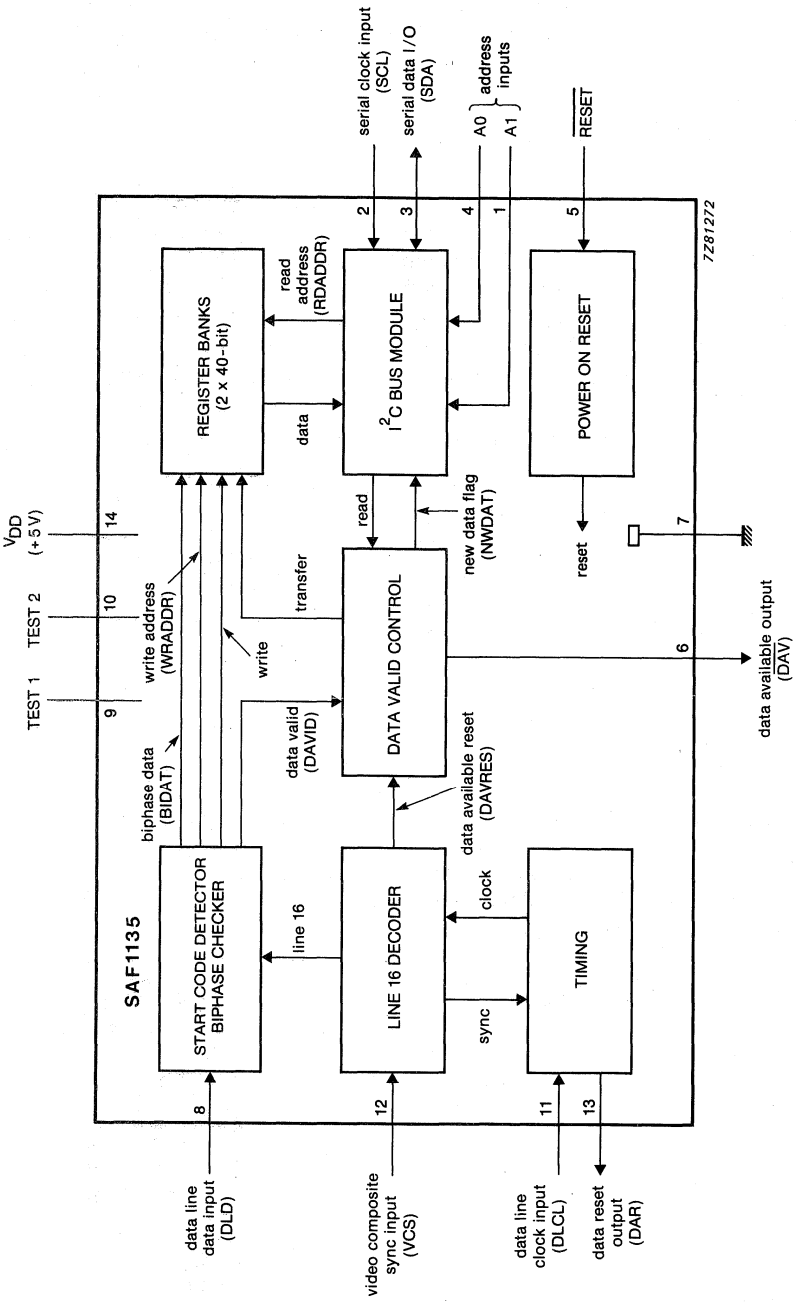


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The SAF1135 is designed to receive and decode Video Tape Recorder (VTR) control information which is transmitted in line 16 of every first field of a standard television signal. The following description refers to the block diagram Fig. 1 unless otherwise stated.

Data line 16

The total information of data line 16 consists of fifteen 8-bit words. The contents of the information is shown in Fig. 2, a timing diagram of the data line in Fig. 3 and a survey of VTR control labels in Fig. 4.

From the total fifteen 8-bit words, the SAF1135 extracts words 5, 11, 12, 13 and 14. The contents of these words can be requested via the built-in I^2C bus interface (see Fig. 9). The circuit is fully transparent, thus each bit is transferred without modification. Only the sequence of the words is changed; words 11 to 14 being transmitted first followed by word 5.

By evaluation of the Video Composite Sync (VCS) signal at pin 12 the SAF1135 identifies the beginning of line 16 in the first field. The line 16 decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection, see Fig. 5) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in register bank R (Receive). If no biphase error has occurred, the contents of register bank R are transferred to register bank T (Transmit) by the data valid control signal (DAVID). If the system has been addressed, this transfer is delayed until the next start or stop condition of the I^2C bus has been received.

The last correct data line information remains available until it is read via the I^2C bus. After it is read once the stored information is no longer considered to be valid, the internal new data flag (NWDAT) is reset and if the circuit is addressed, the only VPS data sent back is "FFF...F". The same conditions apply after power-up. Then no data can be read out.

New data is available after reception of another error-free line 16.

Power-on Reset

Reset pulses applied externally to pin 5 ($\overline{\text{RESET}}$; active LOW) are latched internally by the power-on reset circuit.

$\overline{\text{RESET}}$ = LOW influences:

- I^2C bus logic to no acknowledge
- NWDAT flag and internal timing to reset
- Data available output ($\overline{\text{DAV}}$; active LOW) at pin 6 forced to LOW
- Data reset output (DAR) at pin 13 forced to HIGH
- Serial data (SDA) input/output at pin 3 released

When $\overline{\text{RESET}}$ changes to HIGH the reset period is terminated with the next negative-going transition of the data line clock (DLCL) input at pin 11. Then, the data available ($\overline{\text{DAV}}$) output at pin 6 will go HIGH.

When an external reset is not used pin 5 is connected to V_{DD}. If an external reset is required, the rise time (t_r) of $\overline{\text{RESET}}$ voltage must be greater than 50 μs. An external 10 kΩ resistor connected between pin 5 and V_{DD} and an external 2,7 nF capacitor connected to V_{SS} will result in $t_r \geqslant 50$ μs.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Word	Content
1	Run in
2	Start code
3	Program source identification (binary coded)
4	Program source identification (ASCII sequential)
5	Sound and VTR control information
6	Program/Test picture identification
7	Internal information exchange
8	Address assignment of signal distribution
9	
10	Messages/Commands
11	VTR Control Information
12	
13	
14	
15	Reserve

Fig. 2 Total information of data line 16.

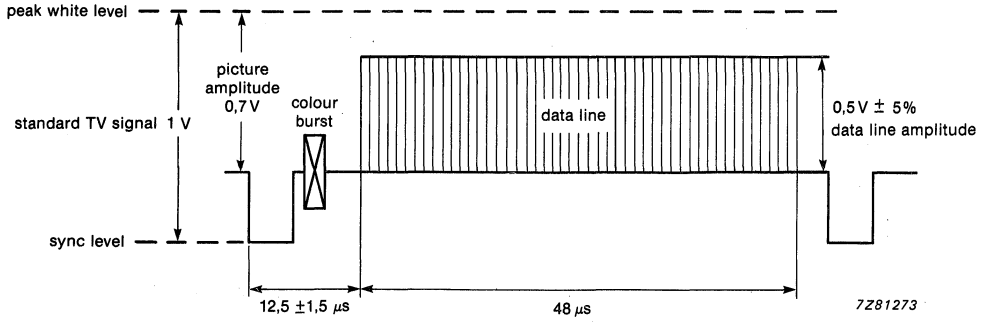


Fig. 3 Timing diagram of data line 16; modulation depth 71,4%.

VTR Control Information

Word-no.	5								11								12								13								14							
Bit-no.	1	2	3	4	5	6	7	8	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Label binary	Bit 1	Bit 2	Status						Address range	Day							Month				Hour				Minute								Nation							Program Source	
	0	0	2-Channel						Special System Code																															
	0	1	Mono																																					
	1	0	Stereo																																					
	1	1	2-Channel																																					
System Status Code									1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		
	Bit 3	Bit 4																																						
Pause Code	1	0	not for children						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		
Interrupt Code	0	1	free						1	X	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	NC	. .	NC	PC	. . . .	PC		

Where:

X = 0 or 1 (bit)
NC is the Nation Code
PC is the Program Source Code

Fig. 4 VTR control information of data line 16.

DEVELOPMENT DATA

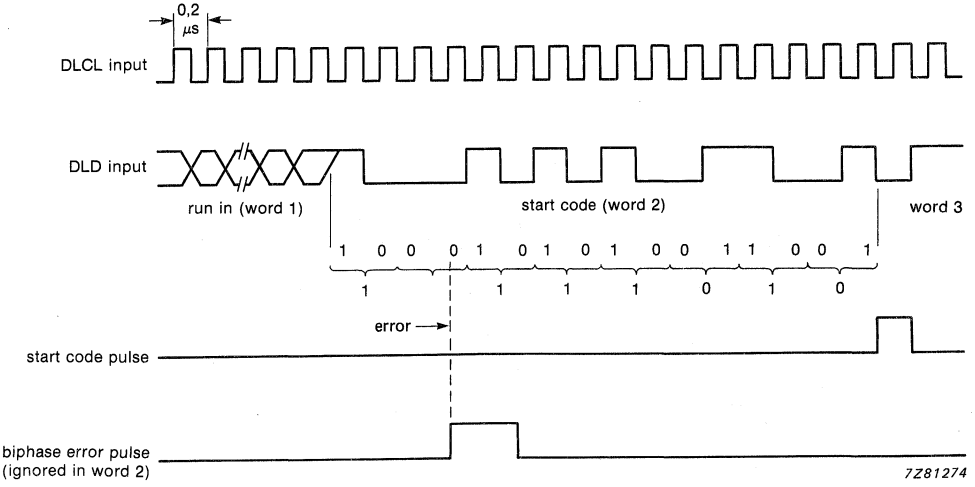


Fig. 5 Timing diagram of start code detection.

FUNCTIONAL DESCRIPTION (continued)

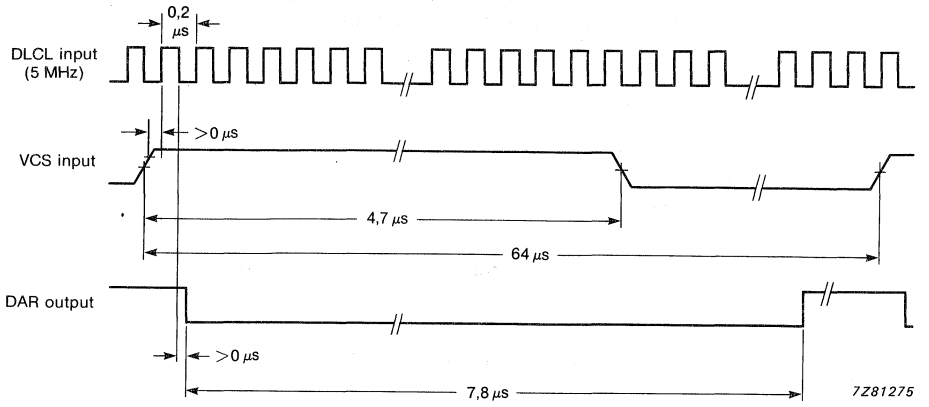


Fig. 6 Timing diagram of the data reset pulse generation.

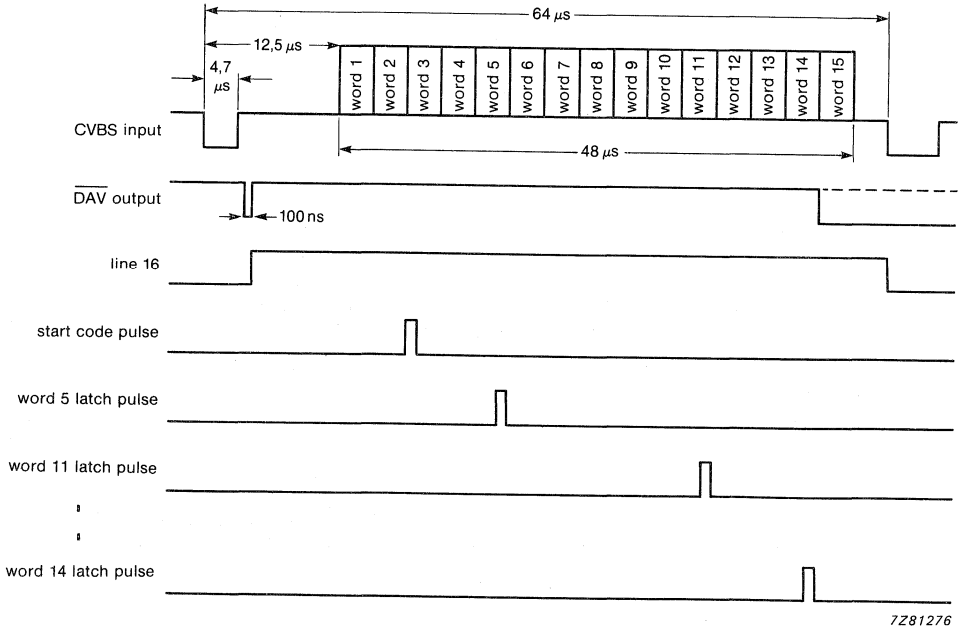


Fig. 7 Timing diagram of the data available output and word latch pulses.

Data line data and clock inputs (DLD; DLCL)

The data line data and clock signals from the SAA5235 are input at pins 8 and 11 respectively. The data transmission is biphase modulated, the bit transfer rate is 2,5 Mbit/s and the clock frequency is 5 MHz.

Input DLD incorporates an internal active clamping circuit. DLCL is internally a.c. coupled.

Video composite sync input (VCS)

The VCS input pulse at pin 12 is used for:

- Generation of the data reset pulse (DAR)
- Identification of the first field
- Selection of line 16

The timing of the data reset pulse generation is shown in Fig. 6.

I^2C bus address inputs (A0; A1)

The two I^2C address inputs at pins 4 and 1 respectively, provide the four different addresses 20H, 22H, 24H and 26H.

Data reset output (DAR)

The DAR output at pin 13 is a line frequency pulse with a 0,88 duty factor derived from the VCS pulse. The DAR pulse is fed to the SAA5235 to reset the data slicer circuit and the clock phase detector circuit.

Data available output ($\overline{DAV}$)

The $\overline{DAV}$ active LOW output at pin 6 is set to LOW after reception of one error-free data line 16. $\overline{DAV}$ returns to HIGH after at the beginning of the next first field.

If no valid data is available $\overline{DAV}$ remains HIGH. However, a short duration (100 ns) pulse inserted at the beginning of line 16 ensures that a HIGH-to-LOW transition occurs, which can be used for triggering.

The timing of $\overline{DAV}$ output and word latch pulses is shown in Fig. 7.

I^2C bus

The internally latched data from words 5 and 11 to 14 can be clocked out via the I^2C interface by a bus master. The lines are the serial clock input (SCL) at pin 2 and the serial data input/output (SDA) at pin 3.

The SAF1135 can operate only as a slave transmitter on the bus.
Data format is shown in Fig. 8.

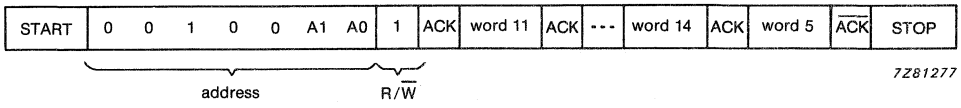


Fig. 8 I^2C bus data format.

- The MSB of each word is transmitted first.
- There is no restriction on the number of words to be transmitted, but if more than five words are requested, word 5 will be repeated.
- Noise pulses less than 200 ns duration are ignored on the bus lines.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 14)	V_{DD}		−0,5 to +7,0	V
Supply current (pin 14)	I_{DD}	max.	20	mA
Supply current (pin 7)	I_{SS}	max.	20	mA
Input voltage (pins 8 and 11)	V_I		−0,5 to +12	V
Input voltage on all other pins	V_I		−0,5 to V_{DD} +0,5*	V
Input current	$\pm I_I$	max.	10	mA
Output current	$\pm I_O$	max.	10	mA
Power dissipation per package**	P_{tot}	max.	400	mW
Power dissipation per output	P	max.	100	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* V_{DD} +0,5 not to exceed 7,0 V.

** Above +60 °C: derate linearly with 8 mW/K.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 14)						
Supply voltage	–	V_{DD}	4,5	5	5,5	V
Supply current	Quiescent at 25 °C All inputs at V_{DD} or V_{SS} $\overline{RESET}$ at V_{SS} TEST 1 and TEST 2 at V_{DD} I_O = 0 mA	I_{DD}	–	–	10	μA
	During normal operation (without LED at $\overline{DAV}$, V_{DD} = 5 V)	I_{DD}	–	1	–	mA
Inputs						
A0, A1, TEST 1, TEST 2, SCL						
Input voltage LOW		V_{IL}	–	–	0,2V_{DD}	V
Input voltage HIGH		V_{IH}	0,7V_{DD}	–	–	V
Leakage current		I_{LI}	–	–	1	μA
DLCL						
Input voltage	Clock internally a.c. coupled	V_I	–	–	12	V
Leakage current	V_I = 0 to 10 V	I_{LI}	–	–	10	μA
$\overline{RESET}$	During normal operation pin 5 connected to V_{DD}					
Input voltage LOW		V_{IL}	–	–	0,3V_{DD}	V
Input voltage HIGH		V_{IH}	0,9V_{DD}	–	–	V
Input current HIGH		I_{IH}	–	–	15	μA
Leakage current		I_{LI}	–	–	10	μA
VCS						
Input voltage LOW		V_{IL}	–	–	0,8	V
Input voltage HIGH		V_{IH}	2,0	–	–	V
Leakage current		I_{LI}	–	–	1	μA

D.C. CHARACTERISTICS (continued)

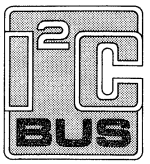
parameter	conditions	symbol	min.	typ.	max.	unit
Inputs/Outputs						
DLD	Internal active clamping circuit, open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	2,0	–	12	V
Leakage current		I_{LI}	–	–	1	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
SDA	open drain output					
Input voltage LOW		V_{IL}	–	–	0,9	V
Input voltage HIGH		V_{IH}	3,15	–	–	V
Leakage current	V_{DD} = 6 V; V_I = 0 or V_{DD}	I_{LI}	–	–	6	μA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Outputs						
DAR						
Output voltage LOW	I_{OL} = 1 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V
$\overline{DAV}$						
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1,0	V
Output voltage HIGH	$-I_{OH}$ = 400 μA	V_{OH}	V_{DD}–0,5 V	–	–	V

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs						
Input capacitance		C_I	–	–	10	pF
A0, A1, TEST 1, TEST 2, SCL						
Rise time	$V_{IL(max)}$ to $V_{IH(min)}$	t_r	50	–	–	μs
DLCL						
Clock frequency	sinusoidal input signal	f_{DLCL}	–	5	–	MHz
Input voltage	peak-to-peak value	$V_{I(p-p)}$	1	–	–	V
DLD						
Coupling capacitor		C_{EXT}	—	1	4,7	nF
Set-up time	relative to rising edge of DLCL	t_{SU}	40	–	–	ns
Hold-up time	relative to rising edge of DLCL	t_{HD}	40	–	–	ns
Outputs						
DAR, $\overline{DAV}$						
Rise and fall times	C_L = 50 pF	t_r, t_f	–	–	50	ns
DAR-time LOW		$t_{DAR,L}$	–	7,8	–	μs
SDA						
Fall time	C_L = 400 pF	t_f	–	–	300	ns
I²C bus - Input/Output						
	For both SDA and SCL valid					
Input current HIGH	0,9 V_{DD}, including I_{LI} of possible output stage	I_{IH}	–	–	10	μA
Input capacitance		C_I	–	–	10	pF
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	0,3	μs
Clock frequency		f_{CL}	–	–	100	kHz
Pulse duration LOW		t_{LOW}	4,7	–	–	μs
Pulse duration HIGH		t_{HIGH}	4,0	–	–	μs



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

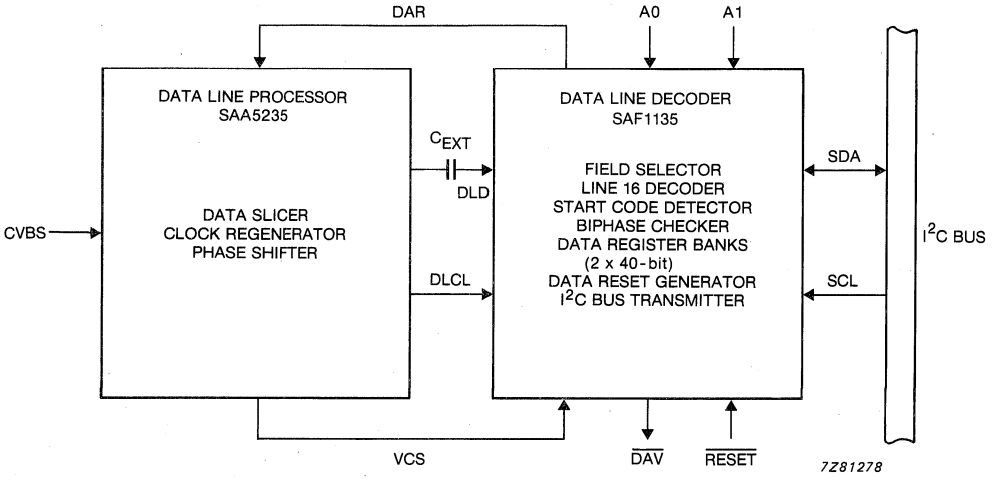


Fig. 9 Data line receiver.

SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

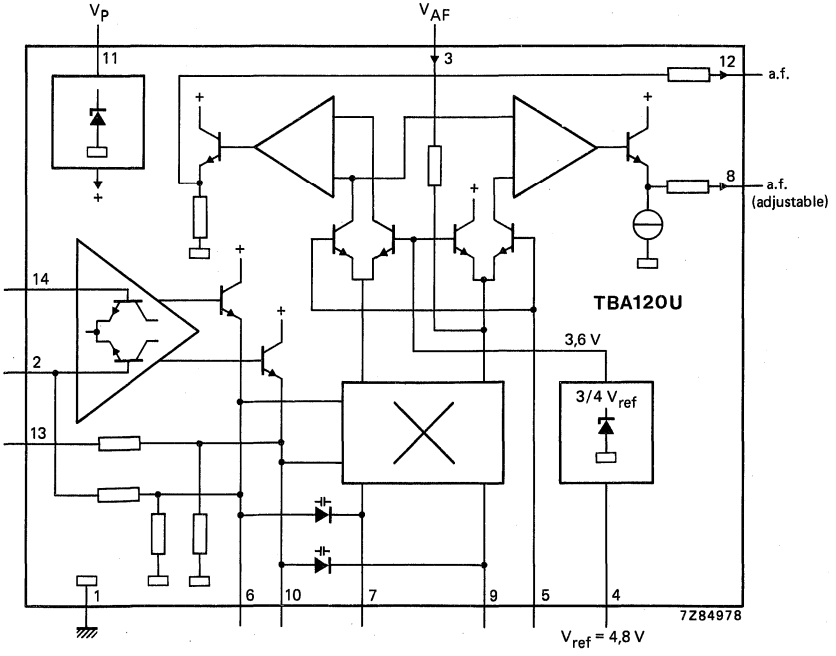


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT27).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\,af\,(rms)}$	typ.	1,0 V
at pin 8	$V_{o\,af\,(rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

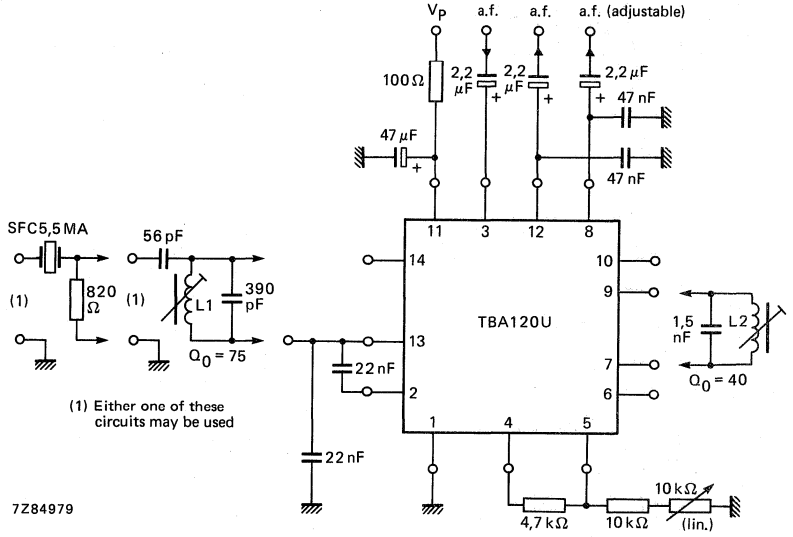


Fig. 2 Application example using TBA120U.

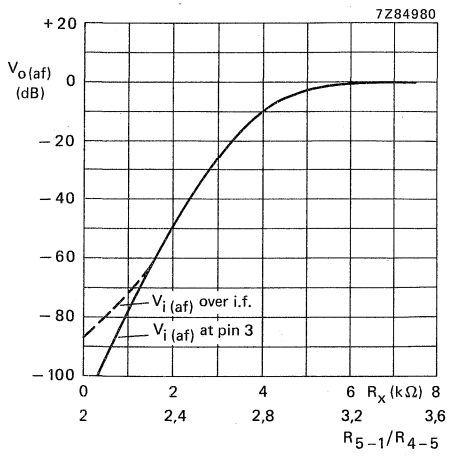


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

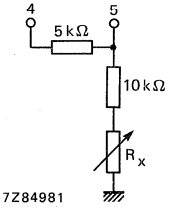
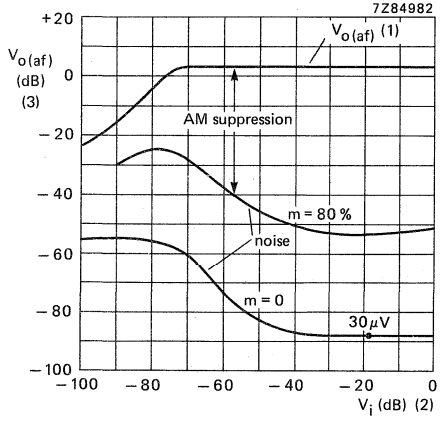


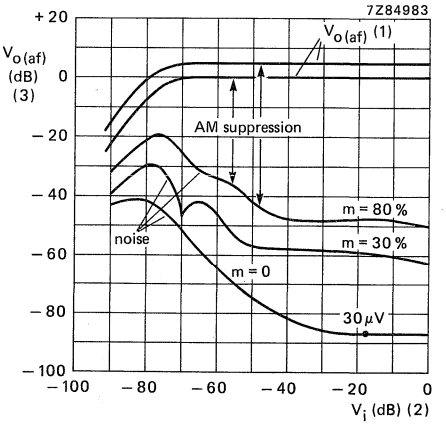
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

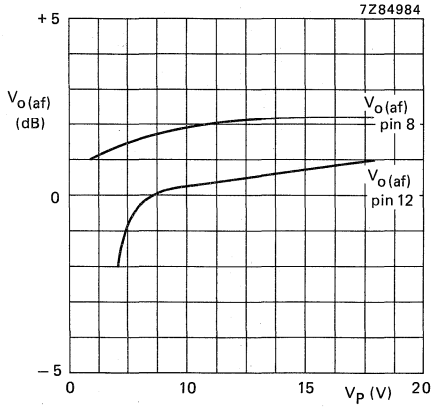


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

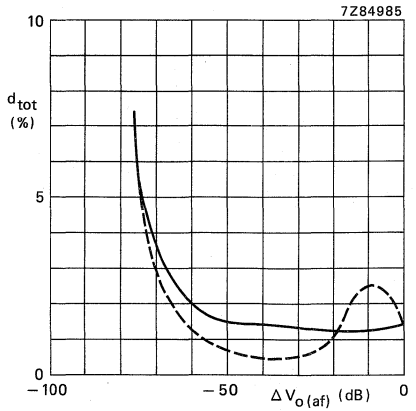


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

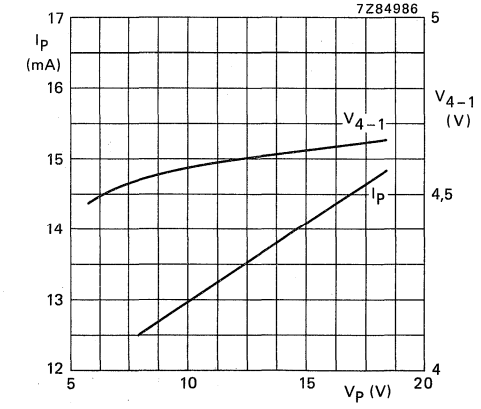


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_v\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

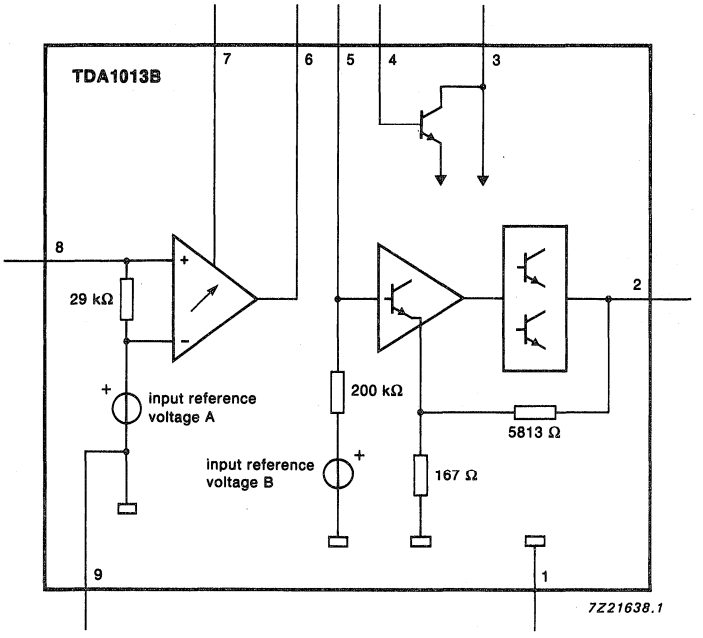


Fig.1 Block diagram.

PINNING

1 signal ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 power ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–55	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

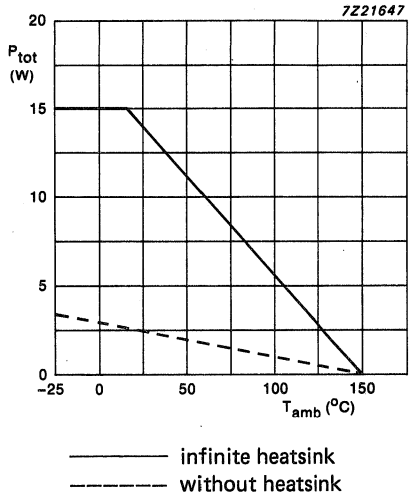


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

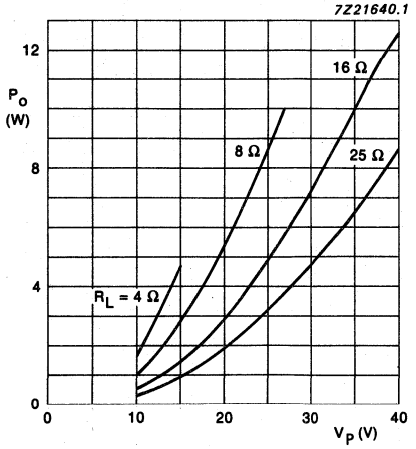


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

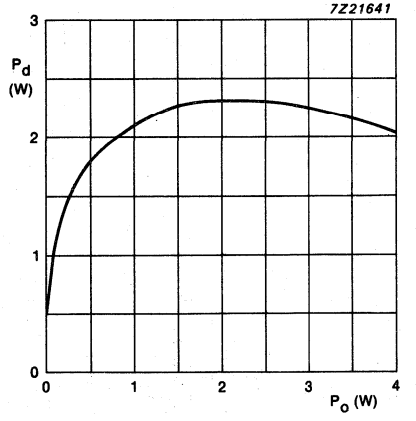


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

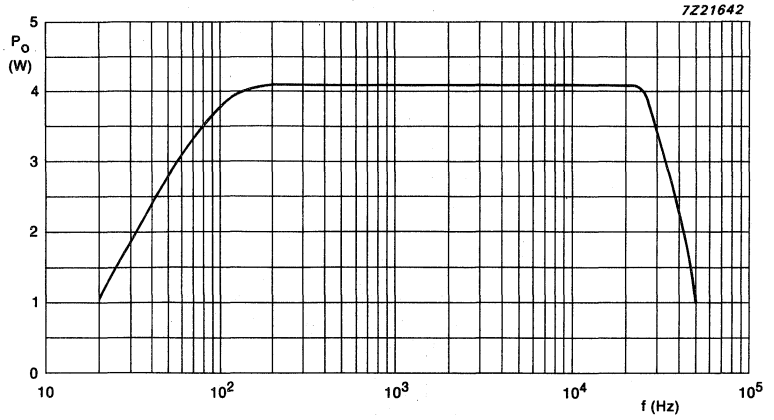


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω; THD = 10% and control voltage (V_7) = 6.5 V.

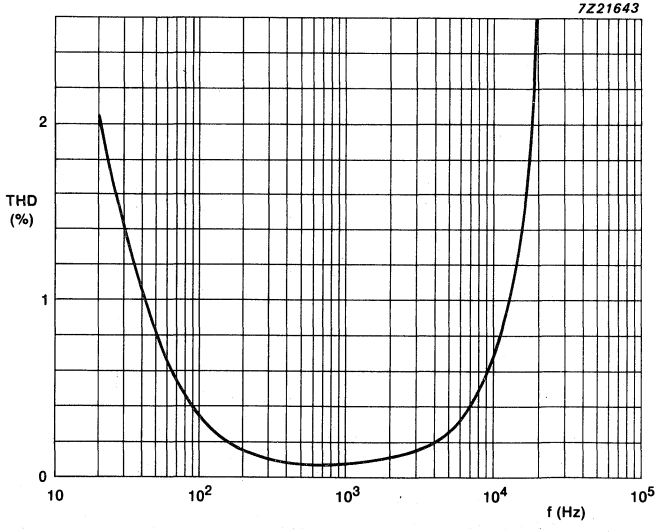


Fig.6 Total harmonic distortion as a function of frequency; V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

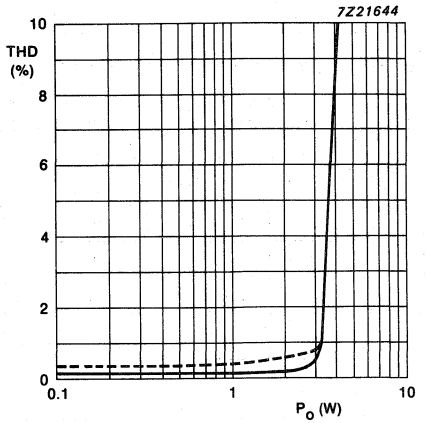


Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

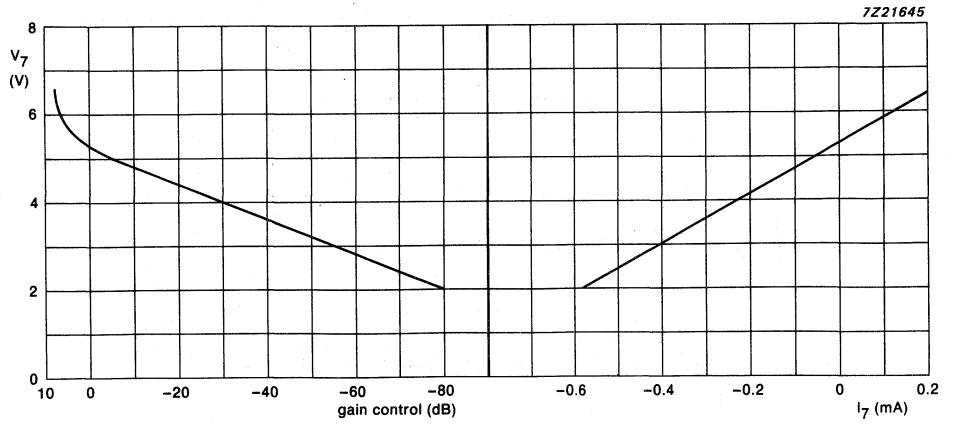


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

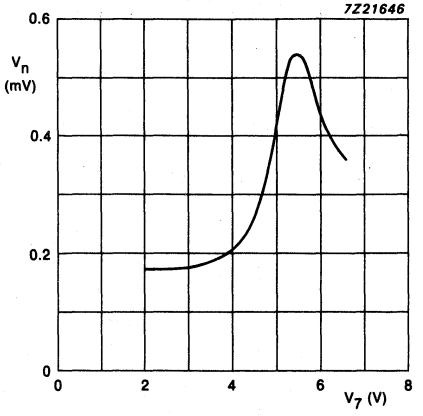
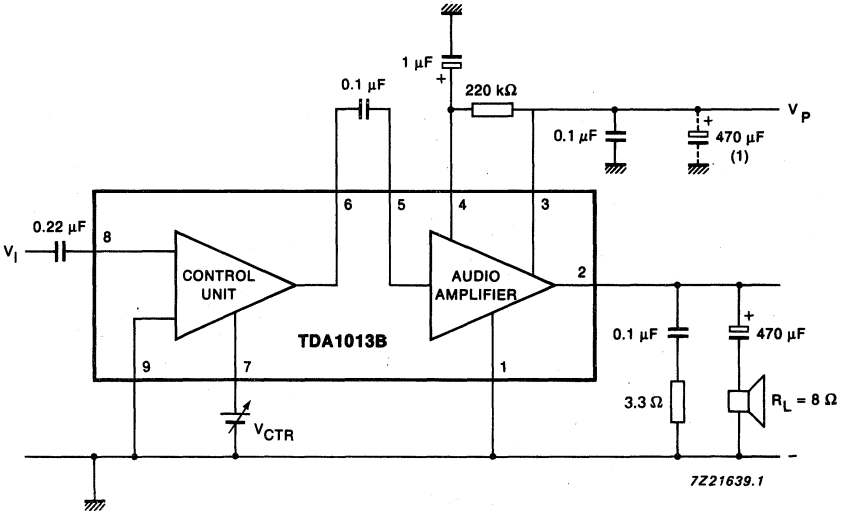


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	>	100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT 110B).

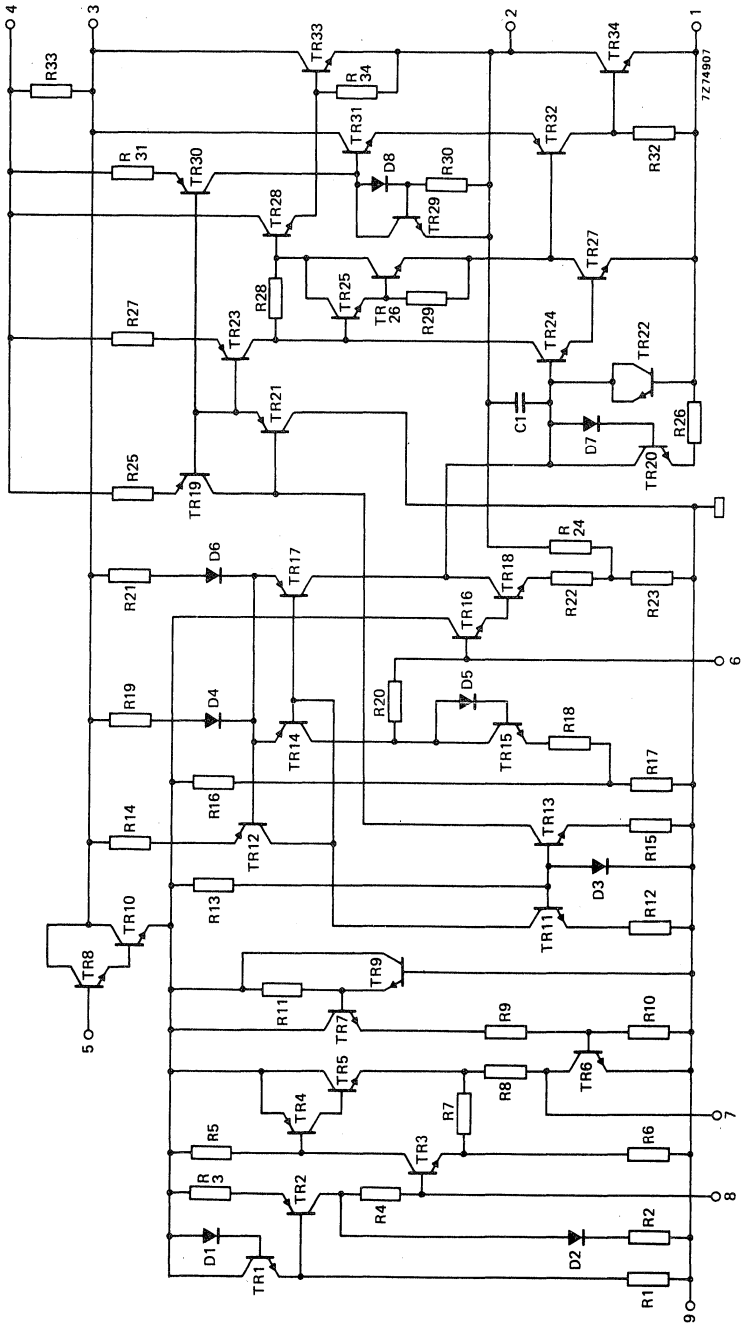


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Peak output current	I_{OM}	max.	2,5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

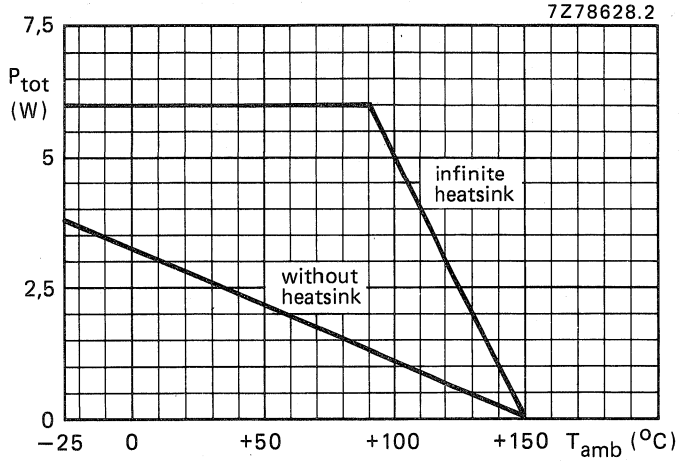


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1,8} = 58\ K/W.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

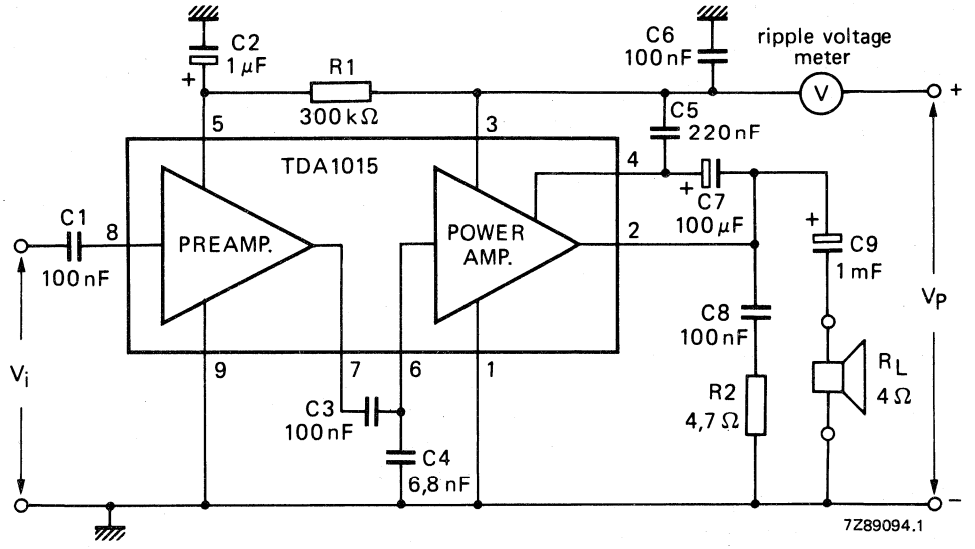


Fig. 3 Test circuit.

APPLICATION INFORMATION

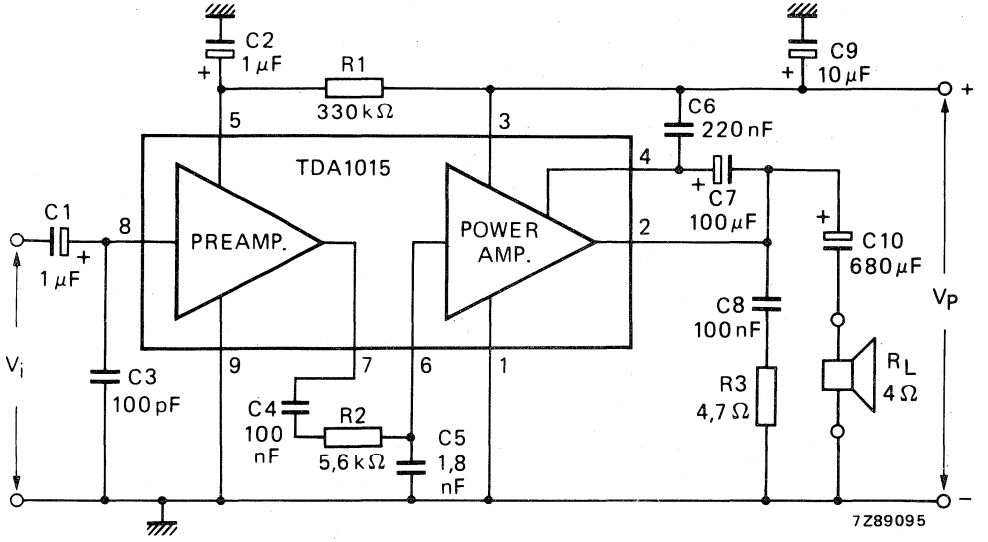


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

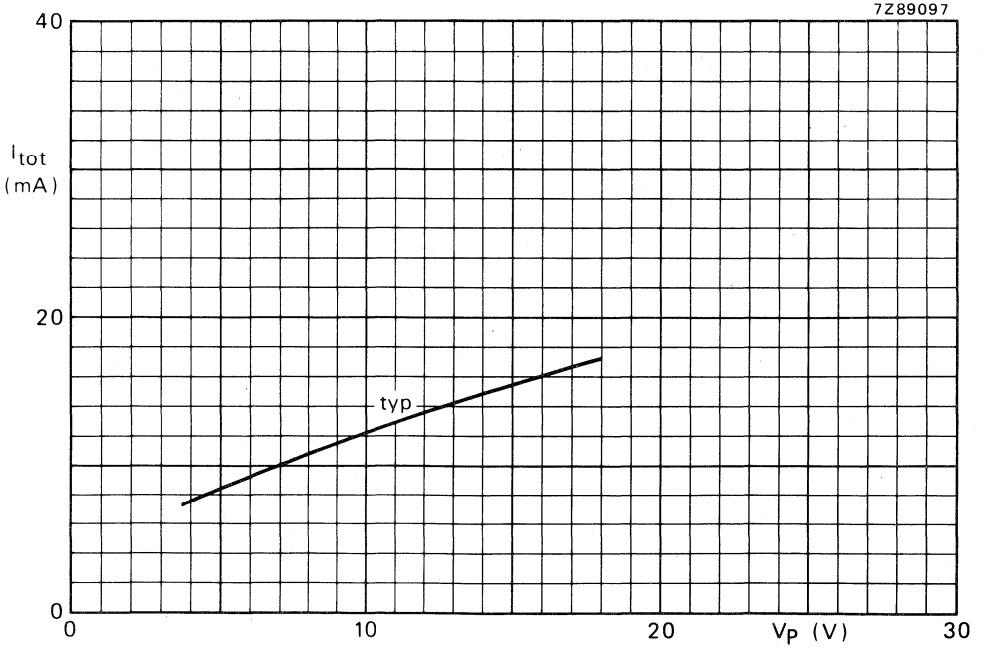


Fig. 5 Total quiescent current as a function of supply voltage.

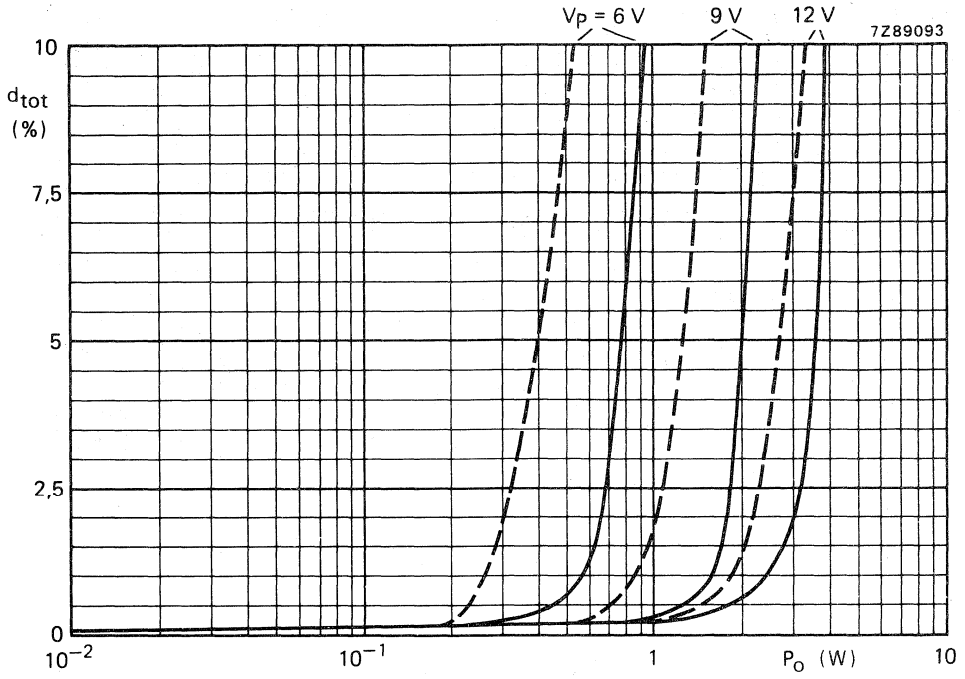


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

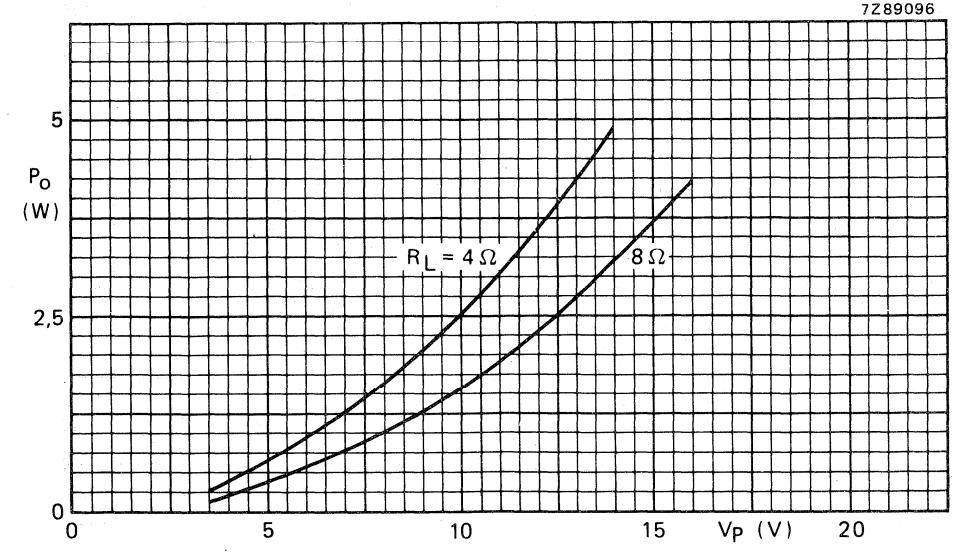


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

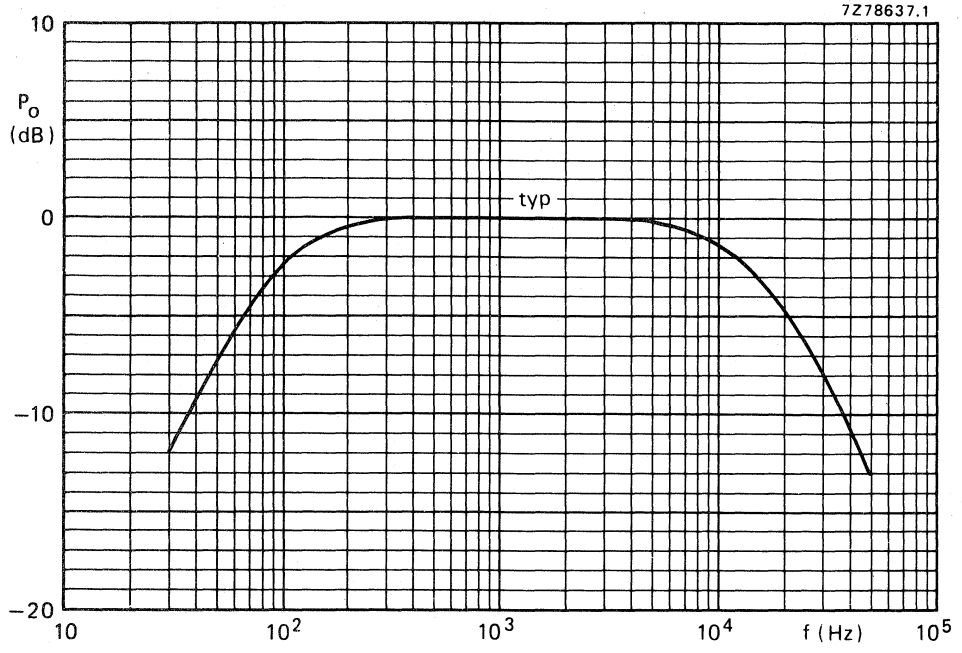


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

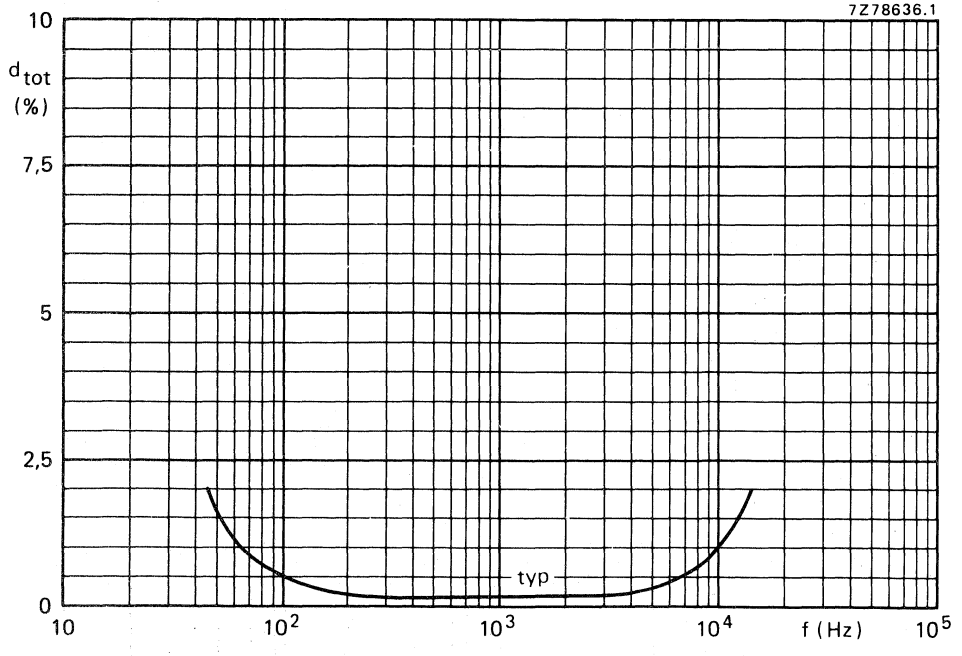


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

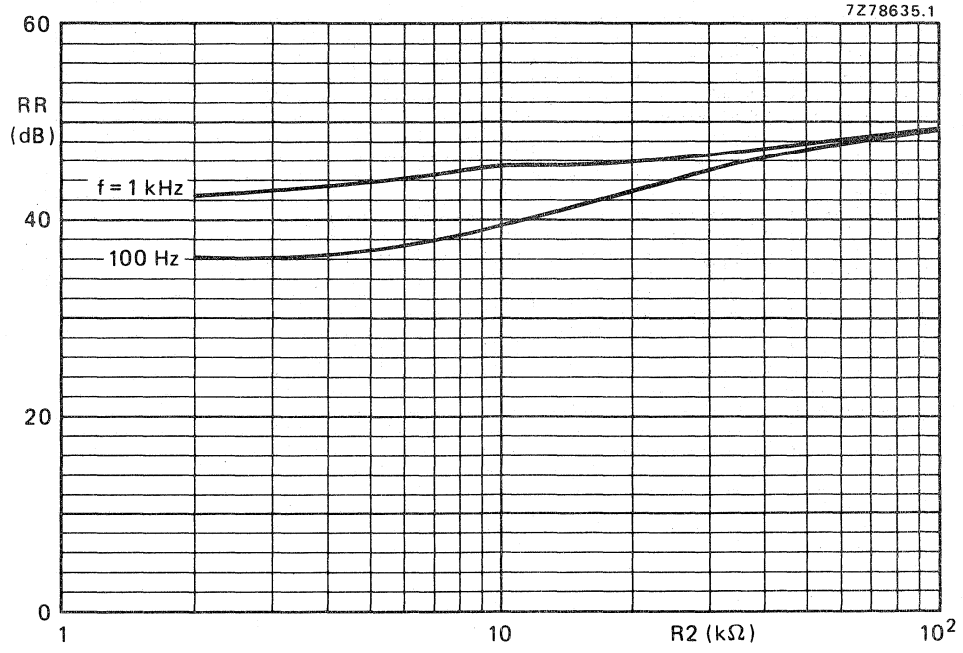


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

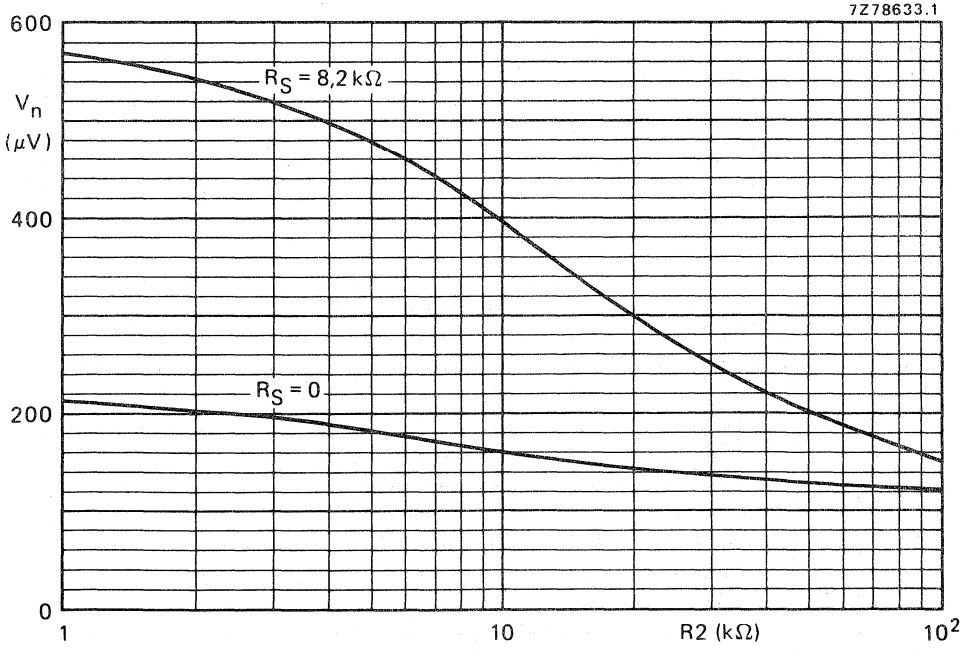


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

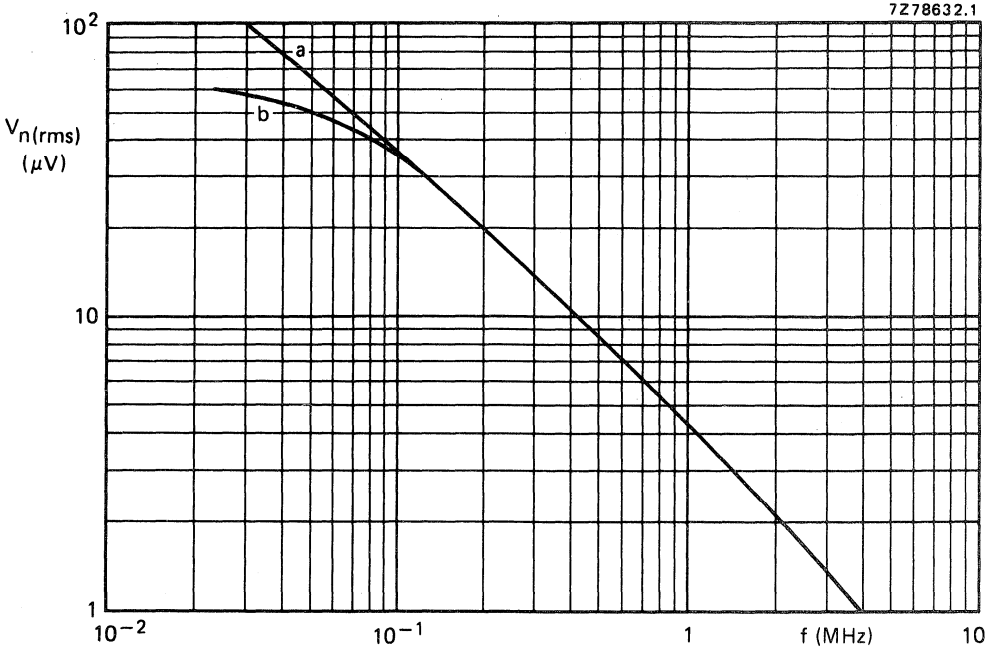


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

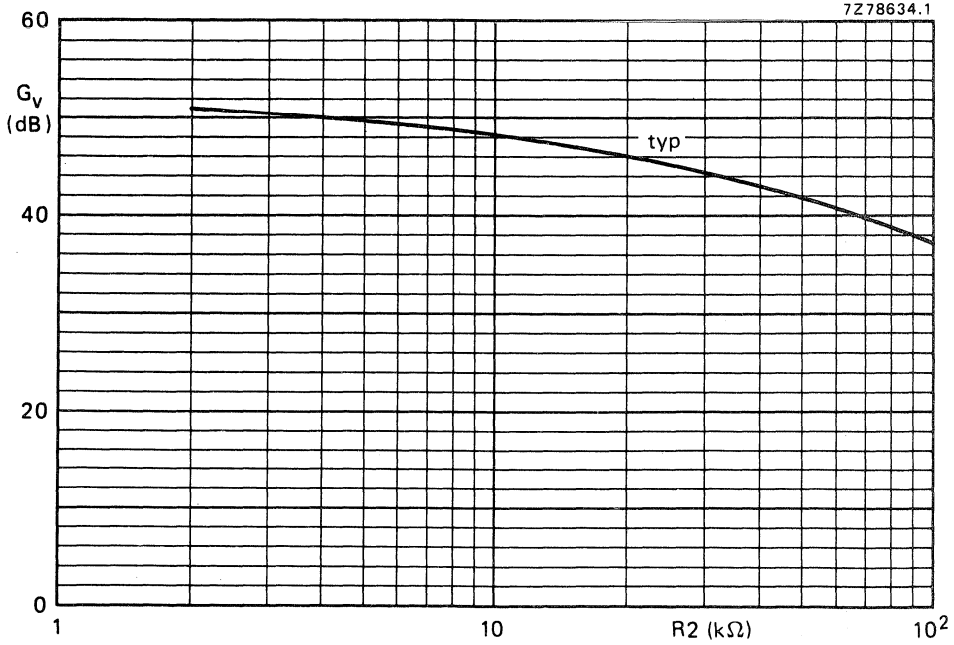


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

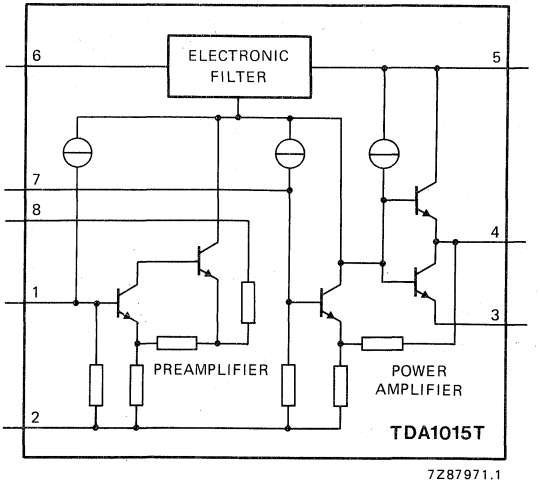


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

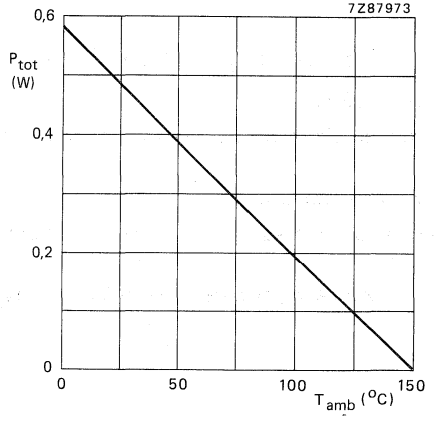


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

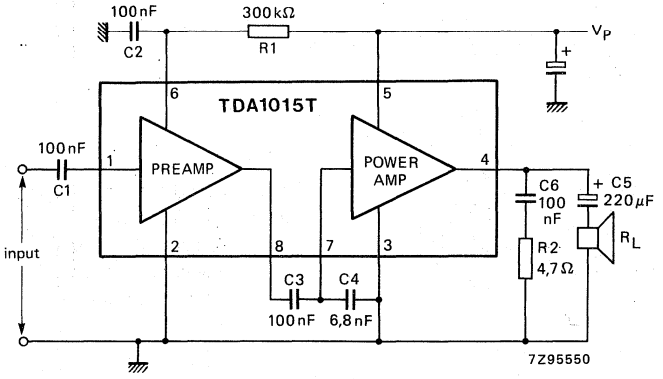


Fig. 3 Test circuit.

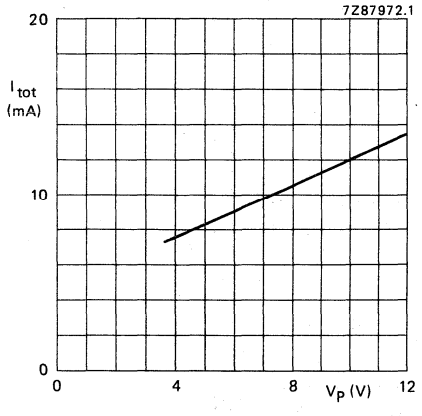


Fig. 4 Total quiescent current as a function of supply voltage.

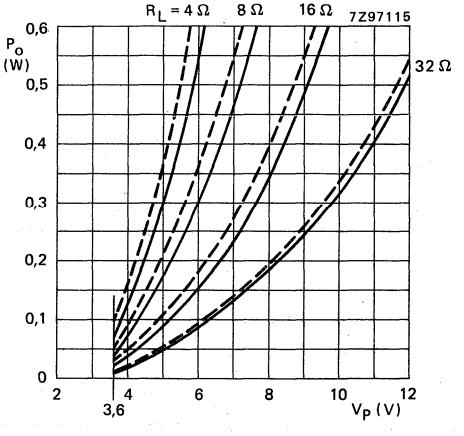


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

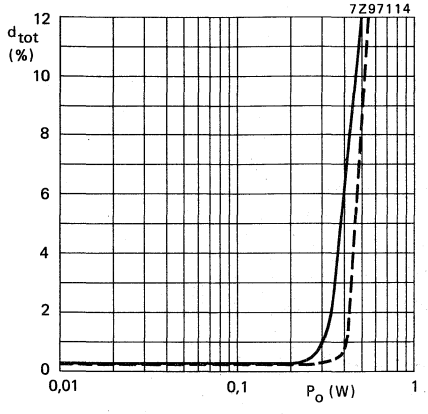


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2..

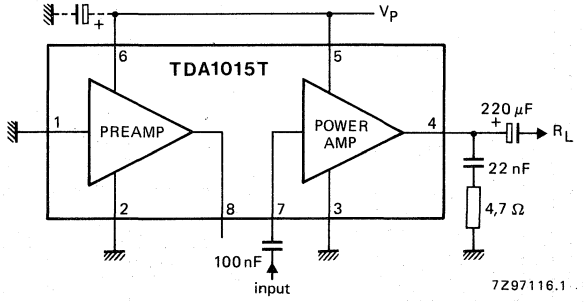


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

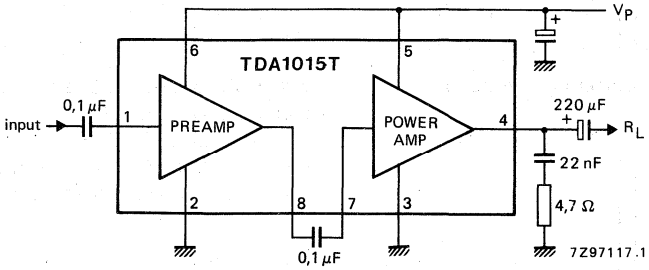


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\ tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

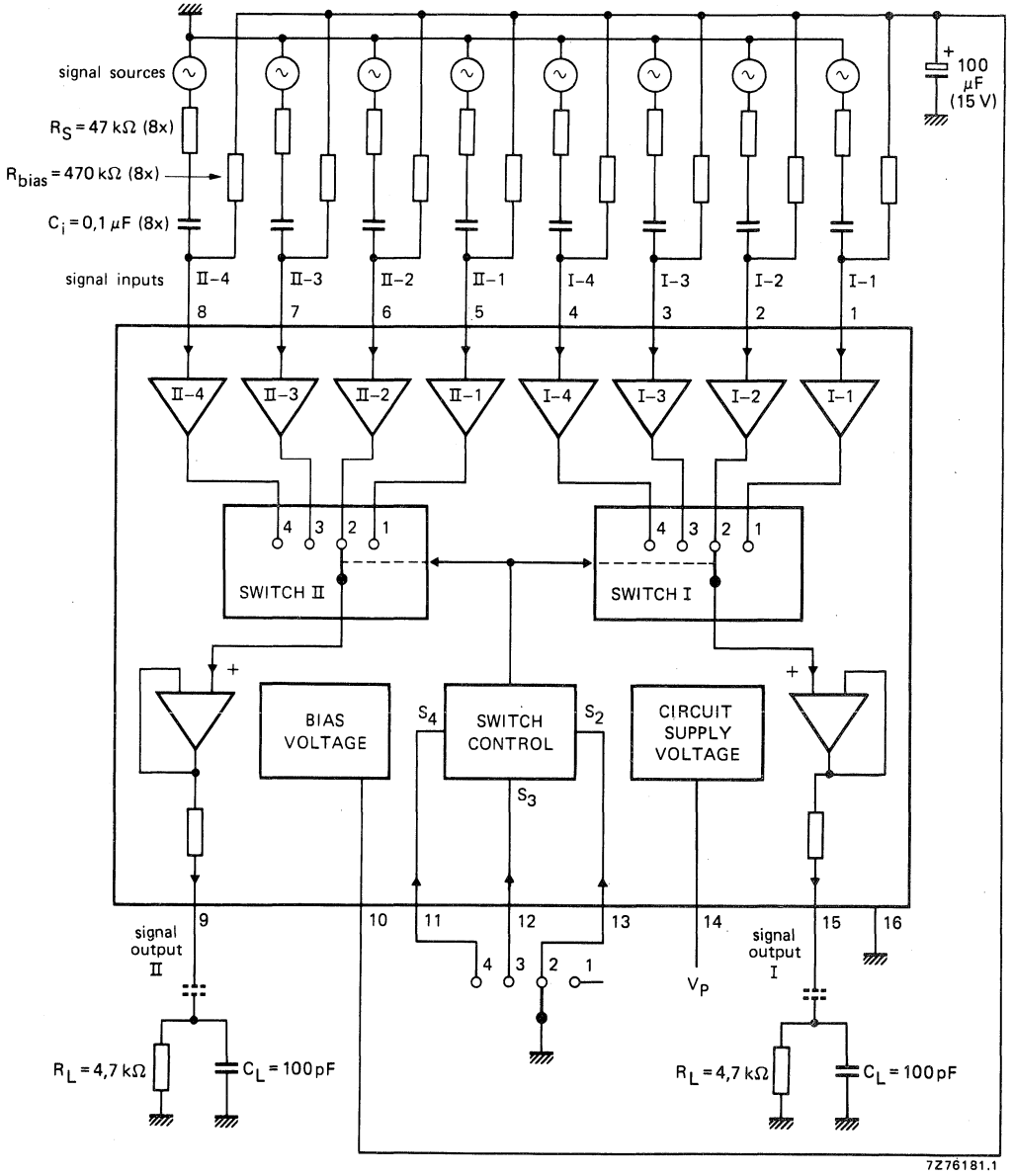


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage				
of switched-on inputs		typ.	2	mV
$R_S \leqslant 1$ kΩ	V_{io}	<	10	mV
Input offset current		typ.	20	nA
of switched-on inputs	I_{io}	<	200	nA
Input offset current				
of a switched-on input with respect to a		typ.	20	nA
non-switched-on input of a channel	I_{io}	<	200	nA
Input bias current		typ.	250	nA
independent of switch position	I_i	<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage				
R_S = 0; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current				
f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input				
and a non-switched-on input;				
measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

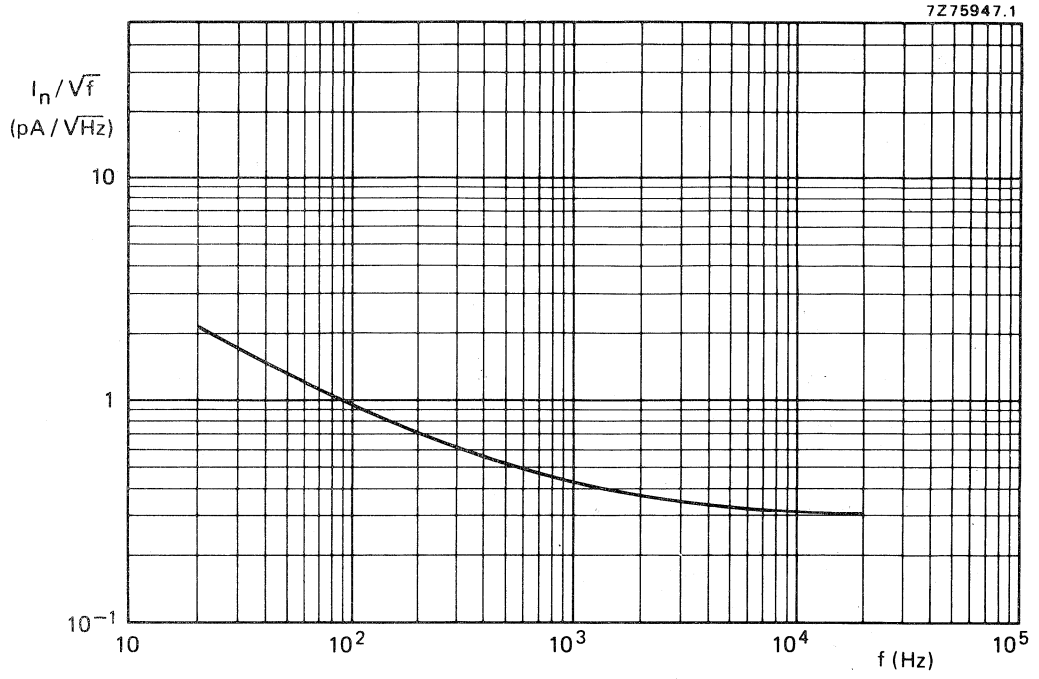


Fig. 2 Equivalent input noise current.

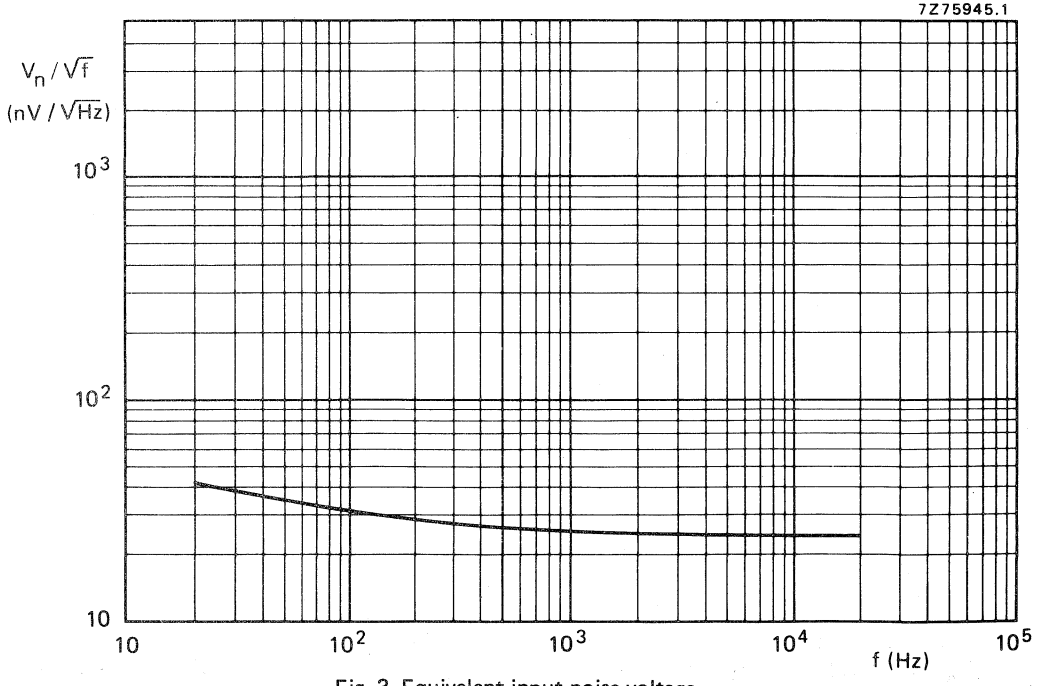


Fig. 3 Equivalent input noise voltage.

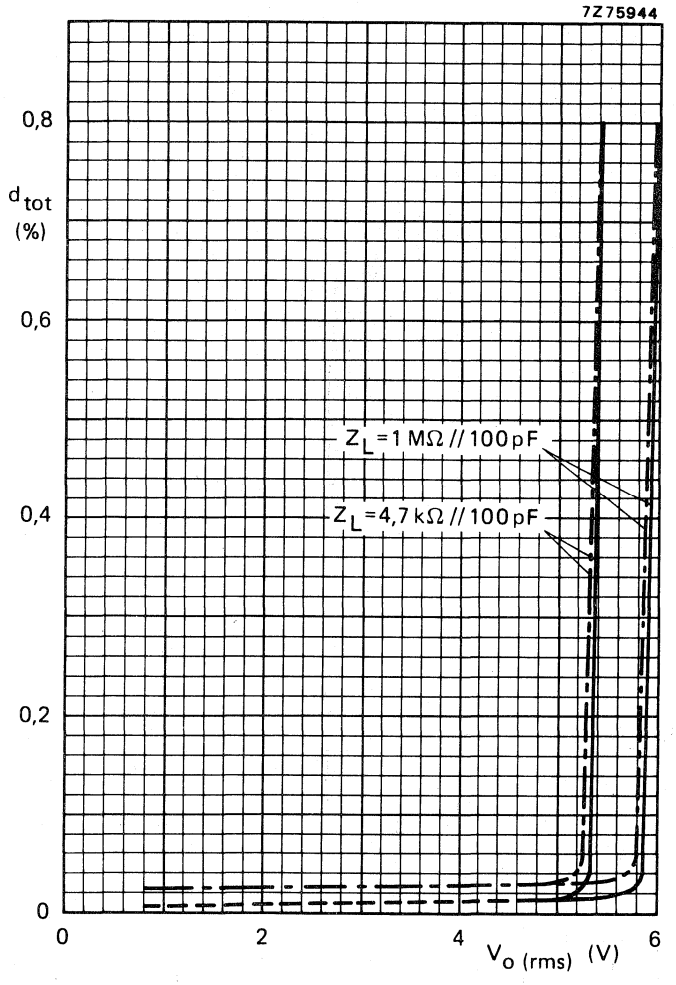


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

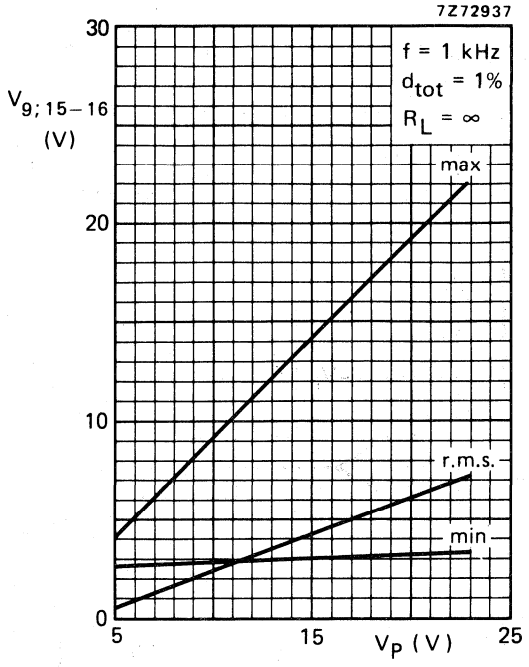


Fig. 5 Output voltage as a function of supply voltage.

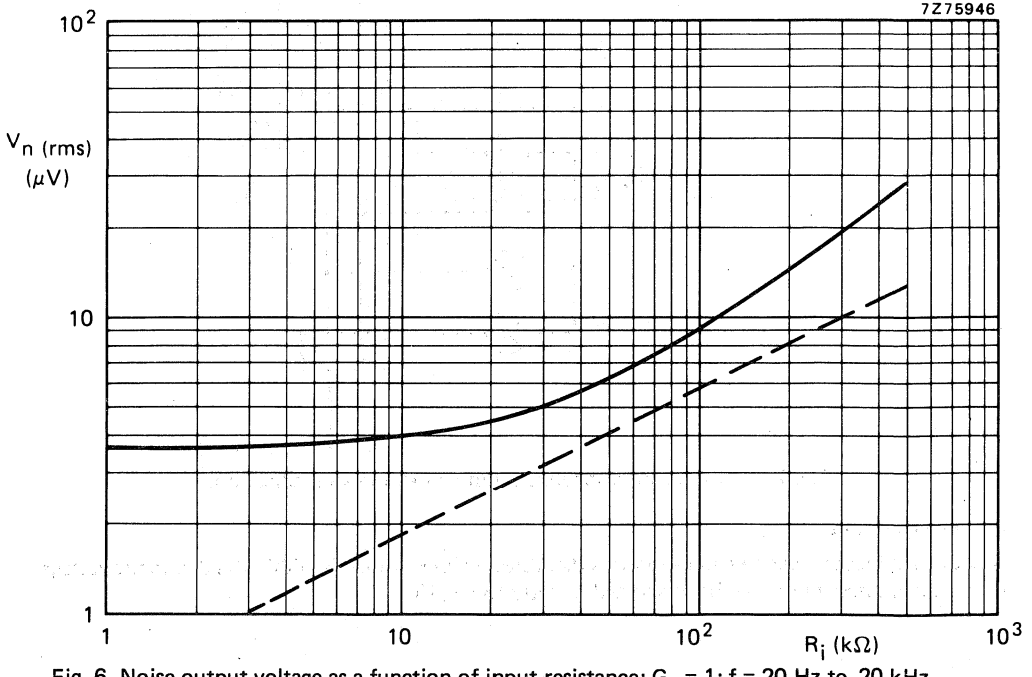


Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

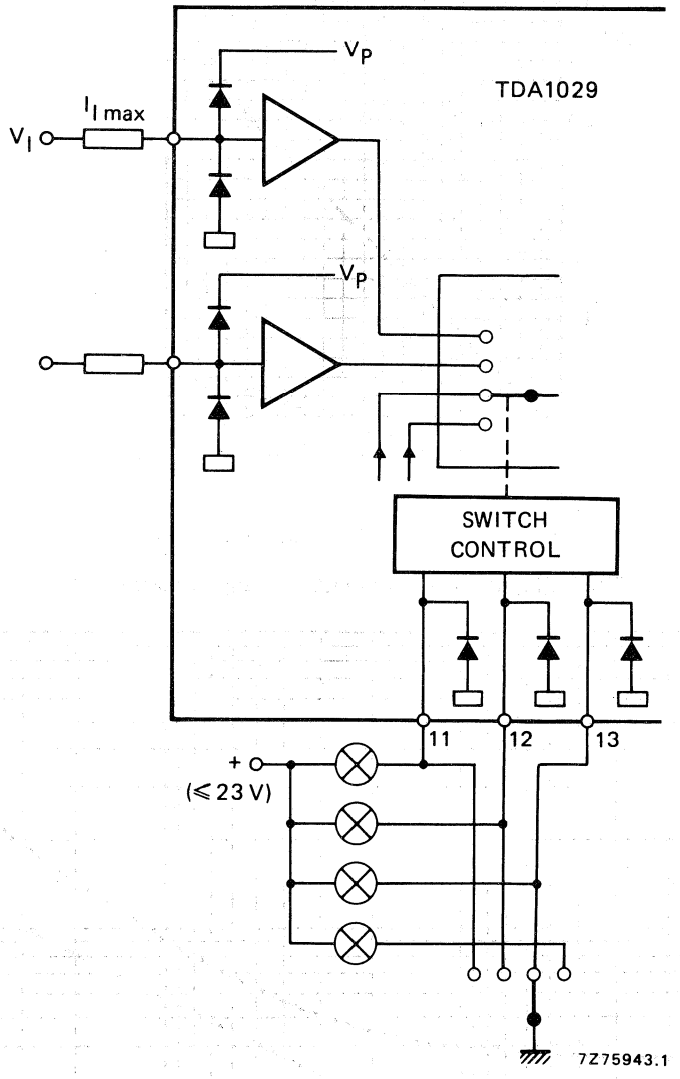


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

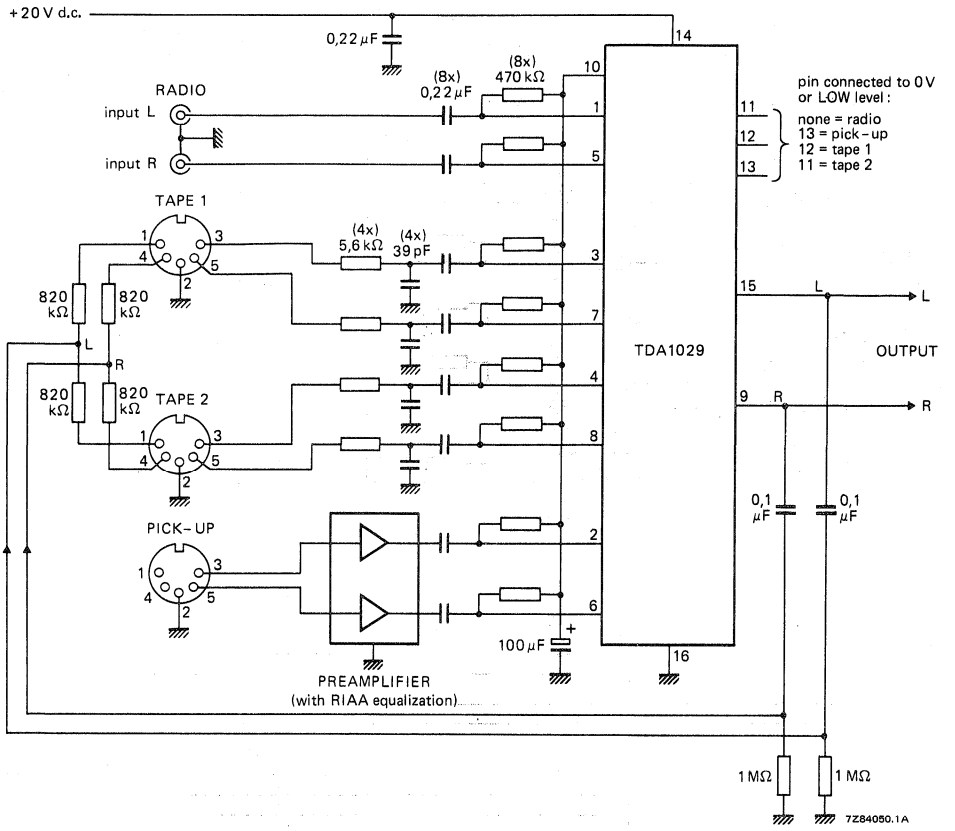


Fig. 8 TDA1029 connected as a four input stereo source selector.

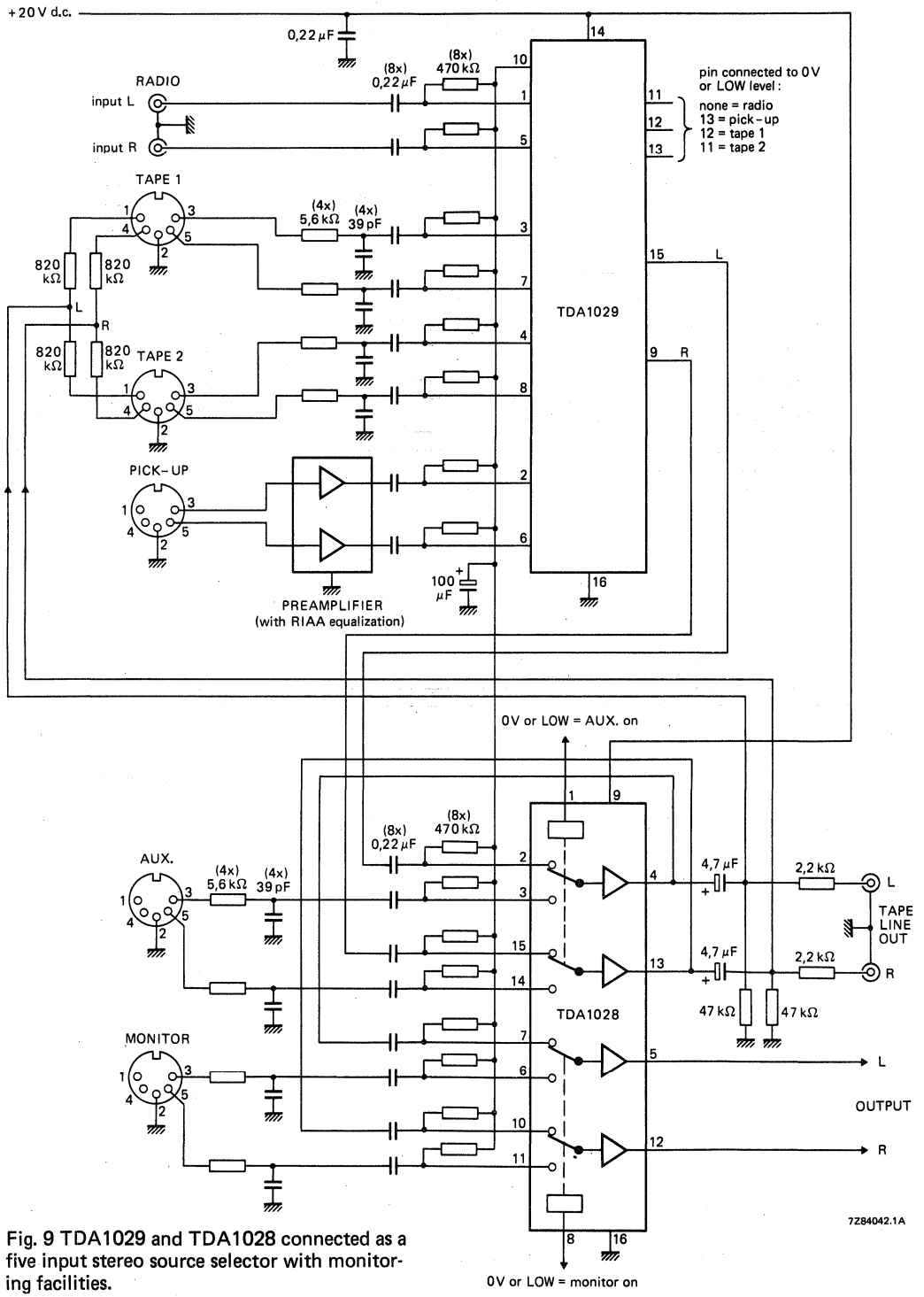


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

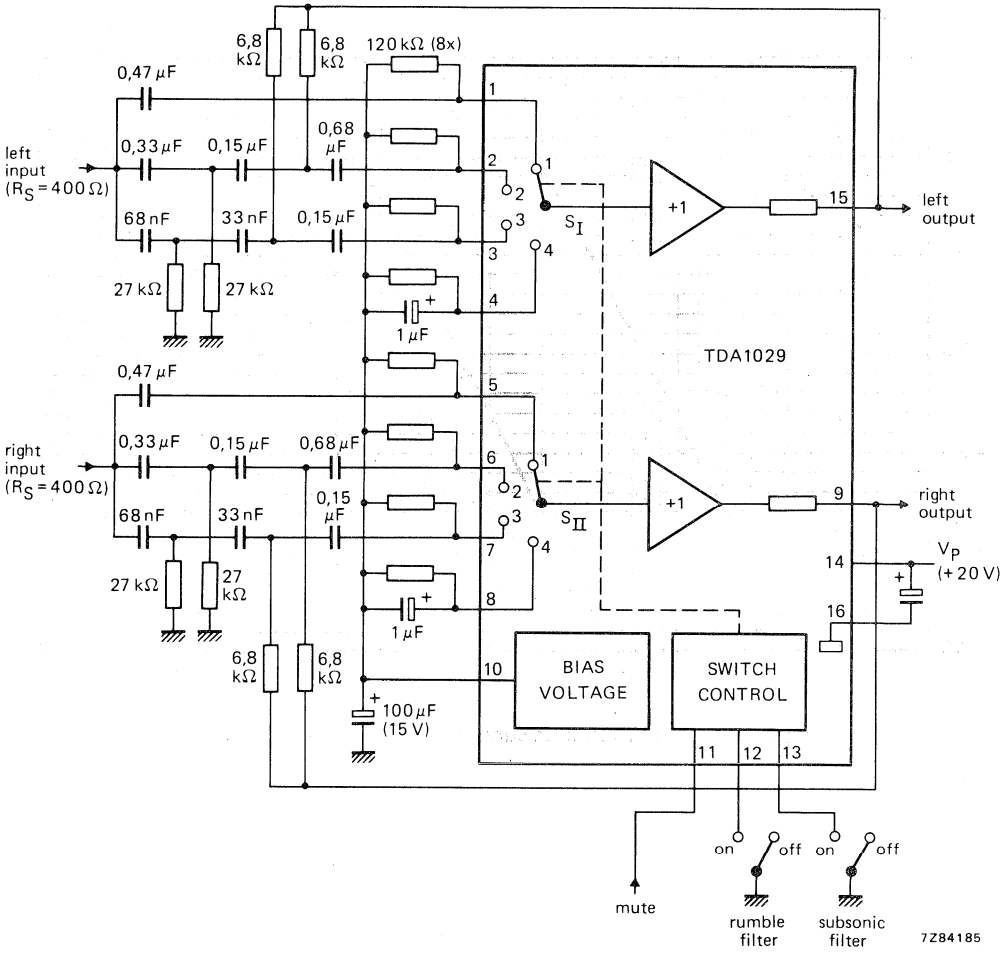


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

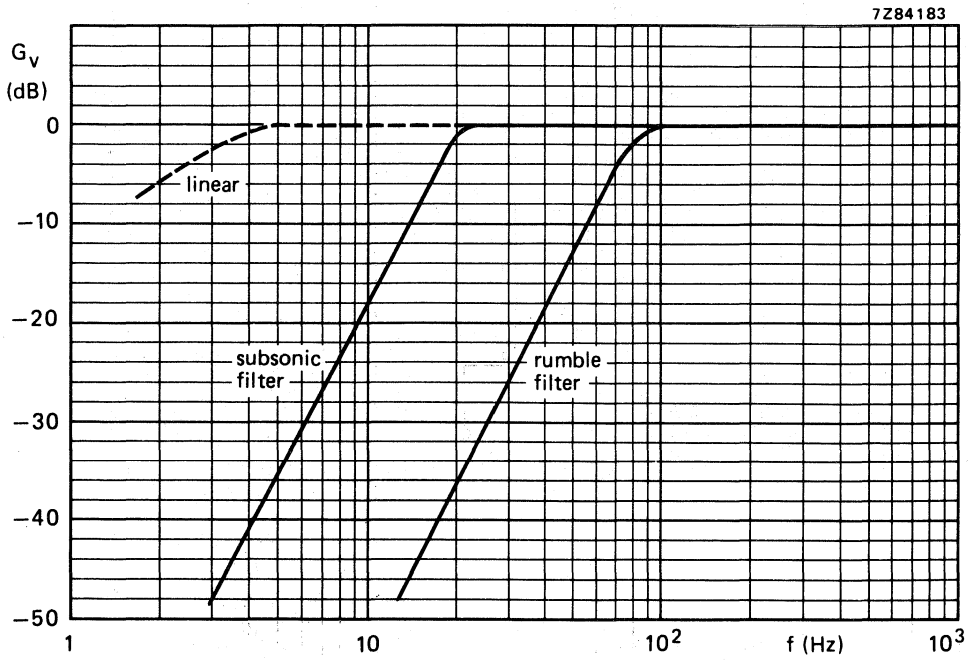


Fig. 11 Frequency response curves for the circuit of Fig. 10.

EAST-WEST CORRECTION DRIVER CIRCUIT

The TDA1082 is a monolithic integrated circuit driving east-west correction of colour tubes in television receivers. The circuit can be used for class-A and class-D operation and incorporates the following functions:

- differential input amplifier
- squaring stage
- differential output amplifier with driver stage
- protection stage with threshold
- switching off the correction during flyback
- voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 1)	V_P	typ.	12	V
Current consumption	I_P	typ.	17	mA
Total power dissipation	P_{tot}	max.	600	mW
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Collector voltage drift external transistor	ΔV_C	typ.	0,7	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

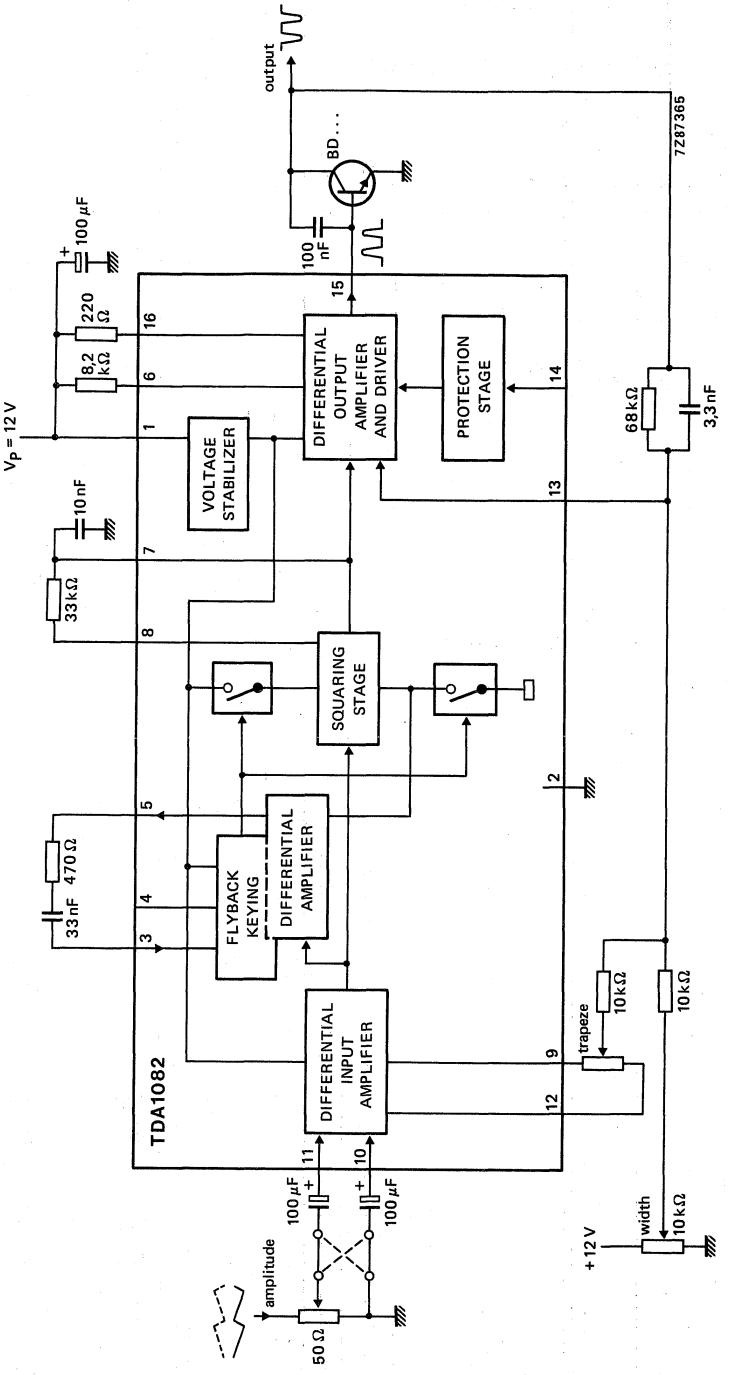


Fig. 1 Block diagram with external components (class-A operation). Also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	V_P	max.	16 V
Output current (pin 15)	$-I_O$	max.	50 mA
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Voltages

with respect to ground (pin 2)	min.	max.	
Pins 1, 5, 7, 8, 9, 12, 13 and 16	0	16	V
Pins 3 and 4	0	−	V
Pins 10, 11 and 15	0	5	V

Currents

Pins 3, 4 and 6	−	5	mA
Pin 14	0	1,5	mA
Pins 15 and 16 ($-I_{15}$ and $+I_{16}$)	0	50	mA

CHARACTERISTICS

V_P = 12 V (range 10,5 to 14 V); T_{amb} = 25; measured in circuit Fig. 1 with colour tube A66-500X; unless otherwise specified

Supply

Voltage range	V_P	10,5	to	14	V
Voltage peak value	V_{PM}	max.		15	V
Current range	I_P	11	to	30	mA
Current typical value	I_P	typ.		17	mA

Sawtooth signal (pin 10 or 11)

Input voltage d.c. value	V_i	typ.		2,5	V
Input resistance	R_i	typ. <		5,6 7,0	kΩ kΩ

Correcting signals (pin 13)

Input voltage d.c. value	V_{13}	typ.		0,6	V
Input current	I_{13}	typ.		0,5	mA

Flyback keying (pin 3)

Input current range	I_3	0,05	to	5	mA
Peak value, d = 5%	I_3	typ.		20	mA

Threshold (pin 14)

Input voltage at I_{14} = 200 μA for switching off the driver stage	V_i	typ. 7,2	to	8 8,8	V V

Output stage (pin 6)			
Generator current	I_6	typ.	1 mA
Flyback differential amplifier (pin 5)			
D.C. value output voltage	V_5	typ.	6 V
Output resistance	R_5	typ.	5,6 kΩ
Squaring stage (pin 7)			
D.C. value output voltage	V_7	typ.	6 V
Peak to peak value output voltage	$V_{7(p-p)}$	typ.	1,5 V
Output resistance	R_7	5,6 to typ.	9,4 kΩ 7,5 kΩ
Correction trapezoidal deformation (pins 9 and 12)			
D.C. voltage	$V_{9,12}$	typ.	5 V
Output resistance	$R_{9,12}$	typ.	7,5 kΩ
Driver output (pin 15)			
Output current	$-I_{15}$	<	50 mA
Drift of d.c. collector voltage			
Of external transistor in closed loop T_{amb} = 15 to 70 °C; V_{CO} = 8 V	ΔV_C	typ.	0,7 V

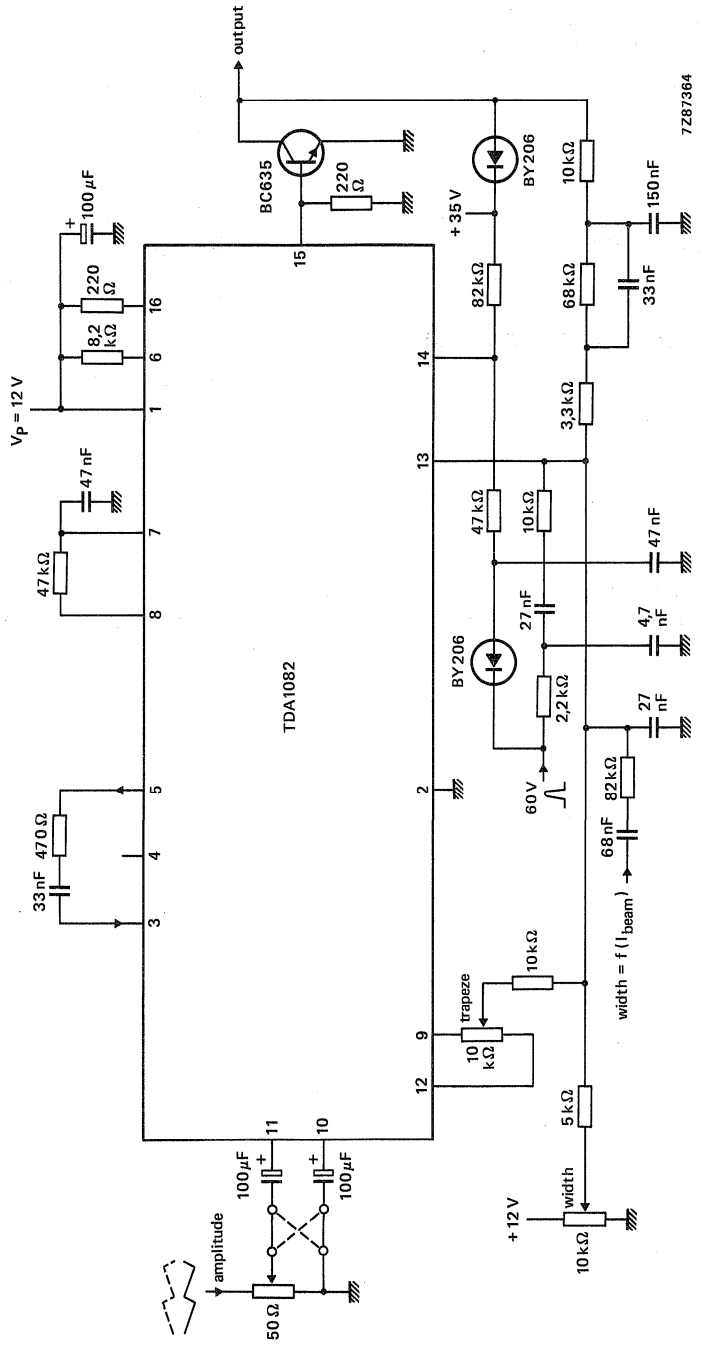


Fig. 2 Application circuit E-W-correction (class-D operation).

12 to 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

PACKAGE OUTLINES

TDA1512A: 9-lead SIL; plastic power (SOT131).
TDA1512AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

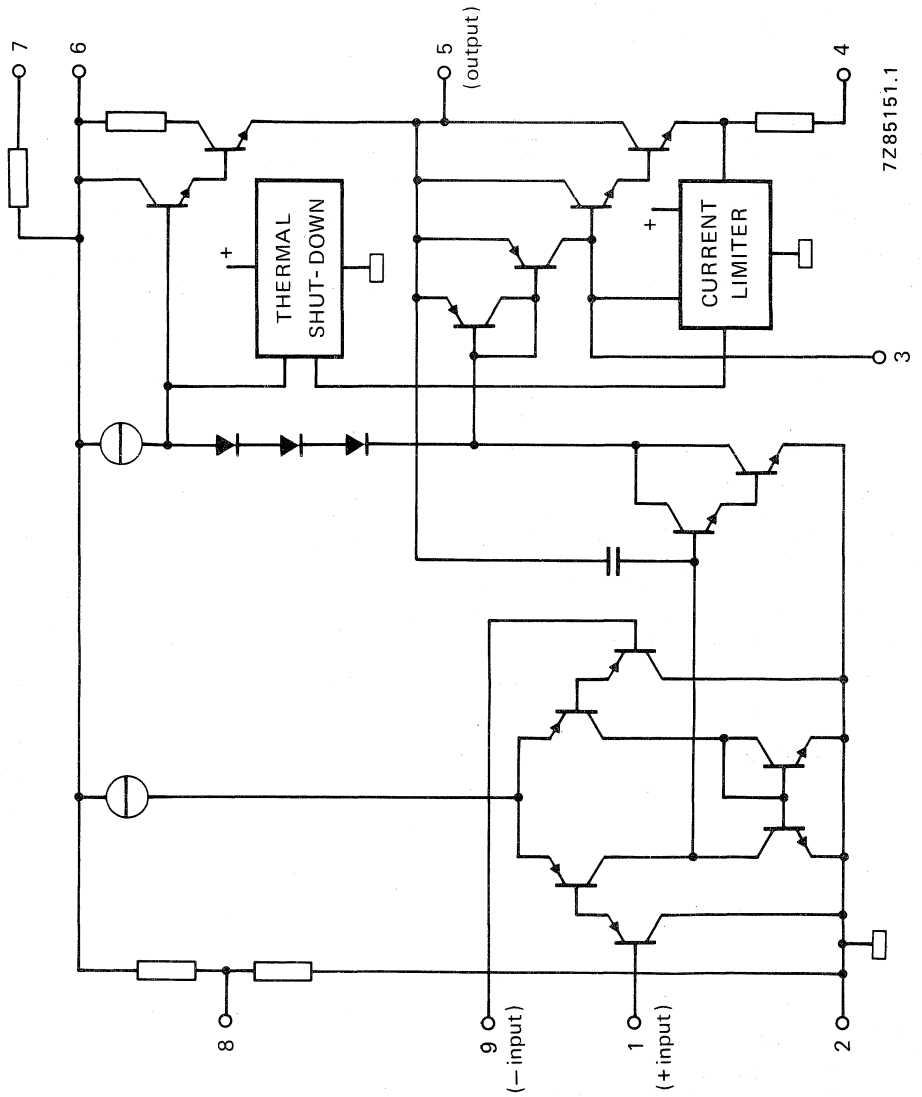


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours

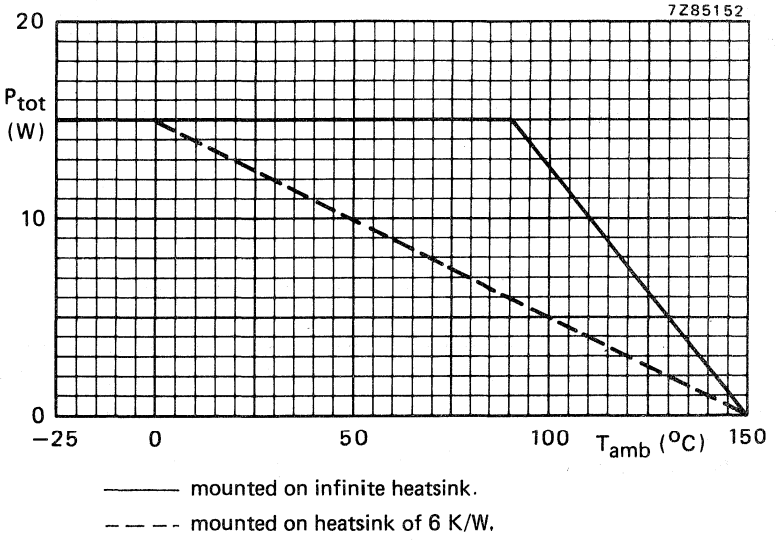


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

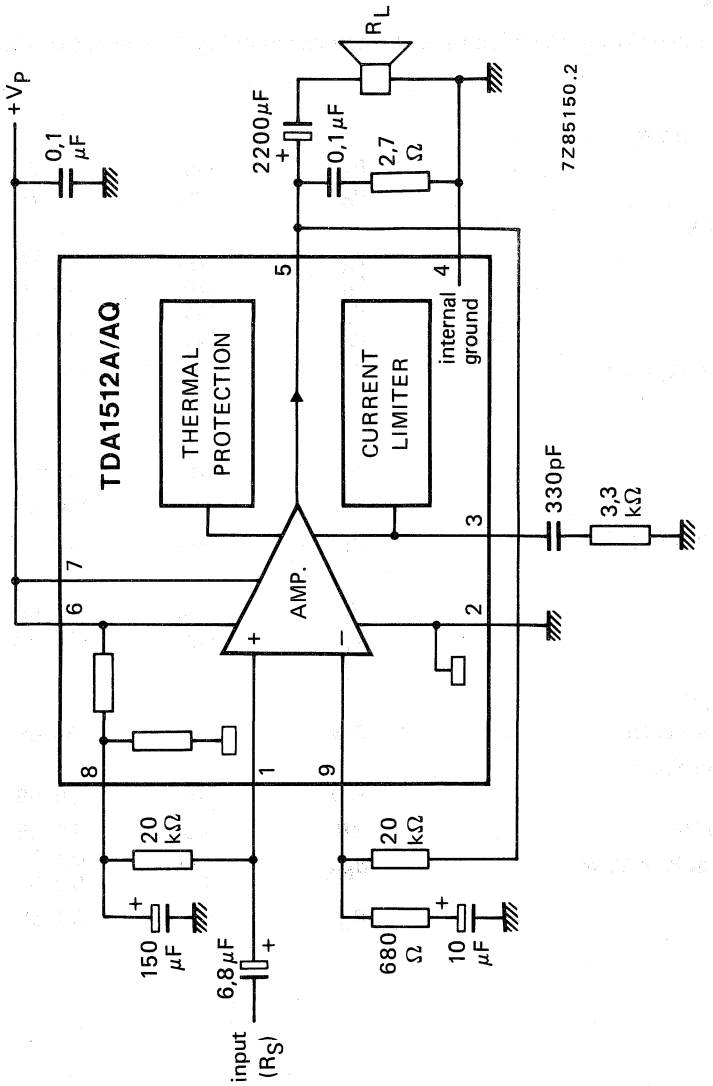


Fig. 3 Test circuit.

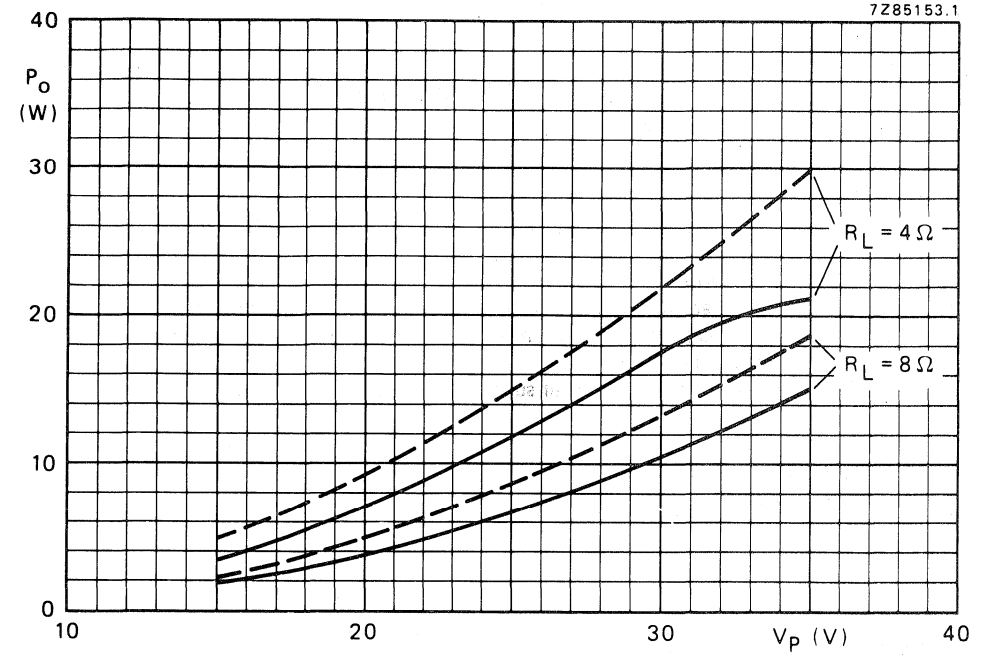


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

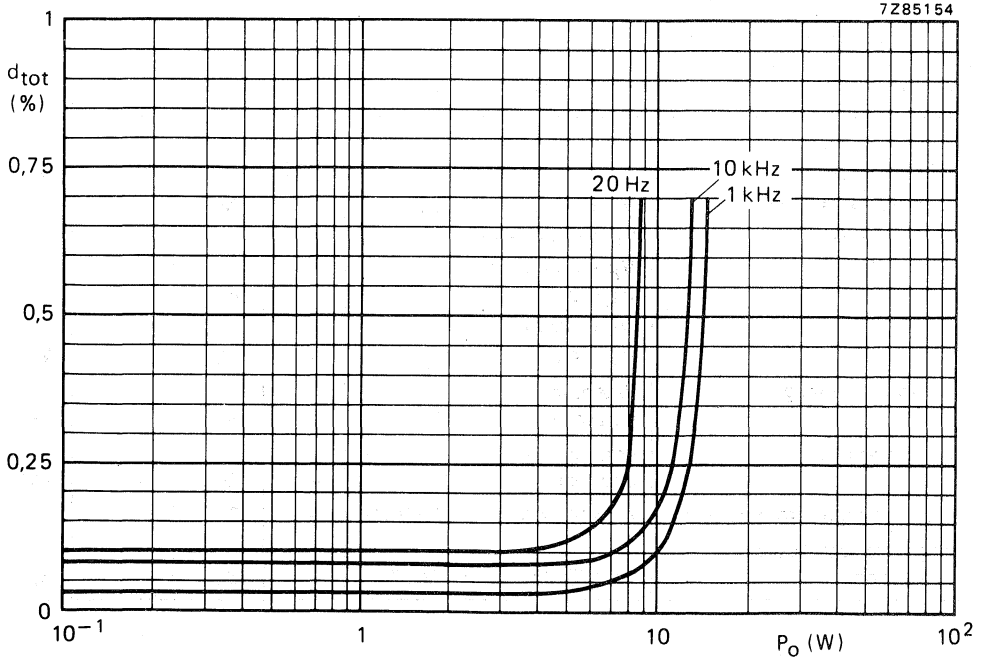


Fig. 5 Total harmonic distortion as a function of the output power.

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	50	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	82	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131A).

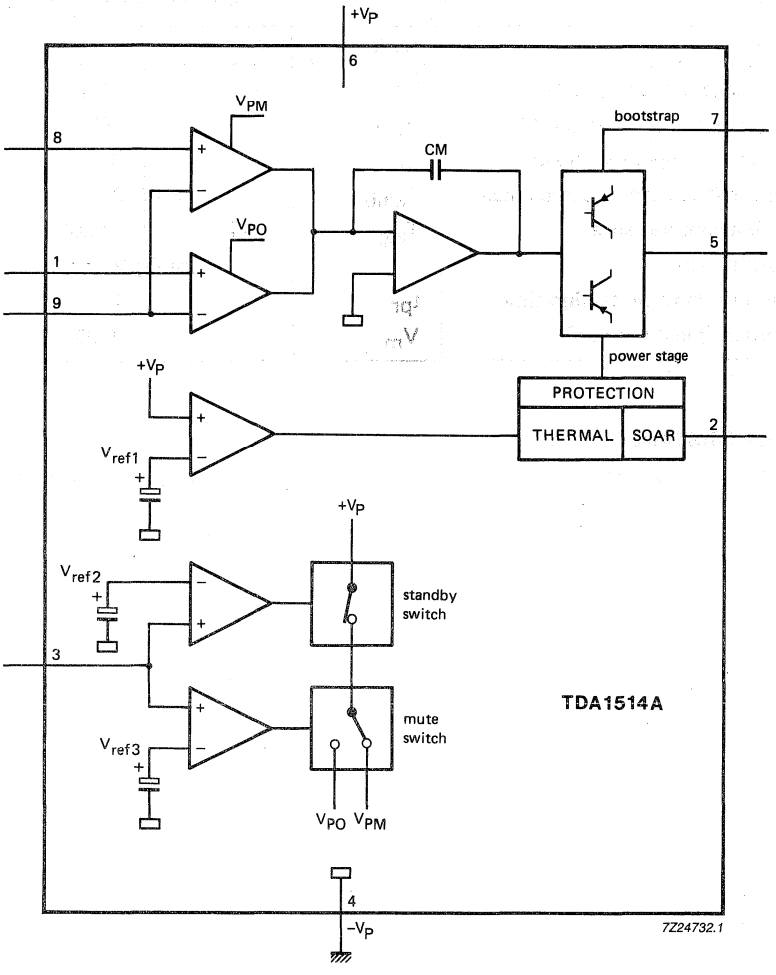


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 4)	V_P	–	±30	V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	–	70	V
Output current (repetitive peak)	I_o	–	8	A
Operating ambient temperature range	T_{amb}	see Fig.2		
Storage temperature range	T_{stg}	–55	+150	°C
Power dissipation		see Fig.2		
Thermal shut-down protection time	t_{pr}	–	1	hour
Mute voltage (pin 3 to pin 4)	V_m	–	7.25	V

THERMAL RESISTANCE

From junction to mounting base $R_{th\ j\text{-}mb}$ max. = 1 K/W

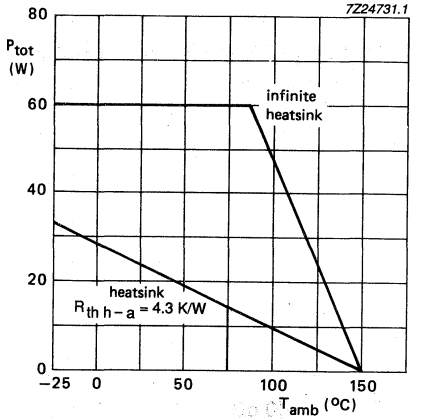


Fig.2 Power derating curve.

The theoretical maximum power dissipation for P_o = 40 W with a stabilized power supply is:

$$\frac{V_P^2}{2\pi^2 R_L} = 19\ W; \text{ where } V_P = \pm 27.5\ V;\ R_L = 8\ \Omega$$

Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C the total thermal resistance is:

$$R_{th\ j\text{-}a} = \frac{150 - 50}{19} = 5.3\ K/W$$

Since the thermal resistance of the SOT131A encapsulation is $R_{th\ j\text{-}mb} < 1$ K/W, the thermal resistance required of the heatsink is $R_{th\ h\text{-}a} < 4.3$ K/W.

SAFE OPERATING AREA (SOAR) PROTECTION

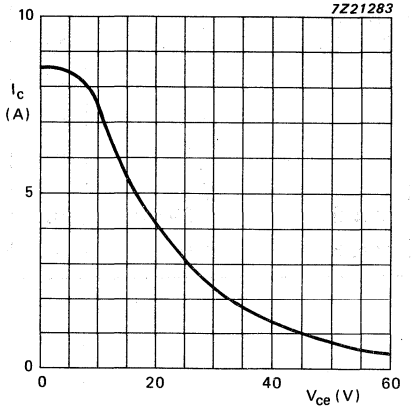


Fig.3 SOAR protection curve.

CHARACTERISTICS

V_P = ± 27.5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; test circuit as Fig.4; unless otherwise specified.

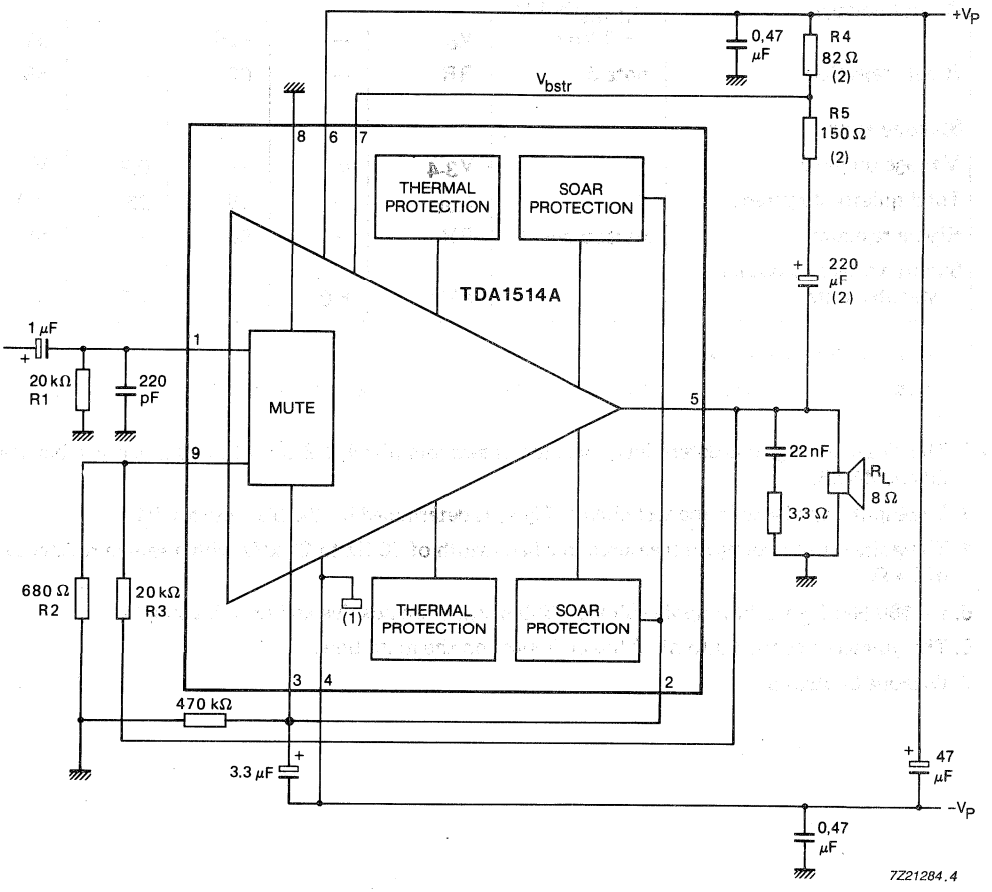
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Maximum output current (peak value)		$I_{OM\,max}$	6.4	–	–	A
Operating state						
Voltage (pins 3 to 4)		V_{3-4}	6	–	7.25	V
Total quiescent current	$R_L = \infty$	I_{tot}	30	56	90	mA
Output power	THD = –60 dB	P_o	37	40	–	W
	THD = –20 dB	P_o	–	51	–	W
Output power	V_P = ± 23 V; THD = –60 dB					
	R_L = 8 Ω	P_o	–	28	–	W
	R_L = 4 Ω	P_o	–	50	–	W
Total harmonic distortion	P_o = 32 W	THD	–	–90	–80	dB
Intermodulation distortion	P_o = 32 W note 1	d_{im}	–	–86	–	dB
Power bandwidth	(–3 dB); THD = –60 dB	B	–	20 to 25 000		Hz
Slew rate		dV/dt	–	14	–	V/μs
Closed loop voltage gain	note 2	G_c	–	30	–	dB
Open loop voltage gain		G_o	–	89	–	dB
Input impedance	note 3	$\|Z_i\|$	1	–	–	MΩ
Signal-to-noise ratio	note 4 P_o = 50 mW	S/N	80	83	–	dB
Output offset voltage		V_o	–	7	200	mV
Input bias current		I_I	–	0.1	1.0	μA
Output impedance		$\|Z_o\|$	–	–	0.1	Ω
Supply voltage ripple rejection	note 5	SVRR	58	64	–	dB
Quiescent current into pin 2	note 6	I_2	–	0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute state						
Voltage on pin 3		V_{3-4}	2	–	4.5	V
Offset voltage		V_o	–	30	200	V
Output voltage	$V_{i(rms)}$ = 1 V f = 1 kHz	V_o	–	450	–	μV
Ripple rejection	note 5	RR	–	60	–	dB
Standby state						
Voltage on pin 3		V_{3-4}	0	–	0.9	V
Total quiescent current		I_{tot}	–	18	25	mA
Ripple rejection	notes 5 and 7	RR	–	60	–	dB
Supply voltage to obtain standby state		$\pm V_P$	5.0	–	7.0	V

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig.4, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig.4) is determined by the bias resistor R1.
4. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistance of 2 kΩ.
5. f = 100 Hz; R_S = 2 kΩ; ripple voltage = 500 $mV_{(eff)}$ on positive and negative supply.
6. The quiescent current into pin 2 has an impact on the mute time.
7. Without bootstrap.



(1) Mounting base connected to $-V_P$.

(2) When used without a bootstrap these components are disconnected and pin 6 is connected to pin 7 thus decreasing the output power by approximately 4 W.

(3) When $R_L = 4\ \Omega$: R4 = 47 Ω and R5 = 82 Ω.

Fig.4 Application and test circuit.

20 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1520B is an integrated hi-fi audio power amplifier designed for use with non-stabilized symmetrical or stabilized asymmetrical power supplies in mains-fed applications (e.g. stereo radio, stereo TV sound and cassette recorder).

Features

- Low offset voltage at output (suitable for BTL application)
- Low cross-over and secondary cross-over distortion
- Low intermodulation and transient intermodulation distortion
- Low harmonic distortion
- Good hum suppression
- High slew rate
- No switch-on/switch-off plop
- Thermal protection

QUICK REFERENCE DATA (note 1)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_{tot}	22	60	105	mA
Output power at THD = 0,5%		P_O	20	22	–	W
Input impedance		Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O = 50 mW	note 2	(S+N)/N	70	75	–	dB
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB

Notes to the Quick Reference Data

1. All values measured from test circuit Fig.6; V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.
2. Bandwidth is 20 Hz to 20 kHz; R_S = 2 kΩ (RMS value).

PACKAGE OUTLINES

TDA1520B: 9-lead SIL; plastic power (SOT131).
TDA1520BQ: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

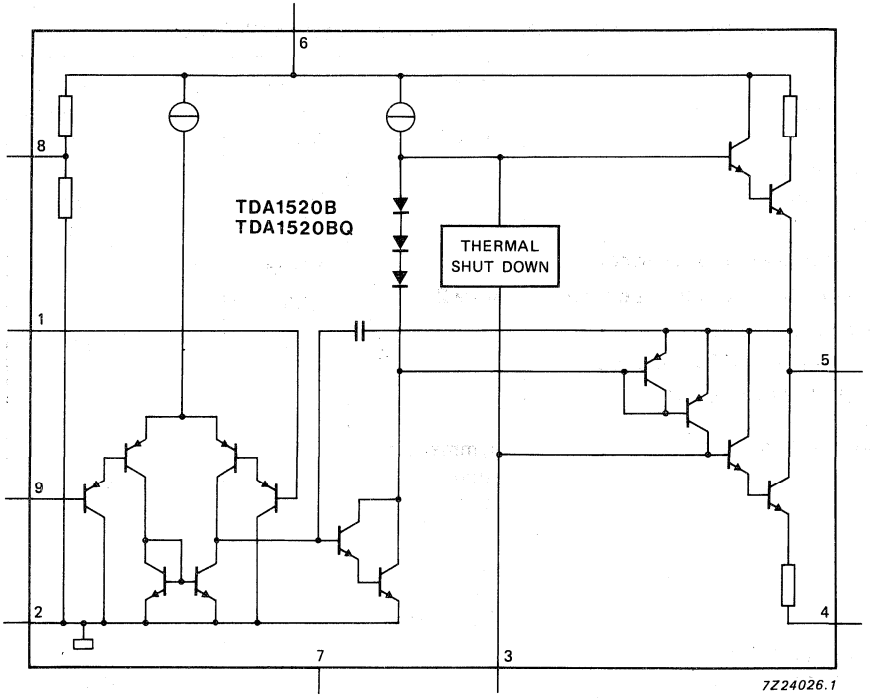


Fig. 1 Block diagram.

PINNING

1 Non-inverting input
2 Input ground (substrate)
3 Compensation
4 Negative supply (ground)
5 Output
6 Positive supply (V_P)
7 Not connected
8 Supply voltage ripple rejection
9 Inverting input (feedback)

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	note 1	V_P	–	50	V
Input voltage					
pins 1 to 2		V_I	–	25	V
pins 9 to 2		V_I	–	25	V
Repetitive peak output current		I_{ORM}	–	4	A
Non-repetitive peak output current	note 2	I_{OSM}	–	5	A
Total power dissipation		P_{tot}	see Fig.2		
AC short-circuit time of the load impedance during signal drive at					
$V_P = \pm 20$ V	symmetrical supply; $R_S = 2\ \Omega$; $f = \geqslant 20$ Hz	T_{sc}	–	1	hour
$V_P = 30$ V	asymmetrical supply; $R_S = 4\ \Omega$	T_s	–	1	hour
Operating ambient temperature range		T_{amb}	see Fig.2		
Storage temperature range		T_{stg}	–55	+ 150	°C

Notes to the Ratings

1. Minimum rise time of the supply must be $\geqslant 20$ ms.
2. Maximum peak current is defined by the internal protection circuits.

POWER DISSIPATION AND HEATSINK INFORMATION

The maximum theoretical power dissipation with a stabilized power supply is ($V_P = 33$ V and $R_L = 4\ \Omega$):

$$\frac{V_P^2}{2\,\pi^2\,R_L} = 13.8\,\text{W}.$$

Worst case power dissipation with a non-stabilized power supply is (regulation factor of 15%; over voltage of 10% and R_L min. = 0.8 x R_L typ.; V_{PL} is the loaded supply voltage):

$$\frac{(1.1 \times V_{PL})^2}{2\,\pi^2\,R_L\,\text{min.}} = 23.4\,\text{W}.$$

With a maximum ambient temperature of 50 °C and a maximum crystal temperature of 150 °C, the required thermal resistance is:

$$R_{th\,j\text{-}a} = \frac{150 - 50}{23.4} = 4.3\,\text{K/W}.$$

The thermal resistance of the encapsulation is $\leqslant 2.5$ K/W, therefore the thermal resistance of the heatsink must be < 1.8 K/W.

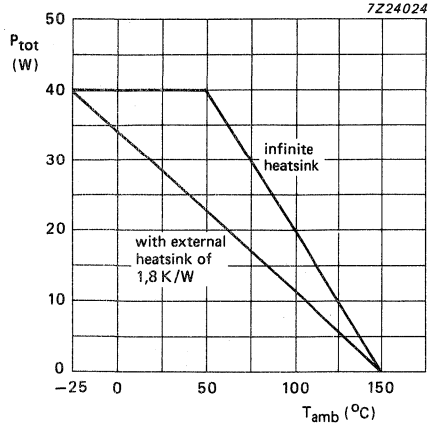


Fig.2 Power derating curve.

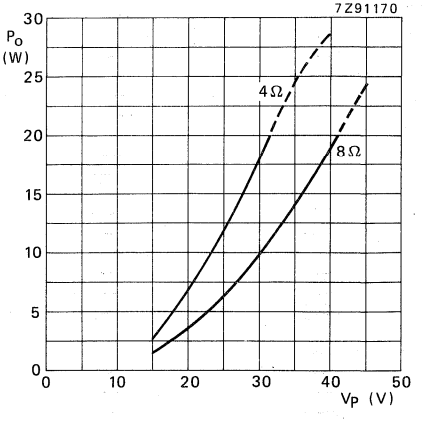


Fig. 3 Output power (P_O) as a function of supply voltage (V_P); f = 1 kHz; d_{tot} = 0.5%; G_V = 30 dB.

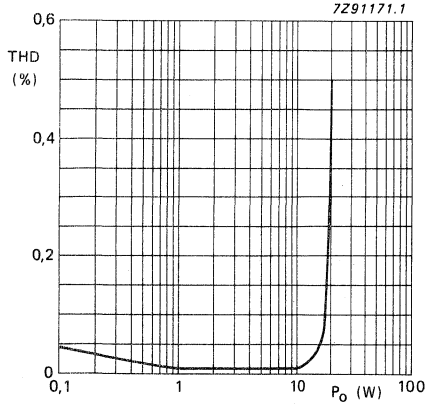


Fig. 4 Total harmonic distortion (THD) as a function of output power (P_O); V_P = 33 V; R_L = 4 Ω; f = 1 kHz.

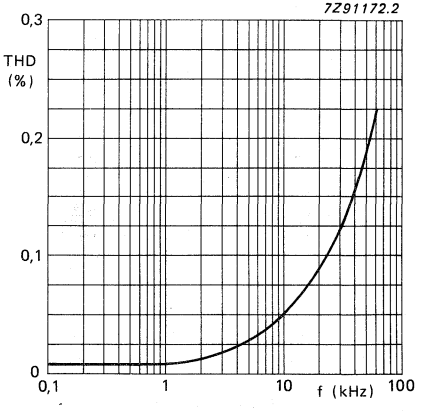


Fig. 5 Total harmonic distortion (THD) as a function of operating frequency (f); V_P = 33 V; R_L = 4 Ω; P_O = 10 W (constant).

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	15	–	50	V
Total quiescent current		I_P	22	60	105	mA
Peak output current		I_{OM}	–	–	3,2	A
Power output at THD = 0.5%	note 1	P_O	20	22	–	W
Total harmonic distortion at P_O = 12 W	note 1	THD	–	0.01	0.1	%
Power bandwidth at THD = 0.5%	P_O = 50 mW to 10 W	B	–	20 to 20 000	–	Hz
Input voltage at P_O = 20 W	note 2	V_I	225	290	325	mV
Input impedance	note 3	Z_I	1000	–	–	kΩ
Signal plus noise to noise ratio at P_O at 50 mW	note 4	(S+N)/N	70	75	–	dB
Offset voltage		$\lvert V_{5\text{-}8} \rvert$	0	± 10	± 100	mV
Input offset current		I_{os}	–	0	1	μA
Output impedance		Z_O	–	–	0.1	Ω
Supply voltage ripple rejection at R_S = 0 Ω	f = 100 Hz	SVRR	45	60	–	dB
	f = 10 kHz	SVRR	45	80	–	dB
Intermodulation distortion at P_O = 10 W		d_{IM}	–	0.02	–	%
Transient intermodulation distortion	note 5	d_{TIM}	–	0.01	–	%
Slew rate		SR	–	6	–	V/μs

Notes to the Characteristics

1. Output power is measured directly at the output pin.
2. The closed-loop gain is determined by external resistors and is variable between 20 to 40 dB.
3. Input impedance in the test circuit is determined by the bias resistor R.
4. Unweighted noise measured in a bandwidth of 20 Hz to 20 kHz at R_S = 2 kΩ.
5. The transient intermodulation distortion is measured at P_O = 10 W. The input signal is a 3.18 kHz square-wave signal mixed with a 15 kHz sine-wave signal and a peak-to-peak voltage ratio of 4:1.

APPLICATION INFORMATION

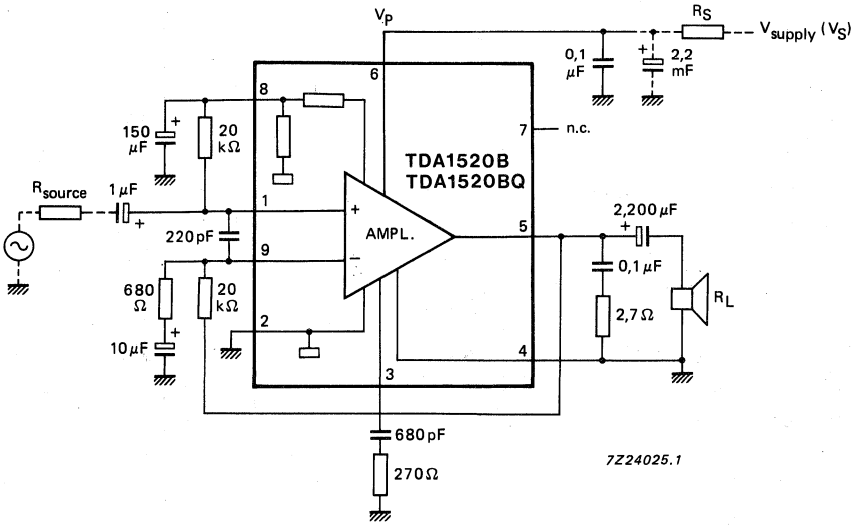


Fig. 6 Test and application diagram.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_o	typ. 12	W
Voltage gain	G_v	typ. 30	dB
Gain balance between channels	ΔG_v	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

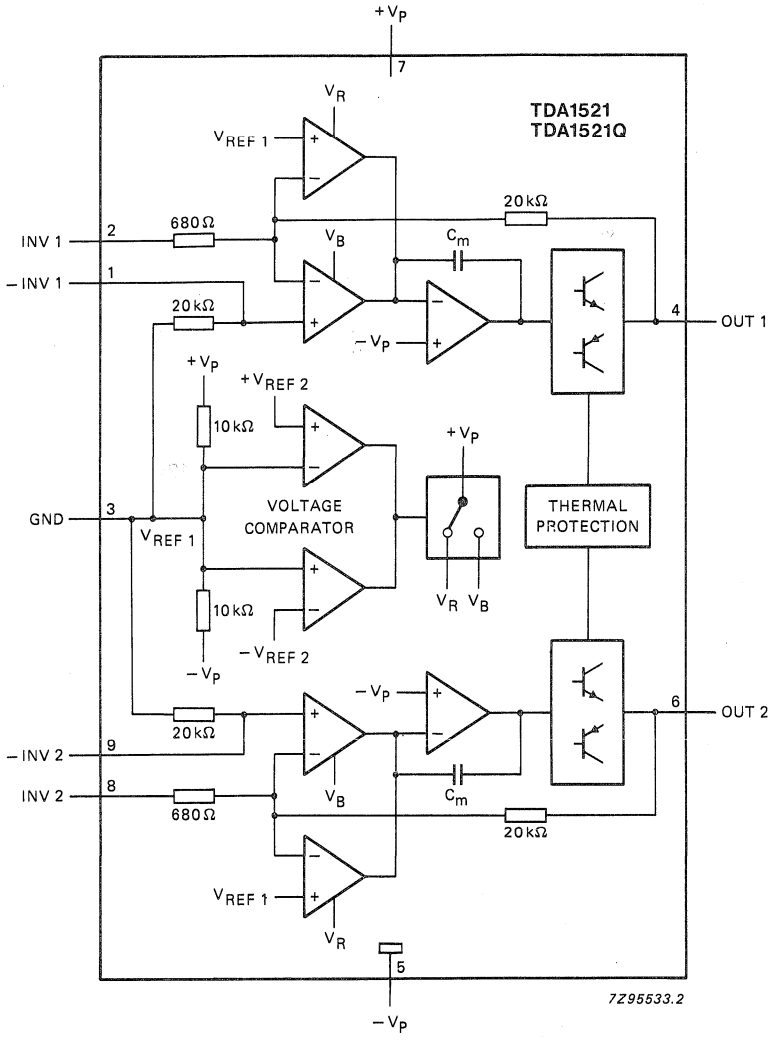


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	–20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

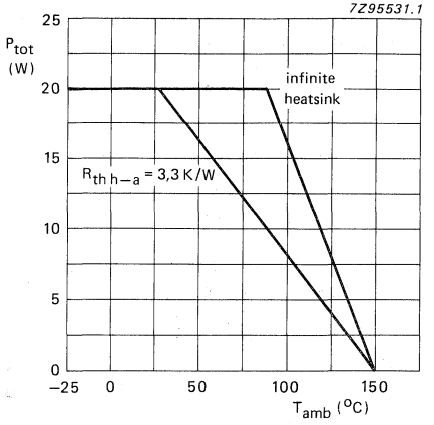


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 2{,}5$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 16$ V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14{,}6} - 2{,}5 = 3{,}3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_P$)

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

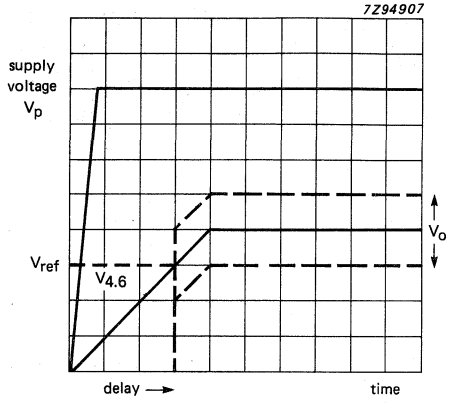


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

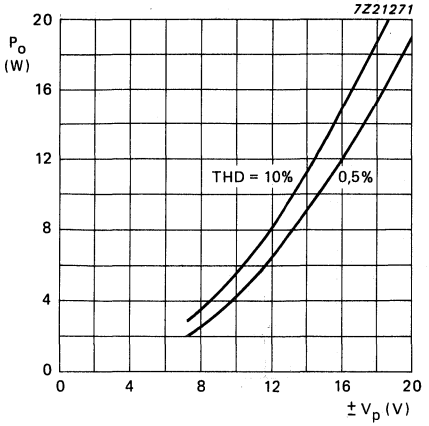


Fig. 4 Output power as a function of supply voltage, symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

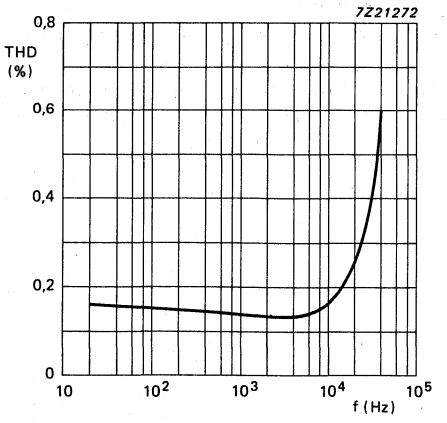


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_o = 6$ W.

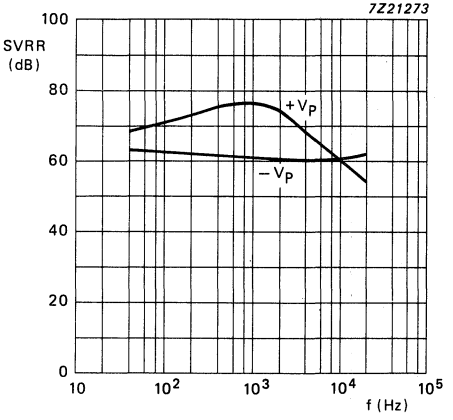


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

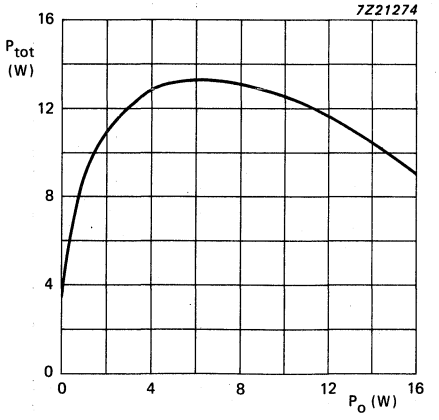


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

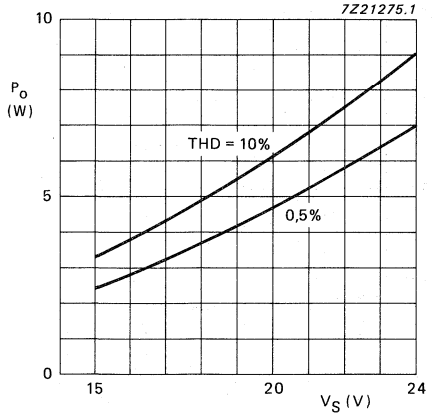


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

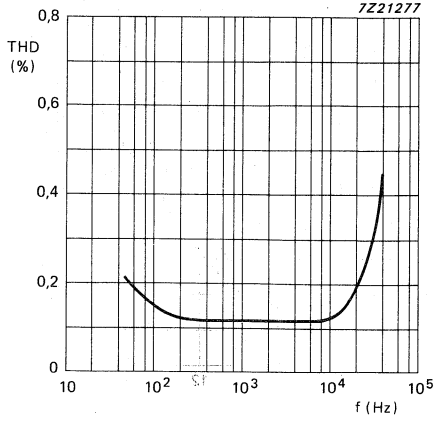


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 4$ W.

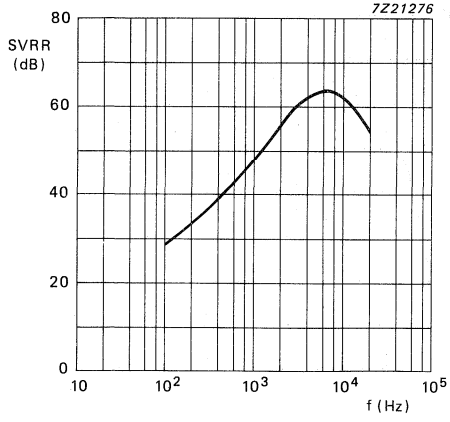


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

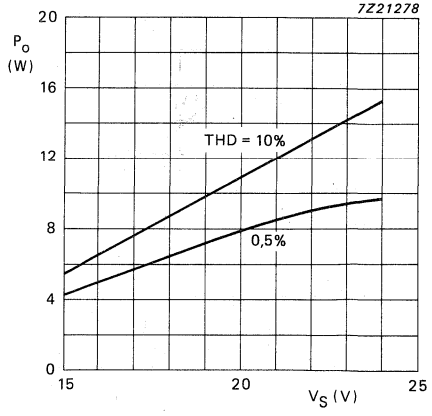
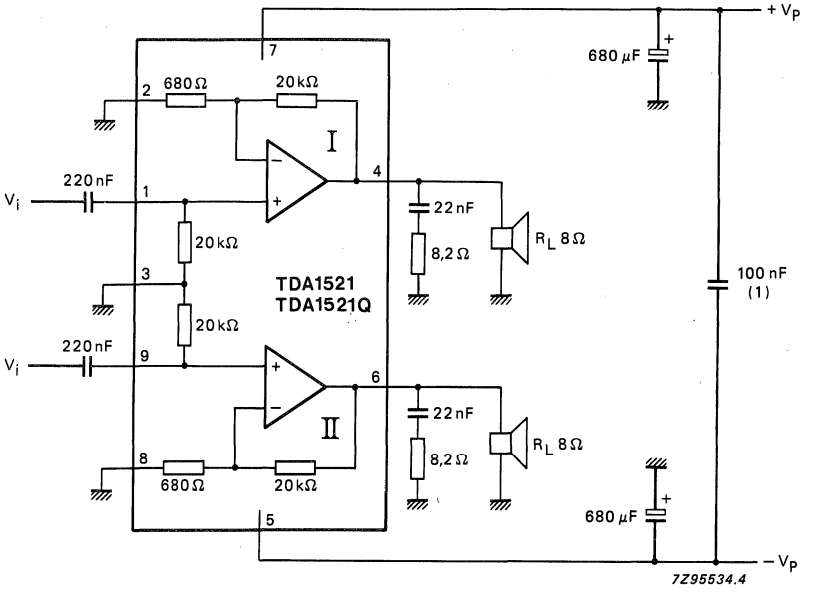
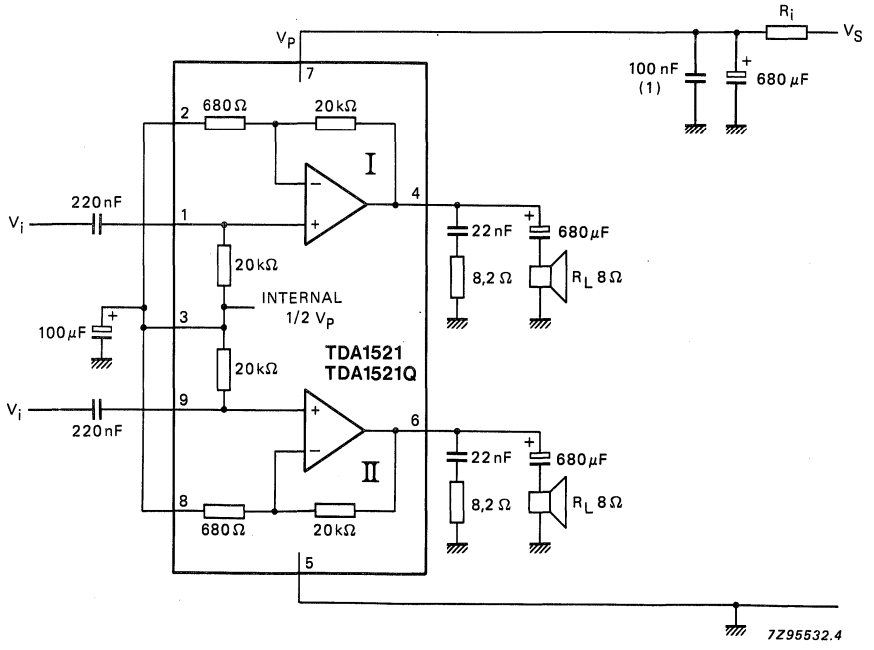


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4\ \Omega$; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

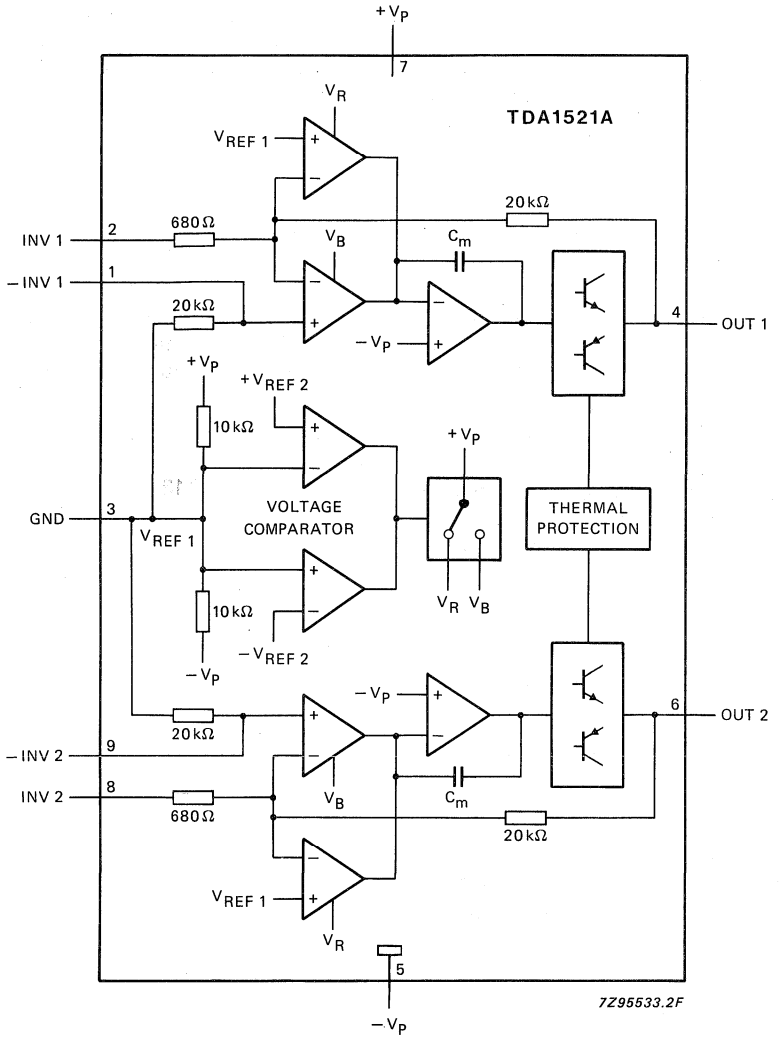


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ V_P (asymmetrical)
4	OUT1	output 1
5	$-V_P$	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	$+V_P$	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

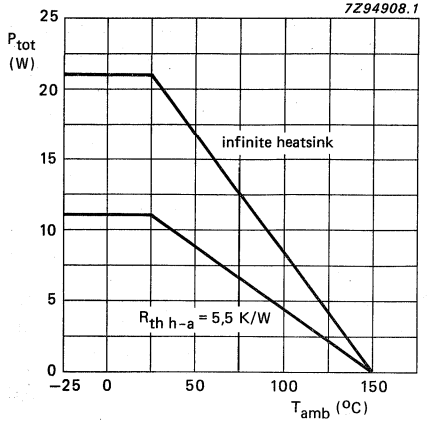


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,5	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	40	50	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

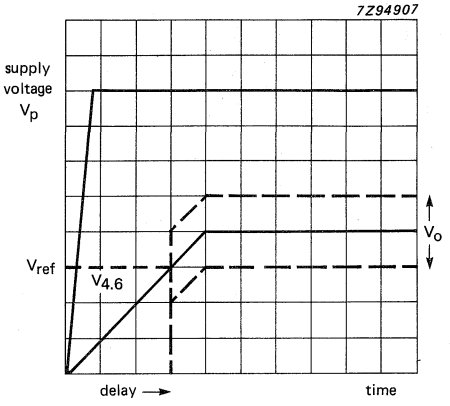


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

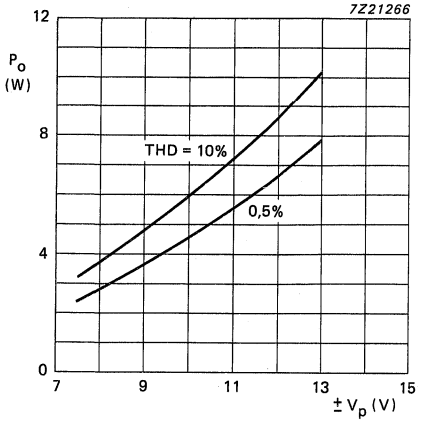


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

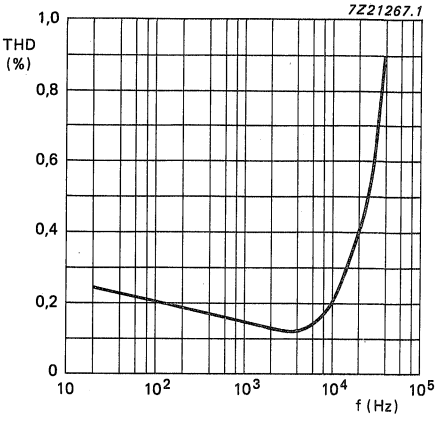


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_p = \pm 12$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

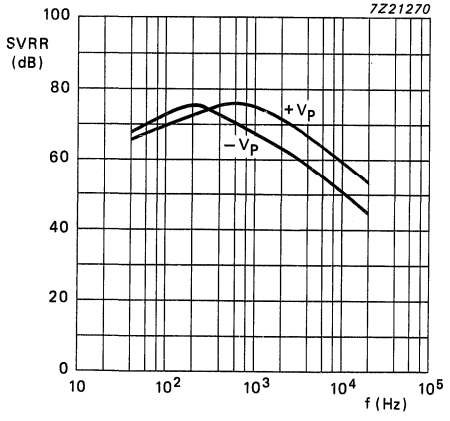


Fig. 6 Supply voltage ripple rejection; symmetrical supply, $V_p = \pm 12$ V; $V_{RR} = 200$ mV.

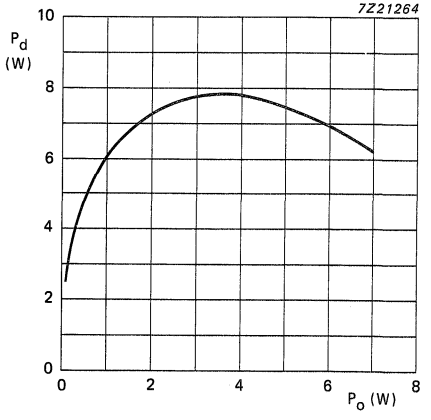


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; f = 1 kHz.

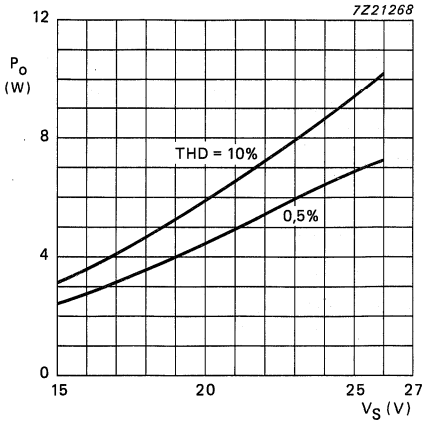


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

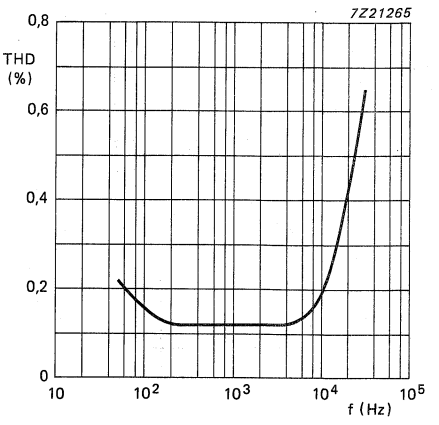


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

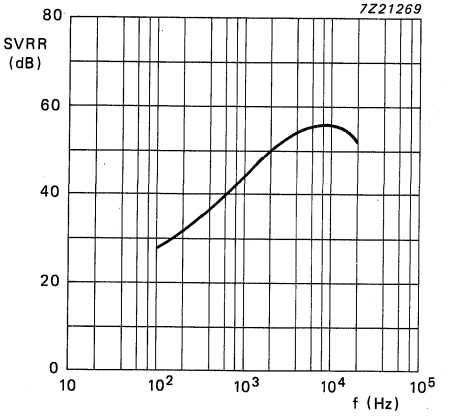
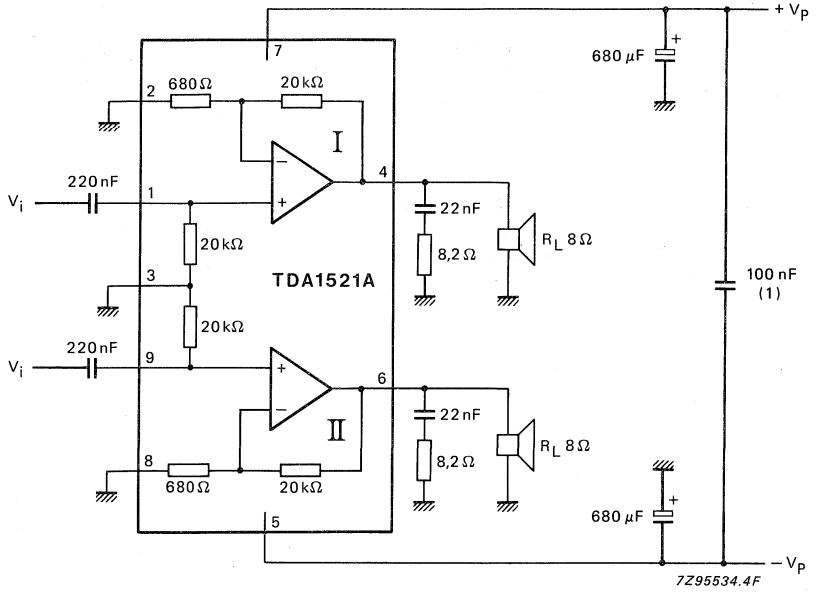


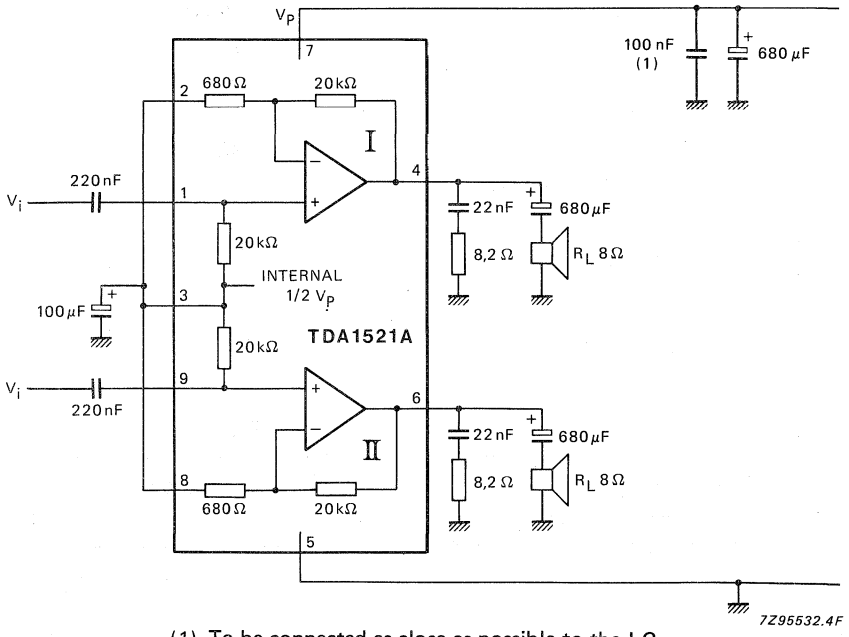
Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

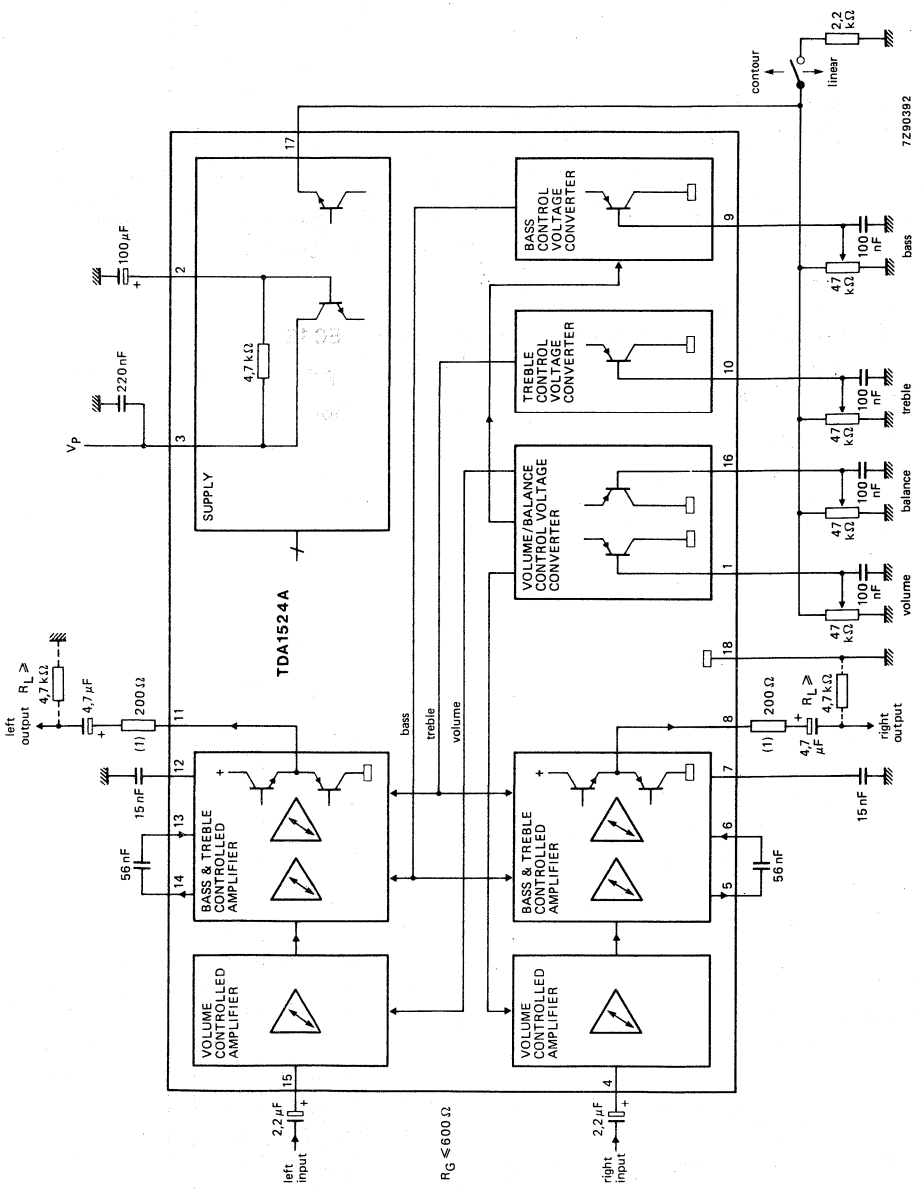
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_v		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_v		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_v = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_v = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_v = −20 to + 26 dB	ΔG_v	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

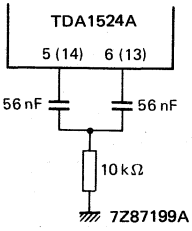


Fig. 2 Double-pole low-pass filter for improved bass-boost.

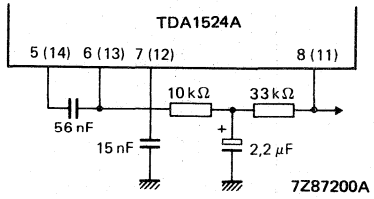


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−30 to + 80	°C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8{,}5$ V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2 - V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\ max}$	20,5	21,5	23	dB
Volume control range; $G_{V\ max}/G_{V\ min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	−40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	−19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to −26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15) at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

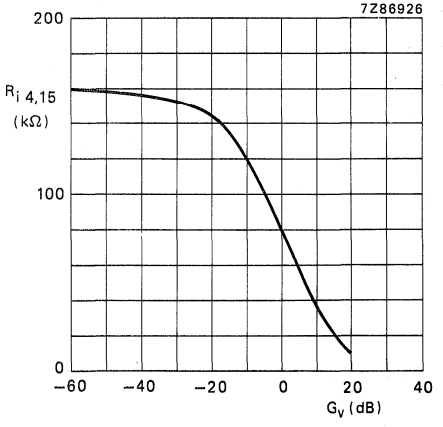


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

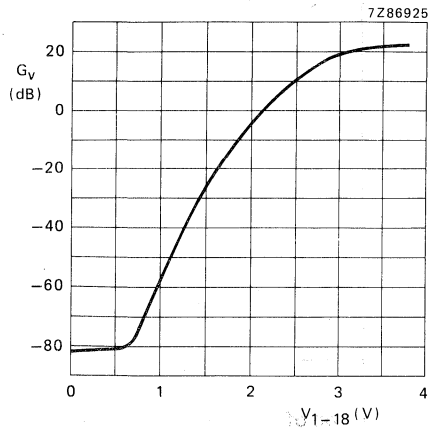


Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

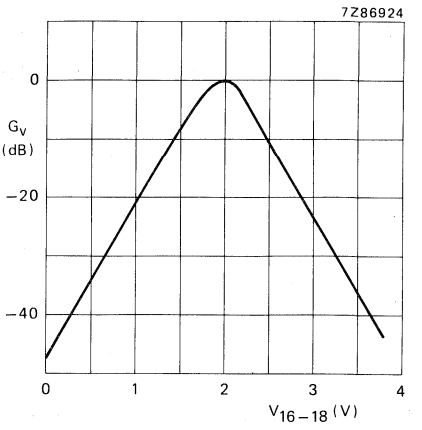


Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

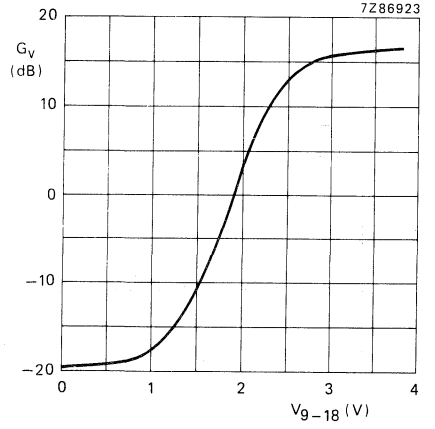


Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

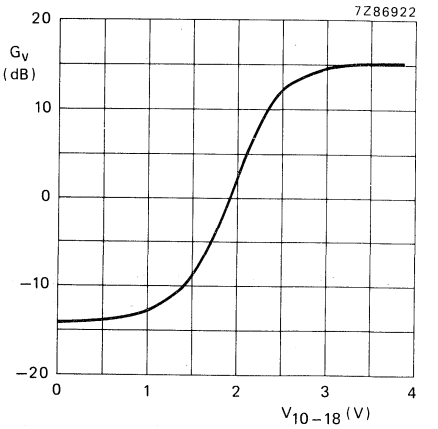


Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

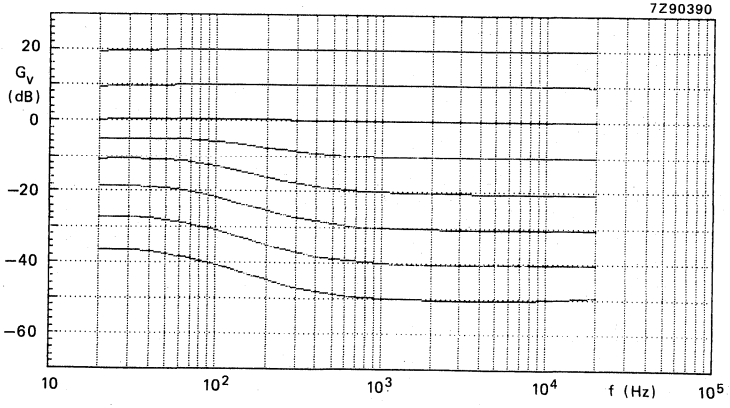


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

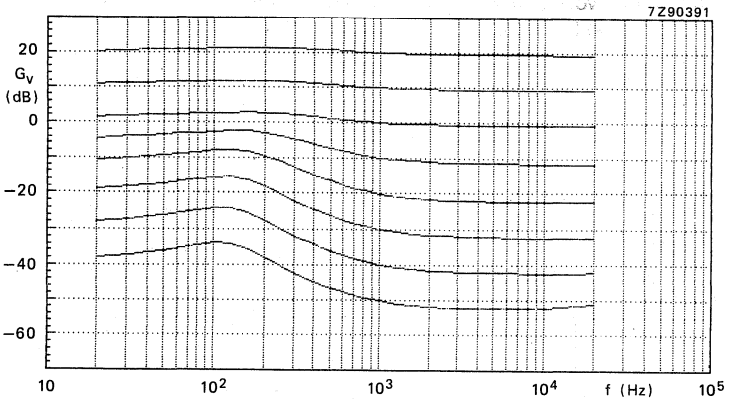


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

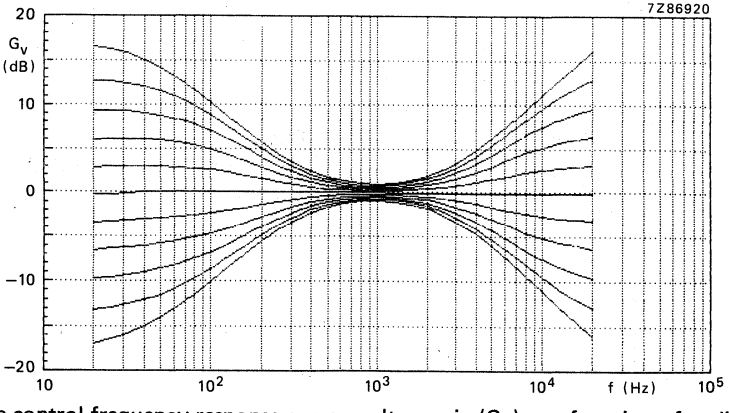


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

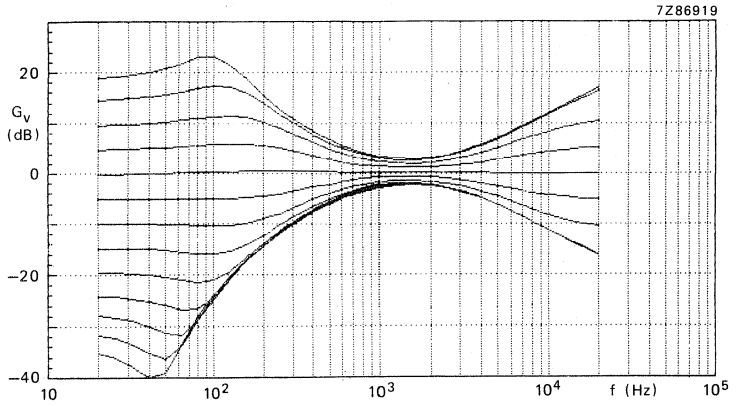


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

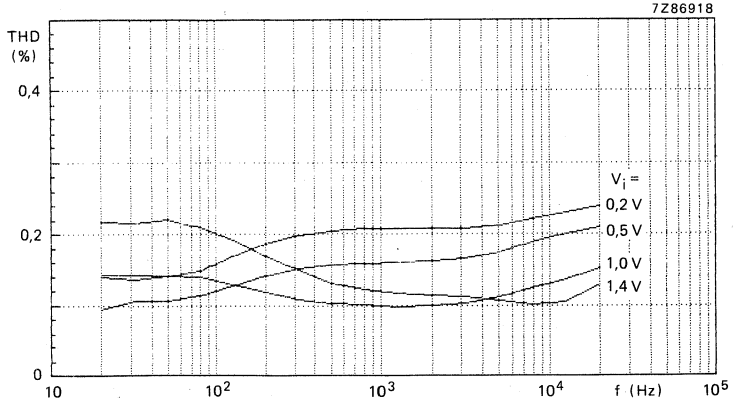


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

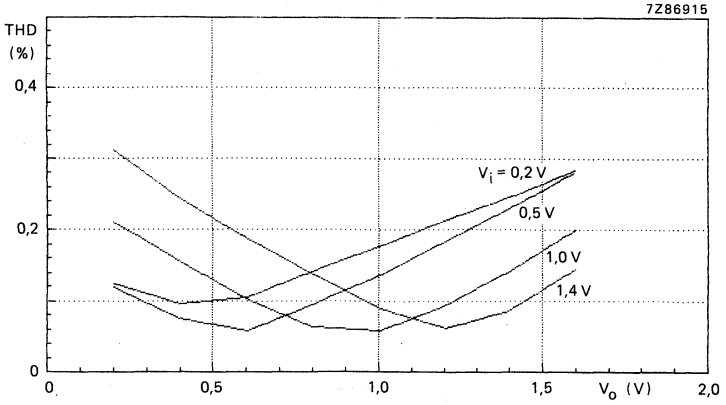
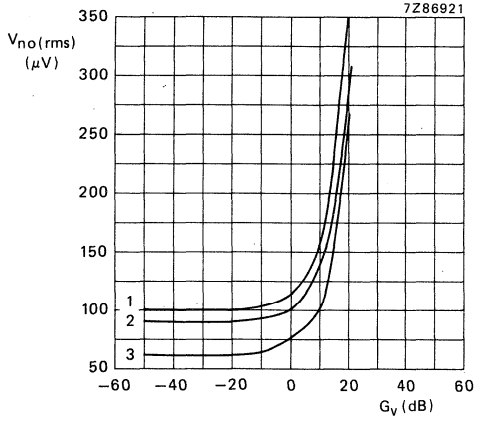


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_o). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_v). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The TDA1525 is an active stereo tone/volume control for car radios, television receivers and mains-fed audio equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

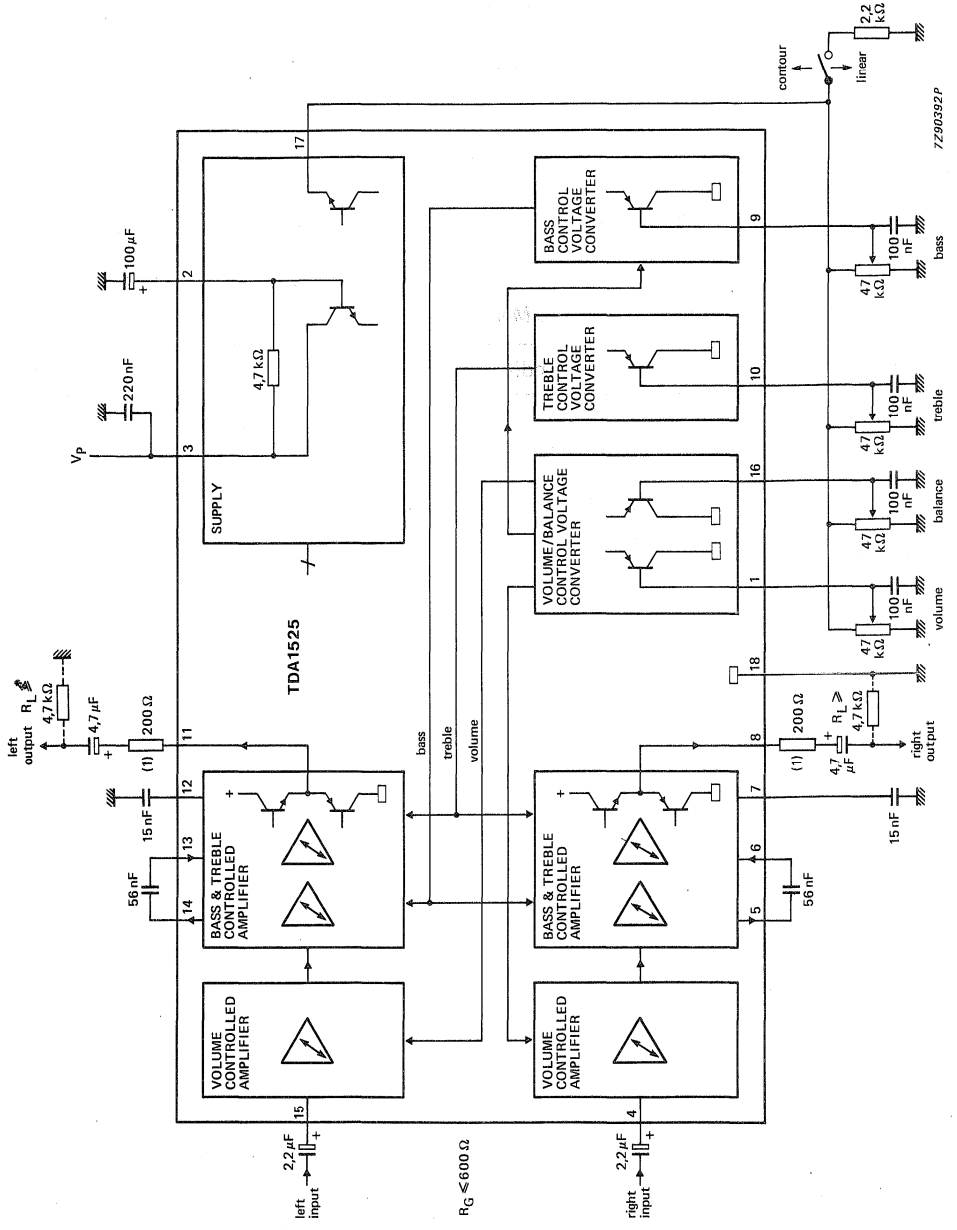
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-18}$	7.5	12	16.5	V
Supply current		I_3	–	35	–	mA
Maximum input signal with DC feedback (RMS value)		$V_{i(rms)}$	–	2.5	–	V
Maximum output signal with DC feedback (RMS value)		$V_{o(rms)}$	–	3.0	–	V
Volume control range		ΔG_v	–80	–	+ 21.5	dB
Bass control range	at 40 Hz	ΔG_v	–	–19 to +17	–	dB
Treble control range	at 16 kHz	ΔG_v	–	± 15	–	dB
Total harmonic distortion		THD	–	0.3	–	%
Output noise voltage (RMS value)	unweighted; f = 20 Hz to 20 kHz; V_P = 12 V					
for maximum voltage gain		$V_{no(rms)}$	–	310	–	μV
for voltage gain = –40 dB		$V_{no(rms)}$	–	100	–	μV
Channel separation	G_v = –20 to + 21.5 dB	α_{cs}	–	60	–	dB
Tracking between channels	G_v = –20 to + 26 dB	ΔG_v	–	–	2.5	dB
Ripple rejection	f = 100 Hz	RR	–	50	–	dB
Operating ambient temperature range		T_{amb}	–40	–	+ 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

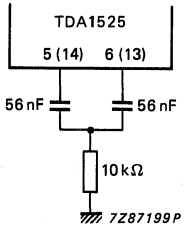


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3\text{-}18}$	–	18	V
Total power dissipation		P_{tot}	–	1200	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

$V_P = V_{3\text{-}18} = 12$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L > 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_3$	7.5	12	16.5	V
Supply current	V_P = 8.5 V	I_3	19	27	35	mA
	V_P = 9.7 V	I_3	–	–	40	mA
	V_P = 12.0 V	I_3	25	35	45	mA
	V_P = 15.0 V	I_3	30	43	56	mA
DC input levels (pins 4 and 15)	V_P = 8.5 V	$V_{4,15}$	3.8	4.25	4.7	V
	V_P = 12.0 V	$V_{4,15}$	5.3	5.9	6.6	V
	V_P = 15.0 V	$V_{4,15}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11)	all control voltage conditions					
	V_P = 8.5 V	$V_{8,11}$	3.3	4.25	5.2	V
	V_P = 12.0 V	$V_{8,11}$	4.6	6.0	7.4	V
	V_P = 15.0 V	$V_{8,11}$	5.7	7.5	9.3	V
Potentiometer supply voltage output (pin 17)	V_P = 8.5 V	V_{17}	3.25	3.6	3.85	V
Contour on/off switch (control by I_{17})						
contour	switch open	$-I_{17}$	–	–	0.5	mA
linear	switch closed	$-I_{17}$	1.5	–	10.0	mA
Application without potentiometer supply from pin 17 (contour cannot be switched off); voltage range forced to pin 17	$V_P \geqslant 10.8$ V	V_{17}	4.5	–	$\frac{V_P}{2} - V_{BE}$	V
DC voltage range for volume, bass, treble and balance controls (pins 1, 9, 10 and 16 respectively)	V_{17} = 5.0 V	$V_{1,9,10,16}$	1.0	–	4.25	V
	using supply from pin 17	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current to pins 1, 9, 10 and 16		$-I_{1,9,10,16}$	–	–	5.0	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; all voltages are with reference to pin 18; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Control range						
Max. gain (volume)	see Fig. 4	$G_{v\,max}$	20.5	21.5	23.0	dB
Volume control range	$G_{v\,max}/G_{v\,min}$	ΔG_v	90	100	–	dB
Balance control range	G_v = 0 dB; see Fig. 5	ΔG_v	–	–40	–	dB
Bass control range	f = 40 Hz; see Fig. 6	ΔG_v	± 12	–19 to +17	–	dB
Treble control range	f = 16 kHz; see Fig. 7	ΔG_v	± 12	± 15	–	dB
Contour characteristics			see Figs 8 and 9			
Input signals (pins 4 and 15)						
Input resistance with volume control gain	note 1					
at 20 dB	G_v = 20 dB	$R_{i4,\,15}$	10	–	–	kΩ
at –40 dB	G_v = –40 dB	$R_{i4,\,15}$	–	160	–	kΩ
Output signals (pins 8 and 11)						
Output resistance		$R_{o8,\,11}$	–	–	300	Ω
Signal processing						
Power supply ripple rejection	$V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_v = 0 dB	RR	35	50	–	dB
Channel separation	250 Hz to 10 kHz; G_v = –20 to + 21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with constant control voltage	$V_1 = V_{17}/2$	ΔG_v	–	–	± 3	dB
Gain tolerance between left and right channels	$V_1 = V_{16} = V_{17}/2$	ΔG_{vL-R}	–	–	1.5	dB
Tracking between channels	G_v = 21.5 to –26 dB; f = 250 Hz to 6.3 kHz; balance adjusted for G_v = 10 dB	ΔG_v	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Signal handling						
Input signal handling (RMS value)	V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 8.5 V; THD = 0.7%; f = 1 kHz	$V_{i(rms)}$	1.8	2.4	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 12 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	1.4	–	–	V
	V_P = 15 V; THD = 0.7%; f = 40 Hz to 16 kHz	$V_{i(rms)}$	2.0	3.2	–	V
Output signal handling (RMS value)	notes 2 and 3; V_P = 8.5 V; THD = 0.5%; f = 1 kHz	$V_{o(rms)}$	1.8	2.0	–	V
	V_P = 8.5 V; THD = 10%; f = 1 kHz	$V_{o(rms)}$	–	2.2	–	V
	V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	2.5	3.0	–	V
	V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz	$V_{o(rms)}$	–	3.5	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 8.5 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz					
for max. voltage gain	note 4	$V_{no(rms)}$	–	260	–	μV
for G_V = –3 dB	note 4	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	890	–	μV
	contour off; G_V = –40 dB	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	310	–	μV
for G_V = –16 dB	note 4	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	940	–	μV
	contour off; G_V = –40 dB	$V_{no(m)}$	–	400	–	μV

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)						
Output noise voltage; unweighted (RMS value)	see Fig. 14; f = 20 Hz to 20 kHz; note 5					
for max. voltage gain	note 4	$V_{no(rms)}$	–	350	–	μV
for G_V = –16 dB	note 4	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN45405 of 1981, CCIR recommendation 468-2 (peak value)						
for max. voltage gain for max. emphasis of bass and treble	note 4	$V_{no(m)}$	–	980	–	μV
	contour off; G_V = –40 dB	$V_{no(m)}$	–	420	–	μV

Notes to the characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\ k\Omega}{1 + G_V};\ G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4.5 dB to RMS values.

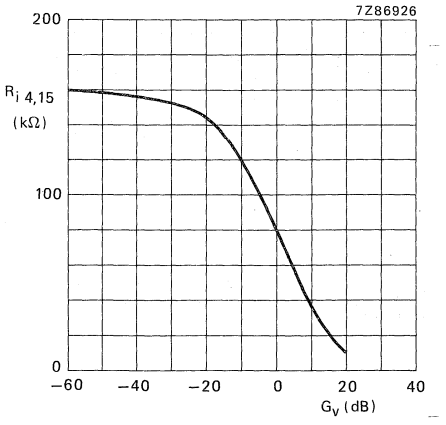


Fig. 3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

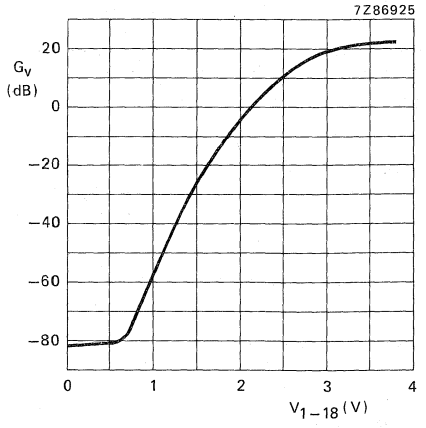


Fig. 4 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

DEVELOPMENT DATA

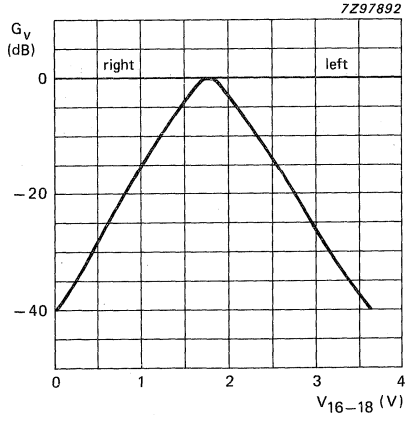


Fig. 5 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

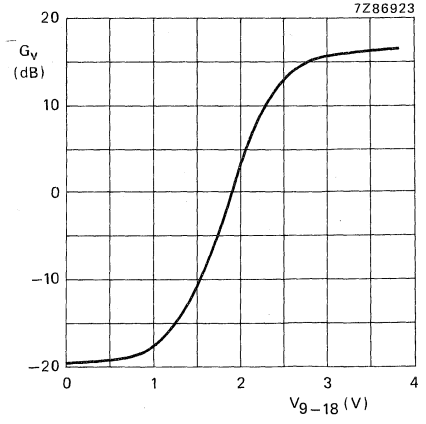


Fig. 6 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

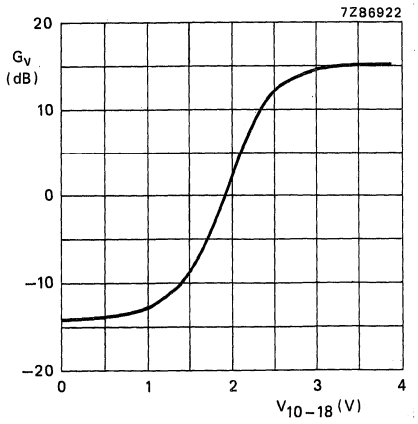


Fig. 7 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

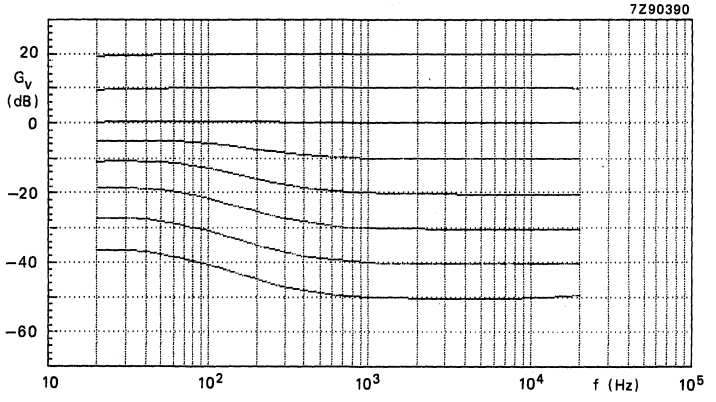


Fig. 8 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

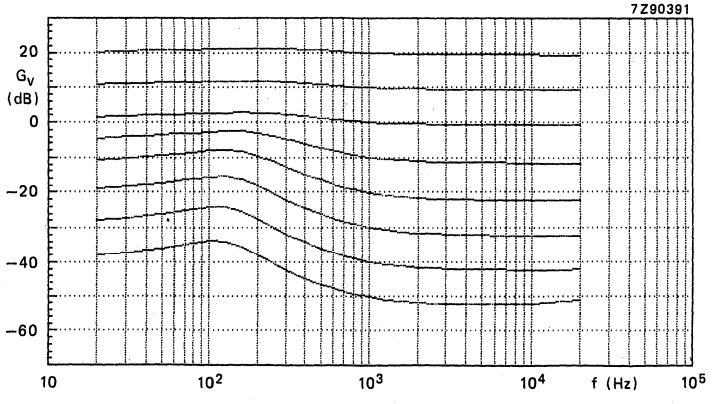


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

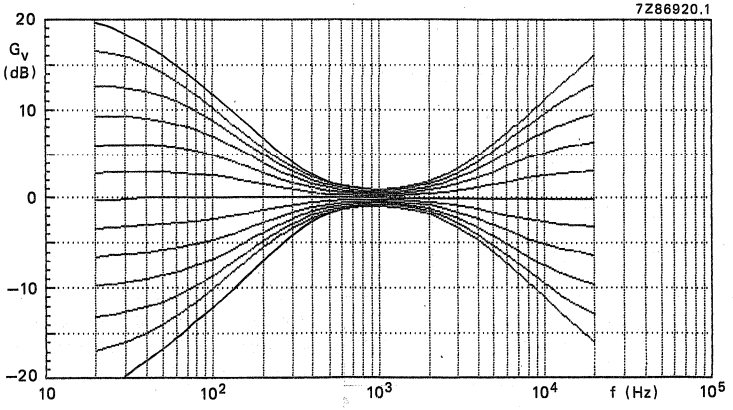


Fig. 10 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

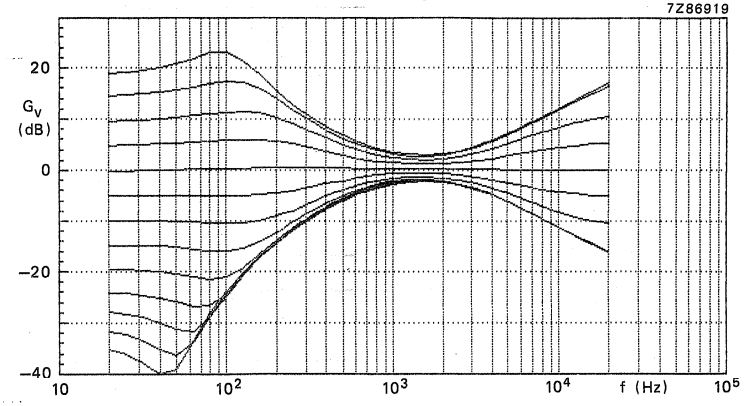


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

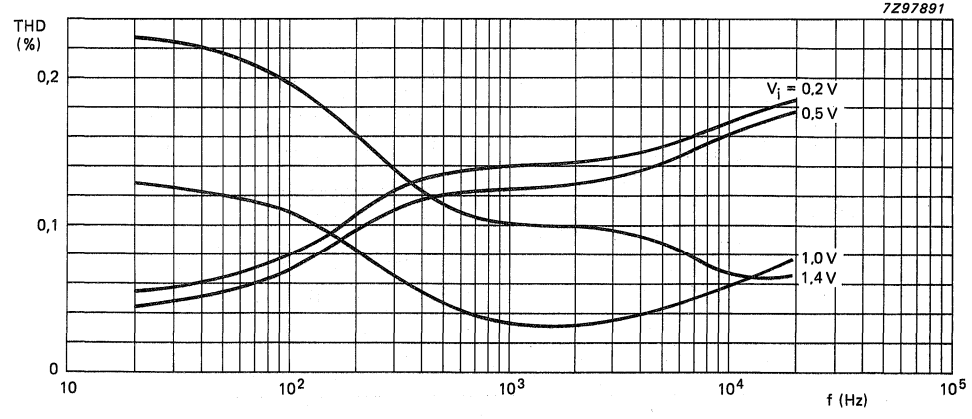


Fig. 12 Total harmonic distortion (THD) as a function of audio input frequency. Measured in Fig. 1; V_P = 8.5 V; volume control voltage gain at $G_V = 20 \log \frac{V_o}{V_i} = 0$ dB.

DEVELOPMENT DATA

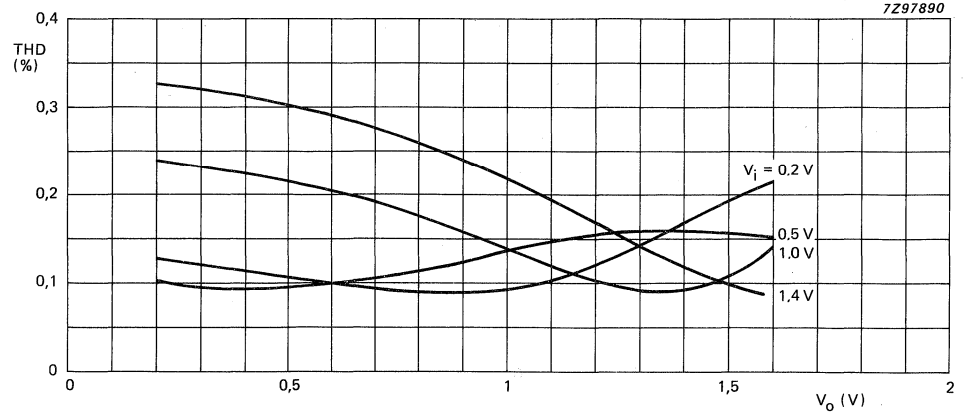
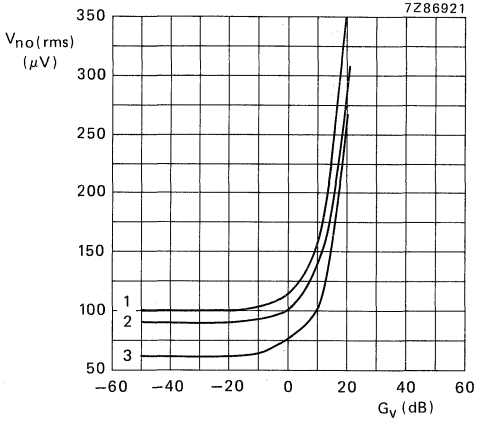


Fig. 13 Total harmonic distortion (THD) as a function of output voltage (V_o). Measured in Fig. 1; V_P = 8.5 V; f = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8.5 V.

Fig. 14 Noise output voltage ($V_{no(rms)}$; unweighted) as a function of voltage gain (G_v). Measured in Fig. 1; f = 20 Hz to 20 kHz.

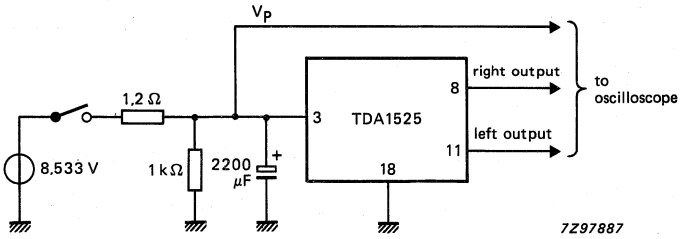
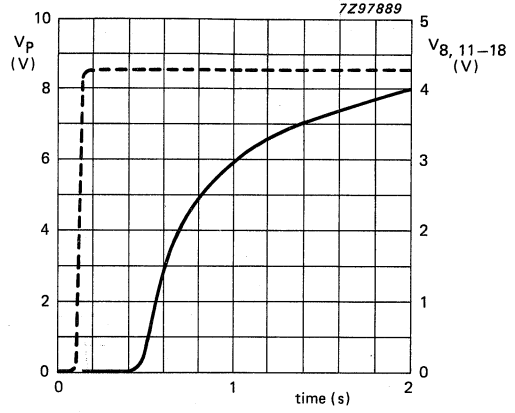


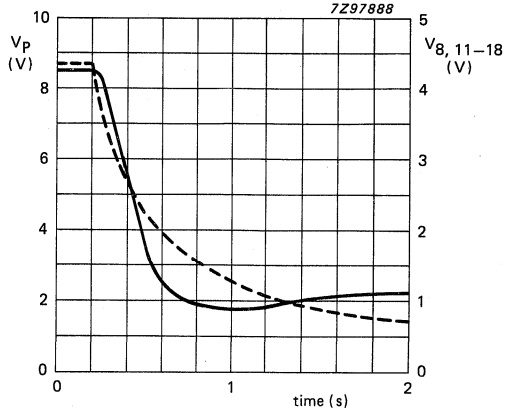
Fig. 15 Test circuit for power-on and power-off response measurements.



– – – – – represents V_P

——— represents $V_{8, 11-18}$

Fig. 16 Response at power-on. Measured in circuit of Fig. 15.



– – – – – represents V_P

——— represents $V_{8, 11-18}$

Fig. 17 Response at power-off. Measured in circuit of Fig. 15.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

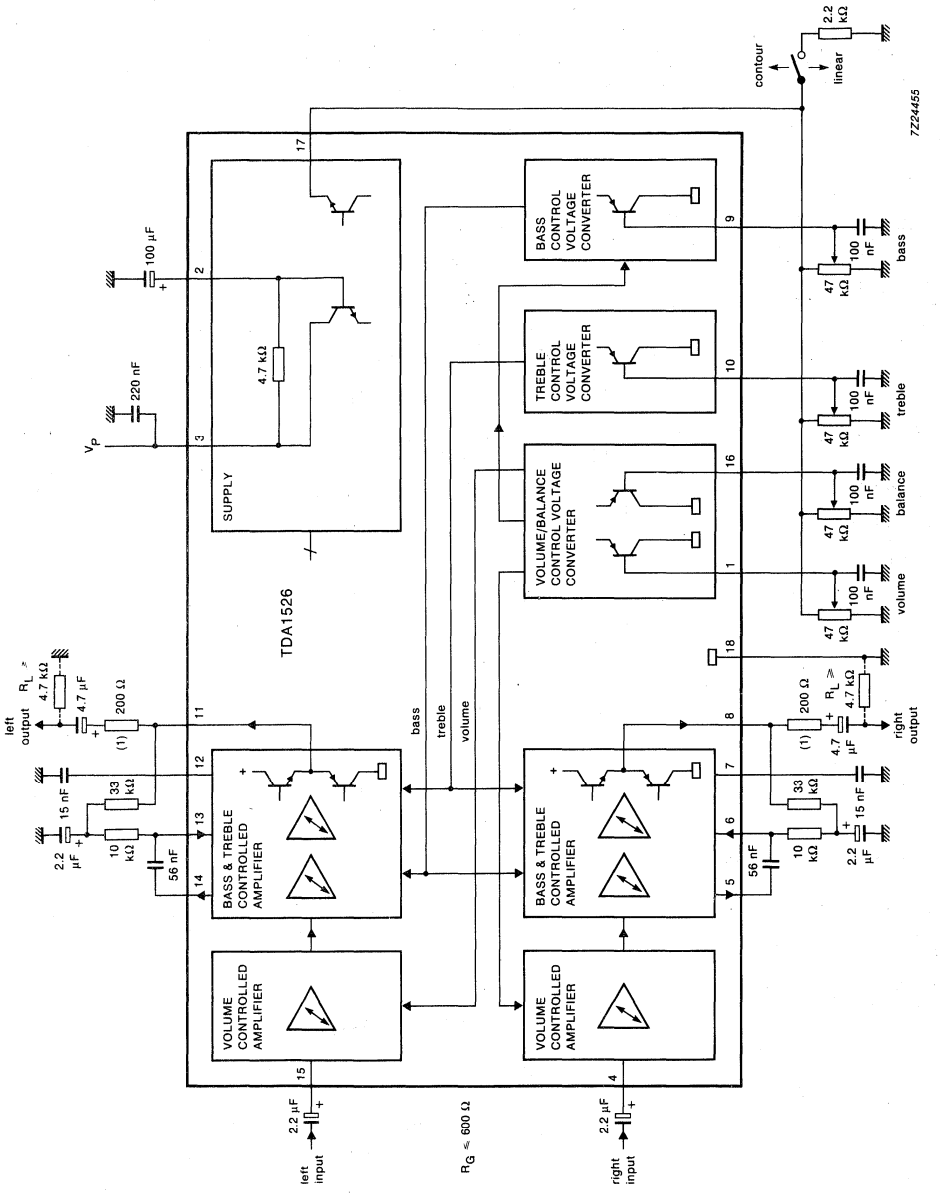
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range	$G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range	G_V = 0 dB; see Fig. 5	ΔG_V	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_V	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_V	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_V = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_V = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels for G_V = 21.5 to –26 dB	f = 250 Hz to 6.3 kHz; balance at G_V = 10 dB	ΔG_V	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

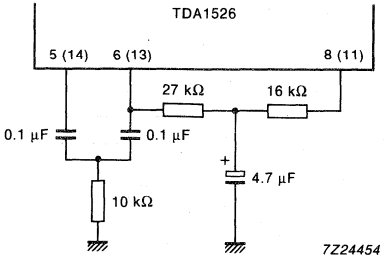


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 5)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	–19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics			see Figs 9 and 10		
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0.5\,V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0.5\,V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels					
for $G_V = 21.5$ to –26 dB					
f = 250 Hz to 6.3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2.5	dB

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_V = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_V};\ G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

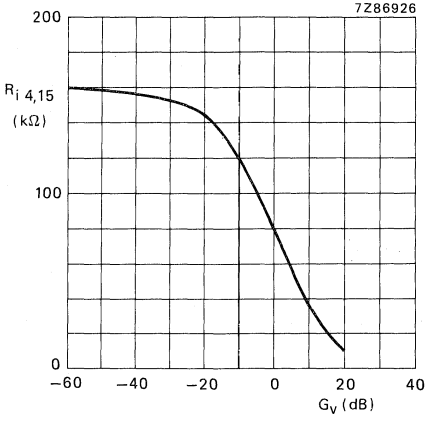


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig.1.

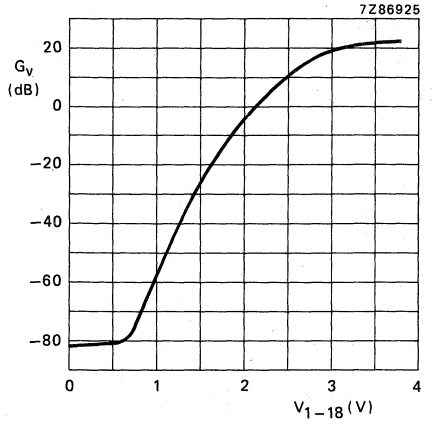


Fig.4 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

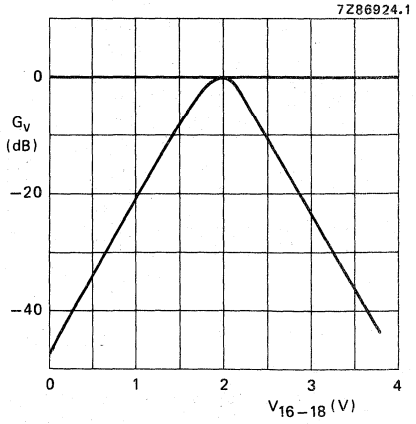


Fig.5 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

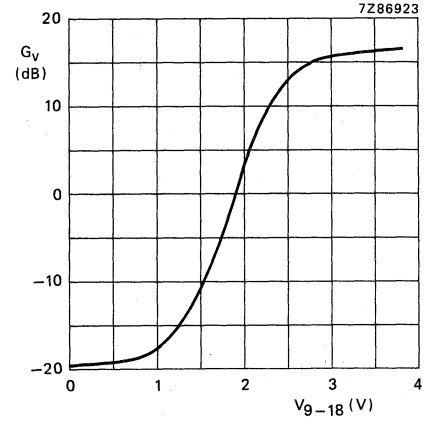


Fig.6 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

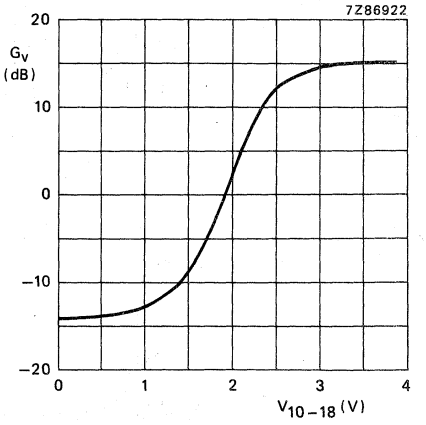


Fig.7 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

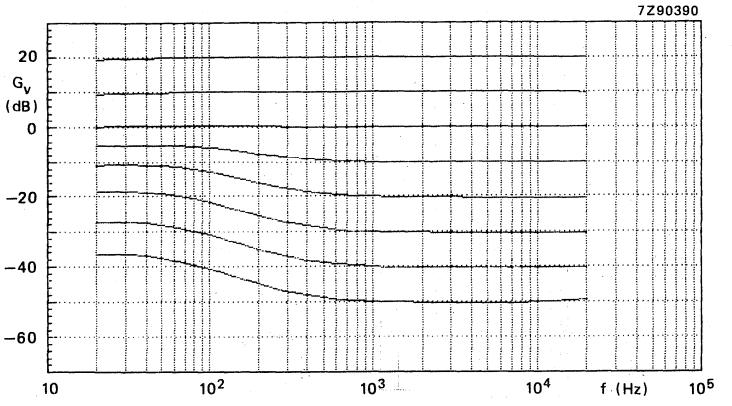


Fig.8 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

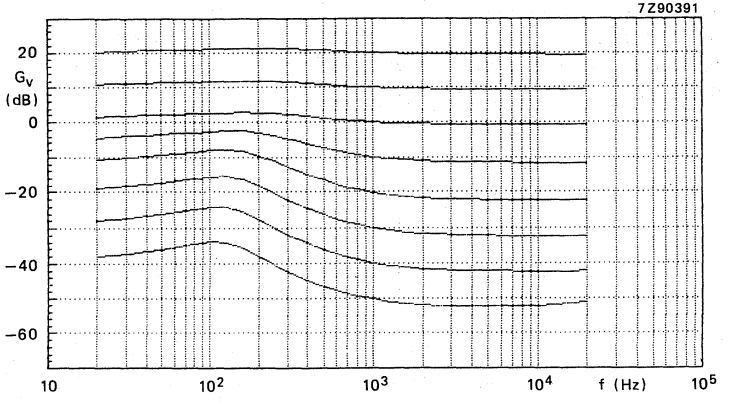


Fig.9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

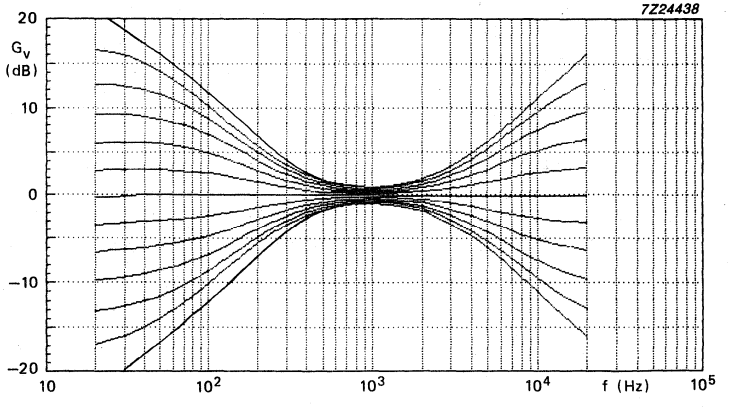


Fig.10 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

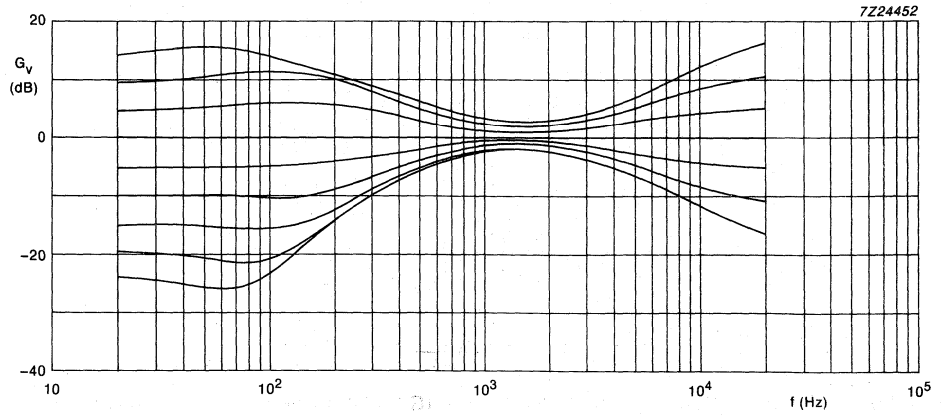


Fig.11 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

DEVELOPMENT DATA

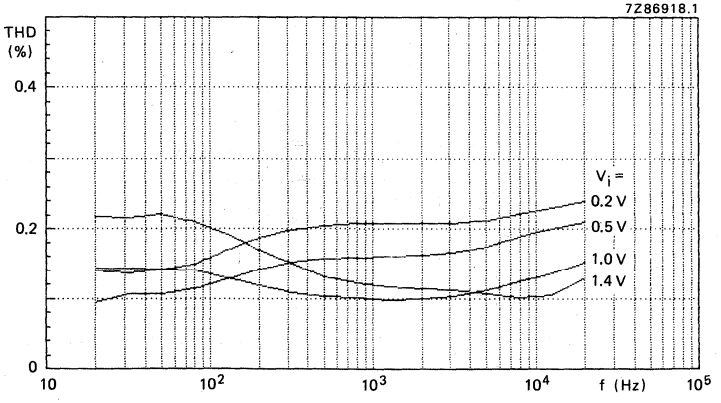


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

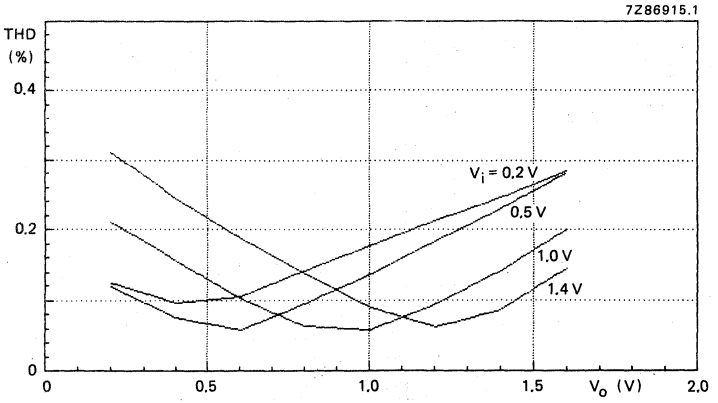


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

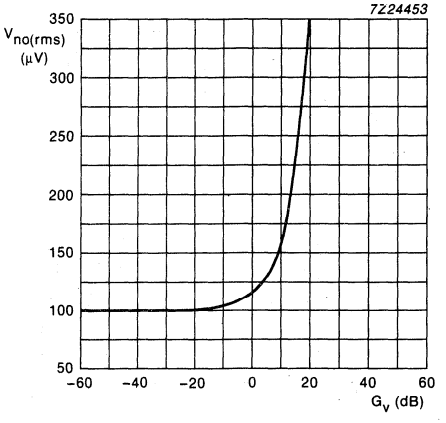


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

Philips Components

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1534

14-bit analog-to-digital converter (ADC)

GENERAL DESCRIPTION

An integrated 14-bit analog-to-digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals. Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	-	5	-	V
$-V_{N1}$	negative supply voltage 1 (pin 6)	-	5	-	V
$-V_{N2}$	negative supply voltage 2 (pin 9)	-	17	-	V
THD	total harmonic distortion including noise	-	−84	-	dB
S/N	signal-to-noise ratio	-	86	-	dB
ILE	integral linearity error	-	±1/2	-	LSB
P_{tot}	total power dissipation	-	500	-	mW
T_{amb}	operating ambient temperature range	−20	-	+70	°C
I_{FS}	full scale input current	-	4	-	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1534	28	DIL28	plastic	SOT117

14-bit analog-to-digital converter (ADC) TDA1534

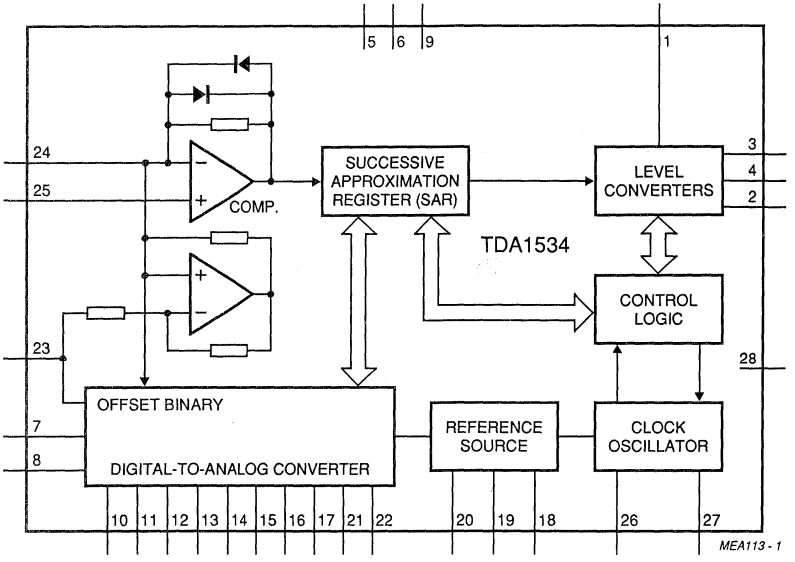


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SC	1	start conversion
SO	2	status out
DO	3	data out
DS	4	data strobe
V_P	5	positive supply voltage
V_{N1}	6	negative supply voltage 1
OSC DAC	7,8	DEM oscillator DAC
V_{N2}	9	negative supply voltage 2
DECOU	10 to 17	decoupling DEM current sources
I_{ref1}	18	I_{ref1}
I_{ref2}	19	I_{ref2}
I_{ref3}	20	I_{ref3}
DECOU	21,22	decoupling DEM current sources
OBI	23	offset binary input
AI	24	analog signal input
GND(A)	25	analog ground
COSC	26,27	oscillator system clock
GND(D)	28	digital ground

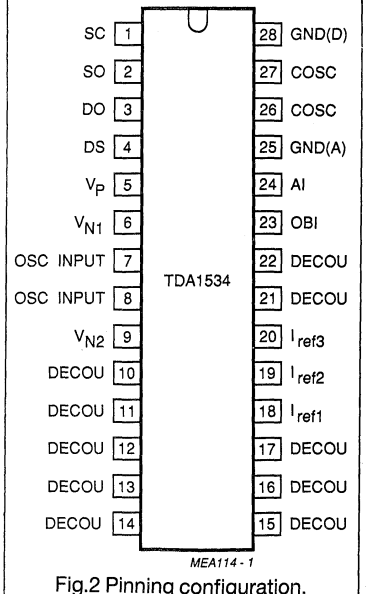


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit digital-to-analog converter (DAC)

Using "dynamic element matching", which results in high accuracy, linearity and long term stability, without the need of trimming. The main parts of the DAC are the dynamic element matching (DEM) circuitry and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the DAC.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig.3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-and-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the ADC starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage (pin 5)	0	7	V
$-V_{N1}$	negative supply voltage 1 (pin 6)	0	7	V
$-V_{N2}$	negative supply voltage 2 (pin 9)	0	20	V
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature	−20	+70	°C
V_{es}	electrostatic handling*	−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	110	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS (see application circuit Figs 5a and 5b)

V_P = 5 V; $-V_{N1}$ = 5 V; $-V_{N2}$ = 17 V; T_{amb} = +25 °C, unless otherwisse specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 5)		4	5	6	V
$-V_{N1}$	negative supply voltage 1 (pin 6)		4	5	6	V
$-V_{N2}$	negative supply voltage 2 (pin 9)		16.5	17	18	V
I_P	positive supply current		-	30	40	mA
$-I_{N1}$	negative supply current		-	37	45	mA
$-I_{N2}$	negative supply current		-	10	13	mA
P_{tot}	total power dissipation		-	500	-	mW
	resolution		-	14	-	bits
Analog input						
I_{FS}	full scale input current	offset-binary current switched off	3.8	4.0	4.2	mA
TC_{IFS}	temperature coefficient	pin 23 short-circuited to ground; note 1	-	30	-	10^{-6}/K
Zero-offset						
$-V_o$	offset voltage	offset-binary current switched off	-	20	30	mV
TC_{Vo}	temperature coefficient		-	4	-	V/K
$-I_o$	offset current		-	500	2000	nA
TC	temperature coefficient		-	1.5	-	nA/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Linearity						
$\|DLE\|$	linearity error (differential)		0	-	0.9	LSB
$\|ILE\|$	linearity error (integral)		0	0.25	0.9	LSB
$\|ILE_T\|$	linearity error	T_{amb} = −20 to +70 °C	0	0.5	-	LSB
I_{BO}	offset binary current		$0.45I_{FS}$	$0.50I_{FS}$	$0.55I_{FS}$	mA
TC_{IBO}	temperature coefficient	note 1	-	30	-	10^{-6}/K
Distortion						
THD	total harmonic distortion including noise		-	−84	-	dB
S/N	signal-to-noise ratio	note 2	-	86	-	dB
Start conversion (pin 1)						
input voltages						
V_{IL}	input voltage LOW	$-I_{IL}$ < 1.6 mA	0	-	0.8	V
V_{IH}	input voltage HIGH	I_{IH} < 40 µA	2	-	5	V
input currents						
$-I_{IL}$	input current LOW	V_{IL} < 0.8 V	-	-	1.6	mA
I_{IH}	input current HIGH	V_{IH} > 2 V	-	-	40	µA
Data, strobe, status (pins 3,4 and 2)						
output voltages						
V_{OL}	output voltage LOW	$I_{OL} \leq$ 6.4 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$-I_{OH}$ < 160 µA	2.4	-	5	V
output currents						
I_{OL}	output current LOW	$V_{OL} \leq$ 0.6 V	-	1.6	1.6	mA
$-I_{OH}$	output current HIGH	$-V_{OH} \geq$ 2.4 V	-	400	400	µA
Timing						
f_{clock}	oscillator clock (pin 26 and 27)		-	3.5	-	MHz
t_c	conversion time determined by C_{26-27}	note 3	6.5	0.042 x C (in pF)	-	µs
t_{sc}	signal width (pin 1)	start conversion	0.2	-	t_c	µs
t_{PDSH}	status delay time HIGH (pin 2)		-	60	200	ns
t_{PDDS}	data strobe delay time		-	900	1100	ns
t_{DSH}	pulse duration (pin 4)	data strobe HIGH	-	125	-	ns
t_{DSL}	pulse duration (pin 4)	data strobe LOW	-	435	-	ns
t_{DS}	set-up time (pin 3)	data out	-	25	350	ns
t_{PDSL}	status delay time LOW (pin 2)		-	200	350	ns
$f_{osc\ x\ DAC}$	oscillator DAC (pins 7 and 8)		100	160	200	kHz

Notes to the characteristics

1. I_{FS} and I_{BO} track with each other over temperature range.
2. Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44.1 kHz.
3. Minimum value is 150 pF and value used with testing is 820 pF. See Fig.4.

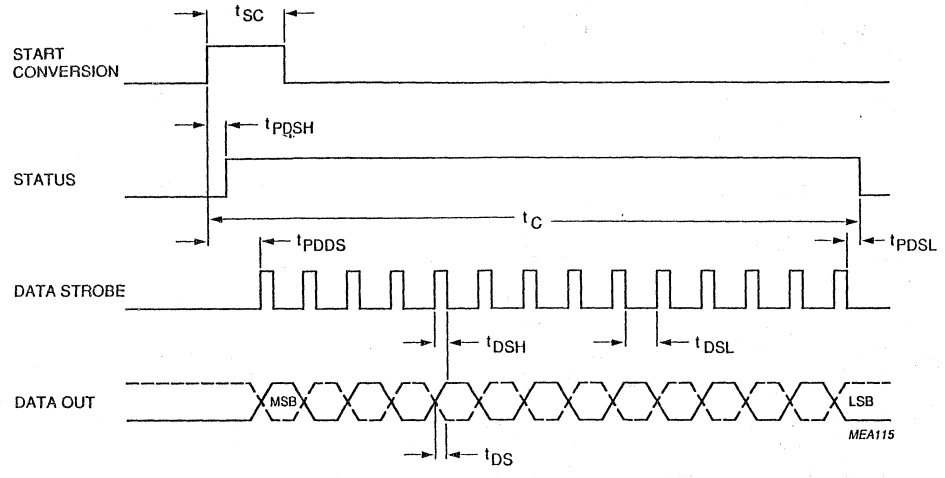


Fig.3 Timing diagram.

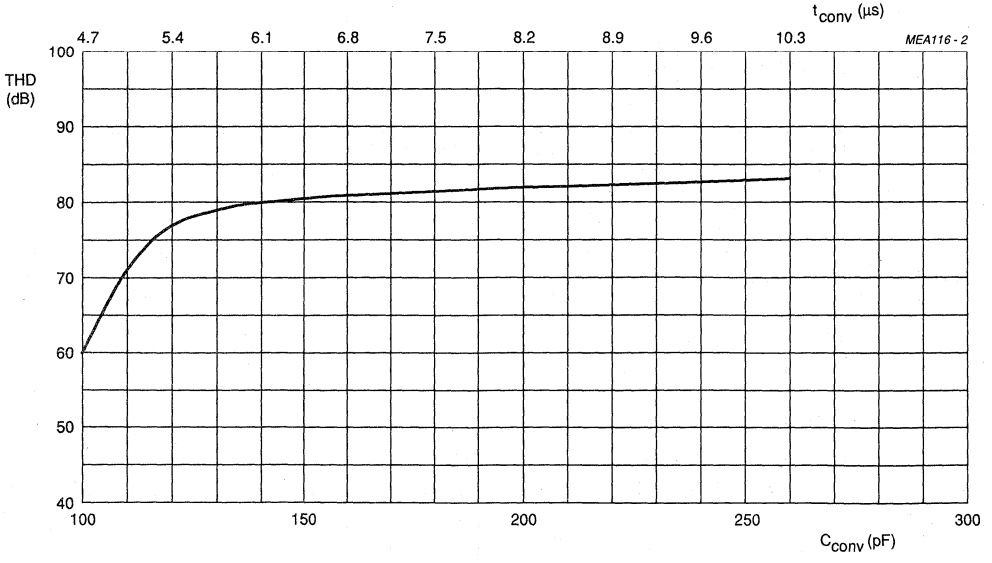


Fig.4 Distortion as a function of conversion time.

14-bit analog-to-digital converter (ADC) TDA1534

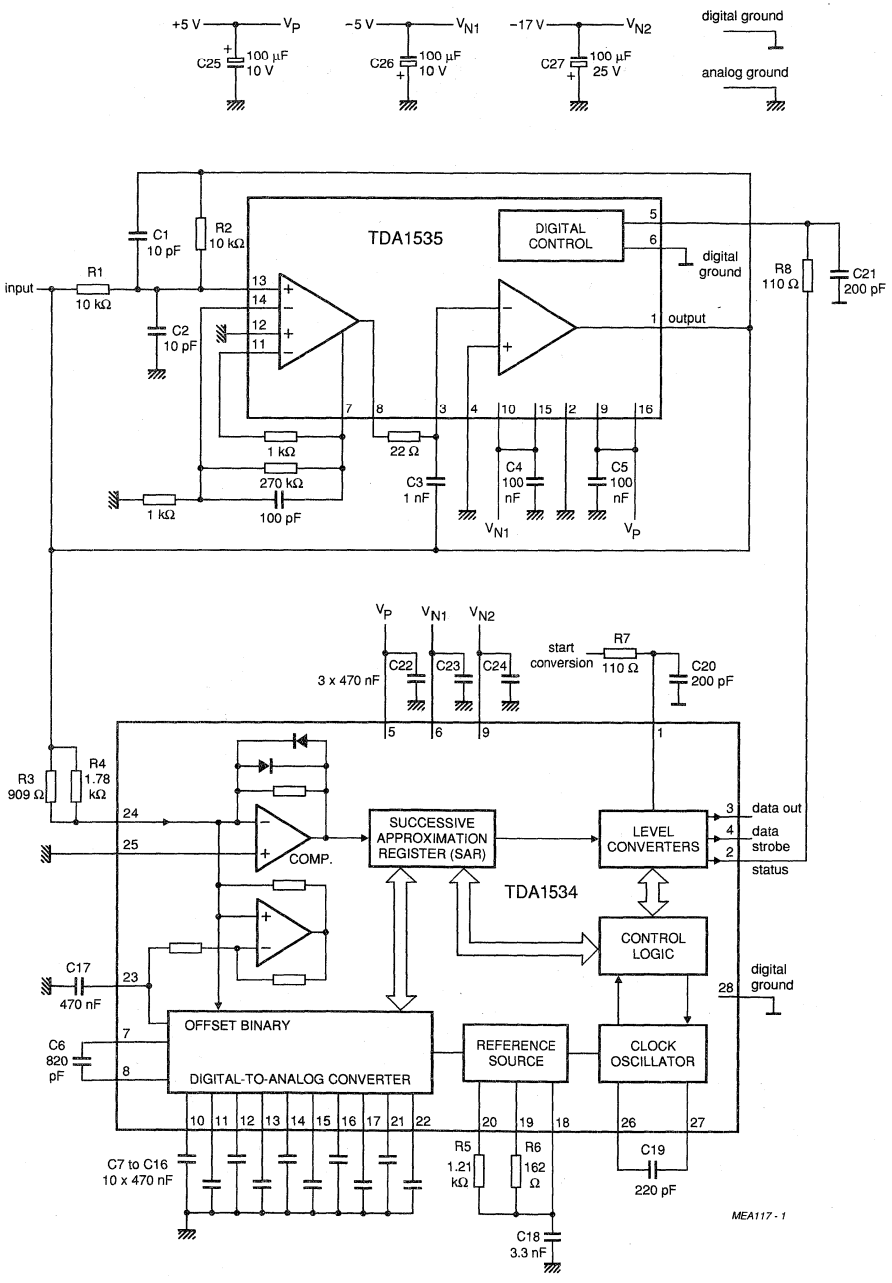


Fig.5a Application diagram.

14-bit analog-to-digital converter (ADC) TDA1534

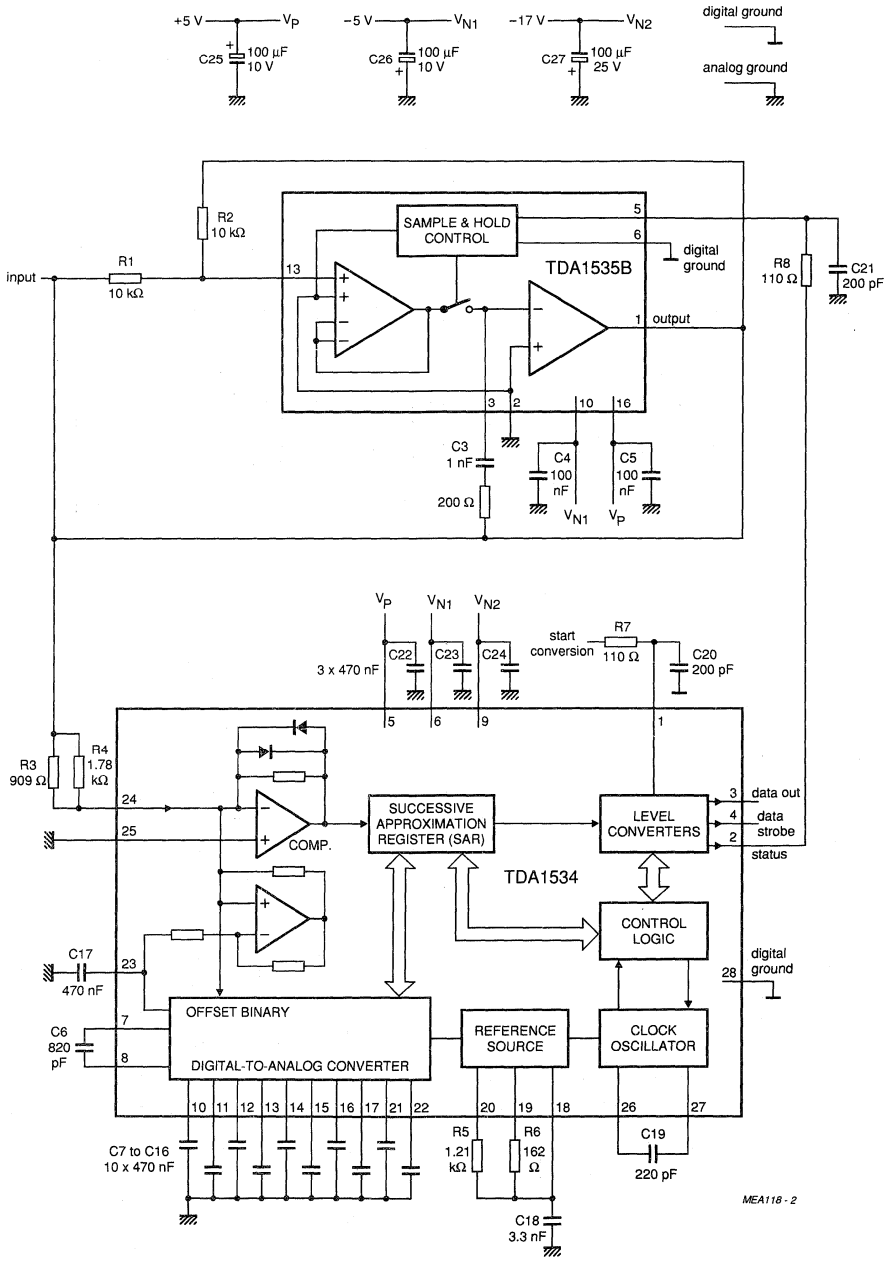


Fig.5b Basic evaluation circuit.

High-speed single sample-and-hold amplifier

TDA1535B

GENERAL DESCRIPTION

The TDA1535B is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with resolution up to 16 bits. The control input is TTL compatible.

FEATURES

- High-speed: fast acquisition, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Low noise: low total harmonic distortion and high signal-to-noise ratio
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a single Sample-and-Hold circuit. The several parts of the diagram will be described in the next sections.

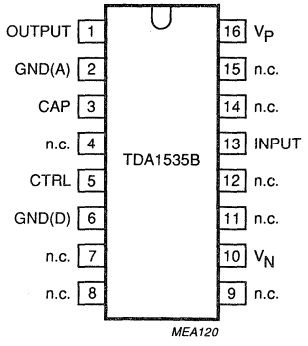


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	4.5	5.0	5.5	V
V_N	negative supply voltage	−5.5	−5.0	−4.5	V
THD	total harmonic distortion	–	−100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	225	–	mW
T_{amb}	operating ambient temperature range	−30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1535B	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
OUTPUT	1	output
GND(A)	2	analog ground
CAP	3	S/H capacitor
n.c.	4	not connected
CTRL	5	S/H control
GND(D)	6	digital ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
V_N	10	negative supply voltage
n.c.	11	not connected
n.c.	12	not connected
INPUT	13	input
n.c.	14	not connected
n.c.	15	not connected
V_P	16	positive supply voltage

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of a current source circuit which contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

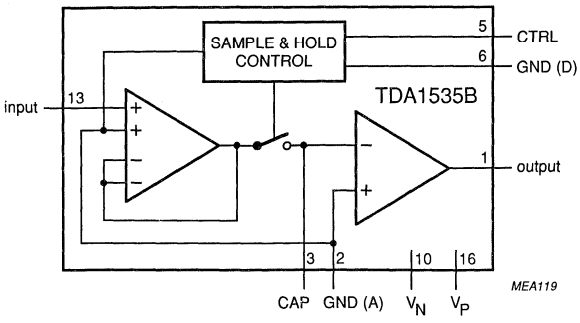


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	6	V
V_N	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned in the above sections in the correct timing order. The supply is taken from the 'V_p' pin via an on-chip separate supply line.

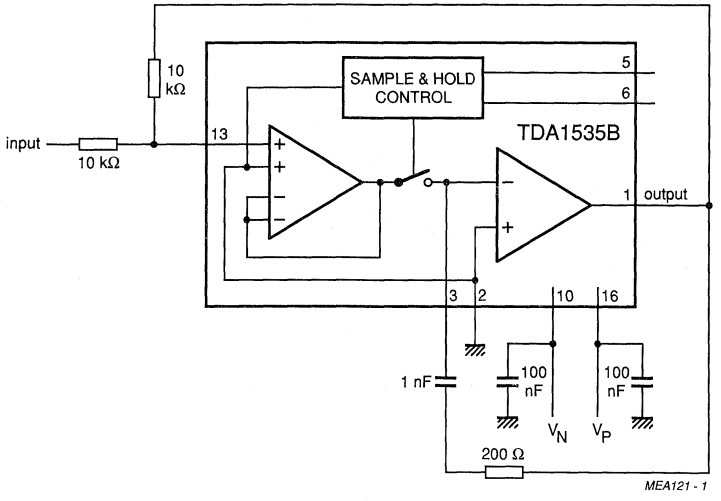


Fig.3 Test and application diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	5.0	5.5	V
V_N	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	22	–	mA
I_N	negative supply current		–	−23	–	mA
P_{tot}	total power dissipation		–	225	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier; amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

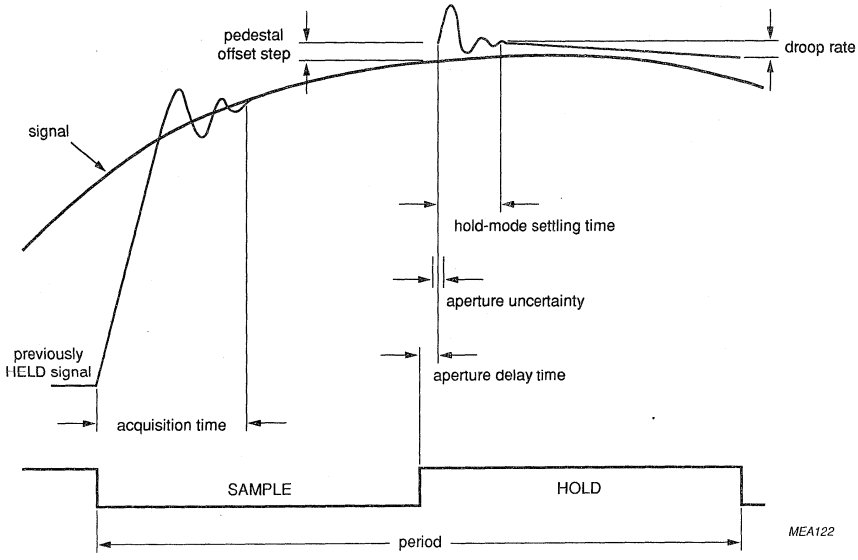


Fig.4 Sample/hold timing characteristics (not to scale).

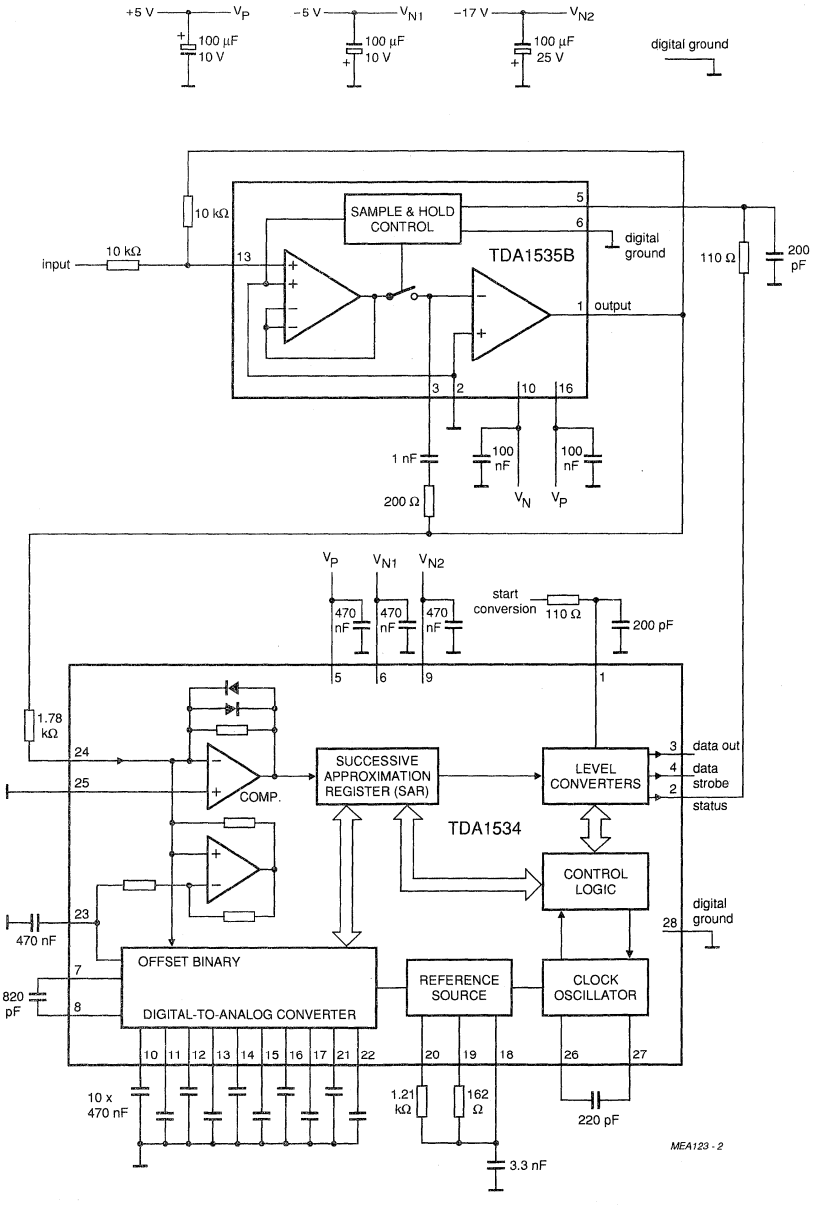


Fig.5 Application diagram of TDA1535B in combination with TDA1534.

High-speed stereo sample-and-hold amplifier

TDA1537

GENERAL DESCRIPTION

The TDA1537 is a high-speed stereo sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with a resolution up to 16 bits, such as hi-fi digital audio equipment. The control input is TTL compatible.

FEATURES

- Low noise: low total harmonic distortion and high signal-to-noise ratio
- High-speed: fast acquisition time, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a stereo Sample-and-hold circuit. The several parts of the diagram will be described in the next sections.

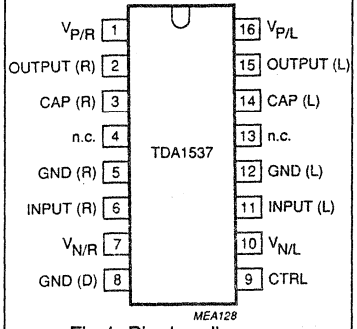


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{P/R}$, $V_{P/L}$	positive supply voltage	4.5	5.0	5.5	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage	−5.5	−5.0	−4.5	V
THD	total harmonic distortion	–	−100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	455	–	mW
T_{amb}	operating ambient temperature range	−30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1537	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{P/R}$	1	VP (right)
OUTPUT (R)	2	output (right)
CAP (R)	3	S/H capacitor (right)
n.c.	4	not connected
GND (R)	5	ground (right)
INPUT (R)	6	input (right)
$V_{N/R}$	7	VN (right)
GND (D)	8	digital ground
CTRL	9	S/H control input
$V_{N/L}$	10	VN (left)
INPUT (L)	11	input (left)
GND (L)	12	ground (left)
n.c.	13	not connected
CAP (L)	14	S/H capacitor (left)
OUTPUT (L)	15	output (left)

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of two separate PTAT current source circuits, for 'left' and the 'right' S/H circuit. In this way a channel separation of more than 100 dB is realized. Each PTAT current source circuit contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

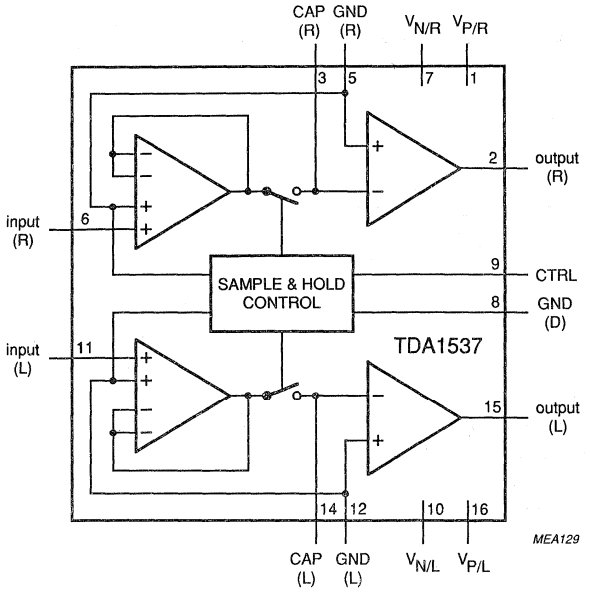


Fig.2 Block diagram.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{P/R}$, $V_{P/L}$	positive supply voltage		–	6	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned into above sections in the correct timing order. The supply is taken from the 'V_p left' pin via an on-chip separate supply line.

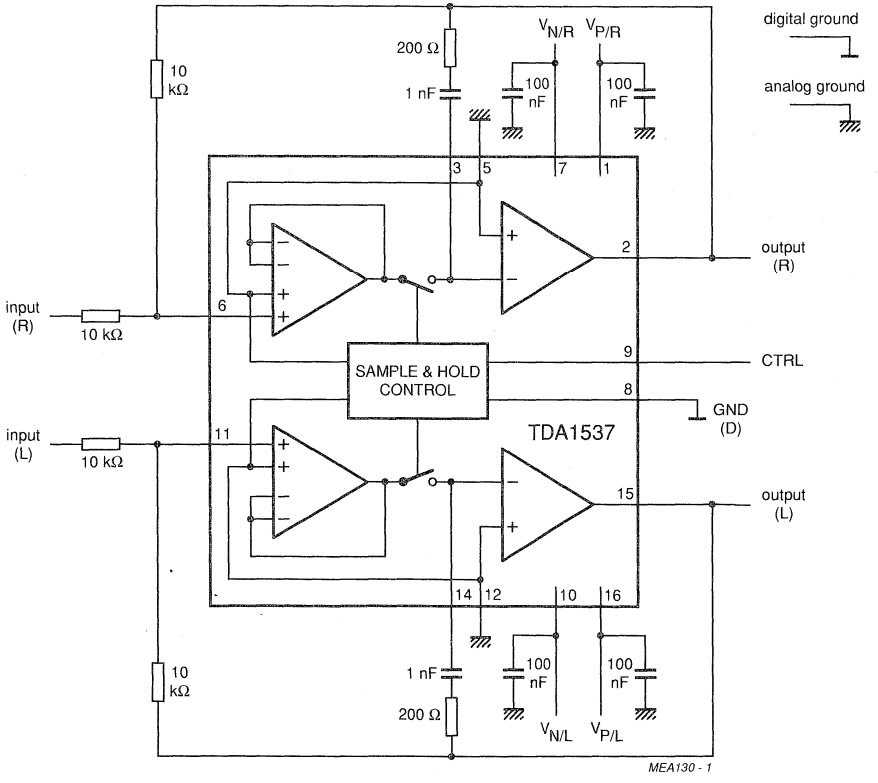


Fig.3 Test and application diagram.

CHARACTERISTICS

$V_{P/R}$, $V_{P/L}$ = +5 V; $V_{N/R}$, $V_{N/L}$ = −5 V; T_{amb} = +25 °C; f = 1 kHz, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{P/R}$, $V_{P/L}$	positive supply voltage		4.5	5.0	5.5	V
$V_{N/R}$, $V_{N/L}$	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	45	–	mA
I_N	negative supply current		–	−46	–	mA
P_{tot}	total power dissipation		–	455	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier;amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

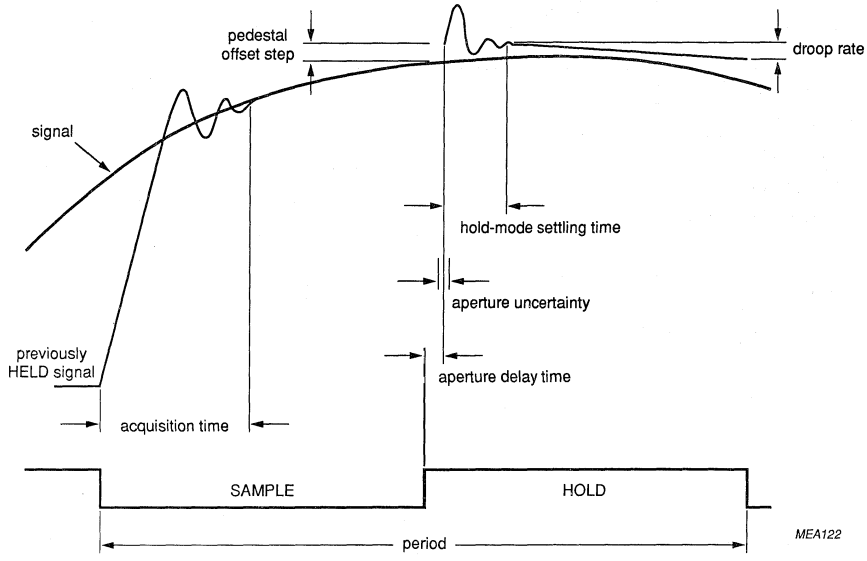


Fig.4 Sample/hold timing characteristics (not to scale).

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

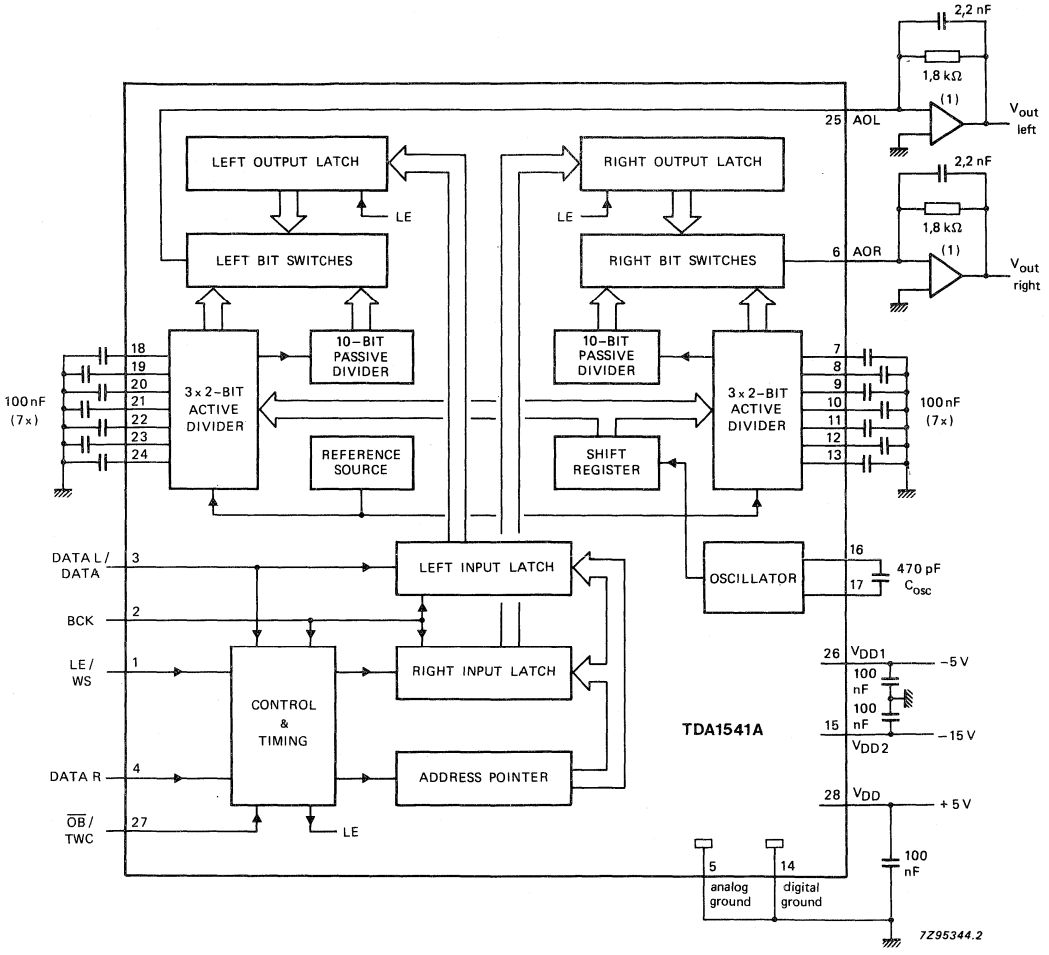
ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	±200 x 10^{-6}	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW

Stereo high performance 16-bit DAC TDA1541A



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

Stereo high performance 16-bit DAC TDA1541A

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	−15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	−5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

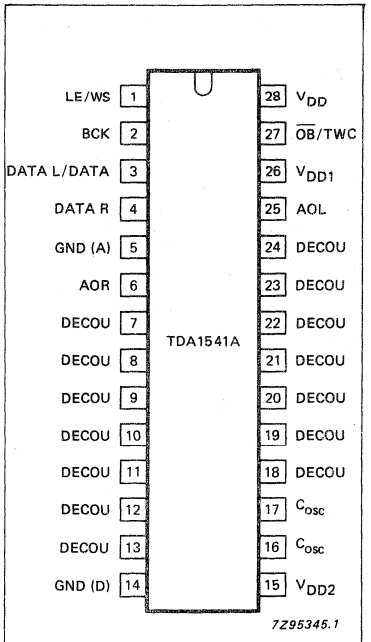


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I²S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C
V_{es}	electrostatic handling*		−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)}$ $-V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB}/TWC}\rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS}\rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	−76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = −5 V; note 4	-	−84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = −15 V; note 4	-	−58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

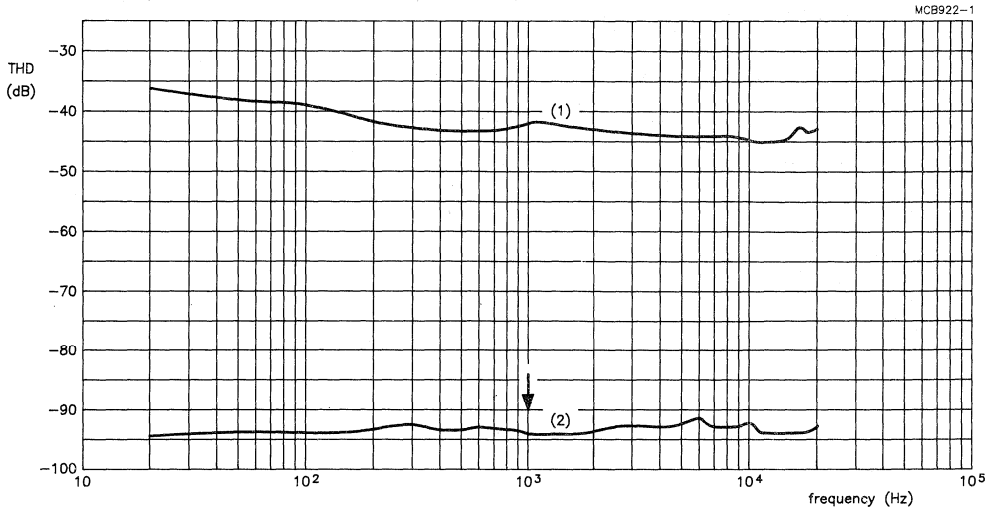
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

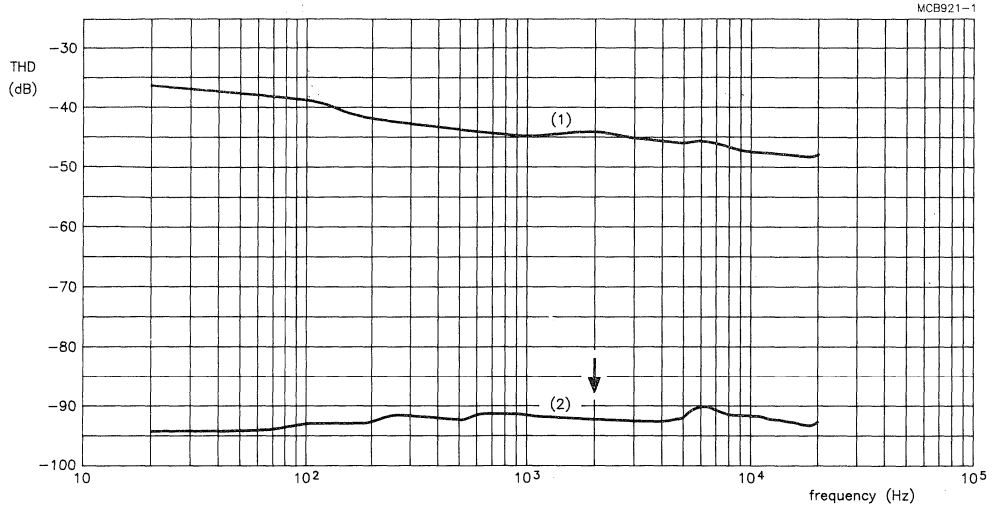


(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

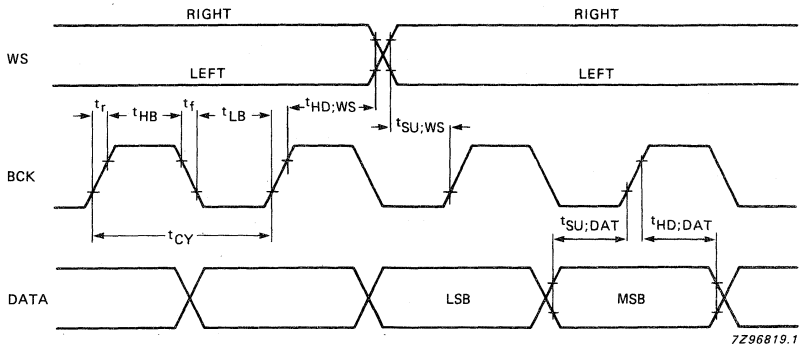


Fig.4 Format of input signals; time multiplexed (I^2S format).

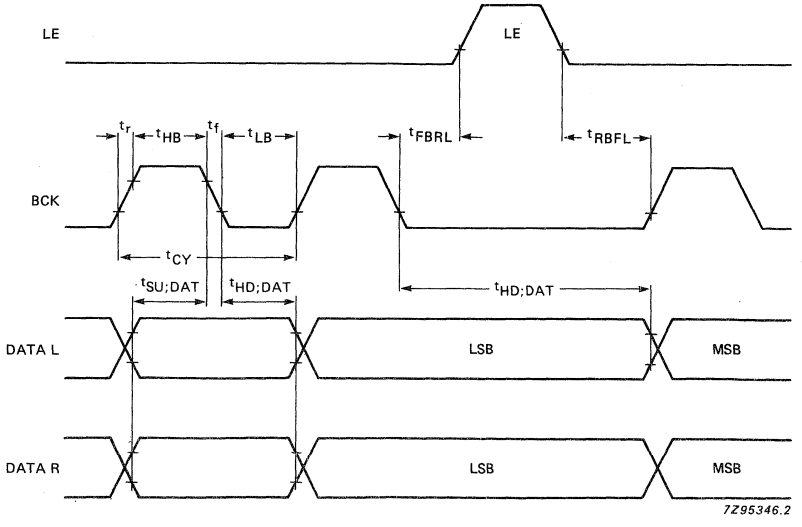


Fig.5 Format of input signals; simultaneous data.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

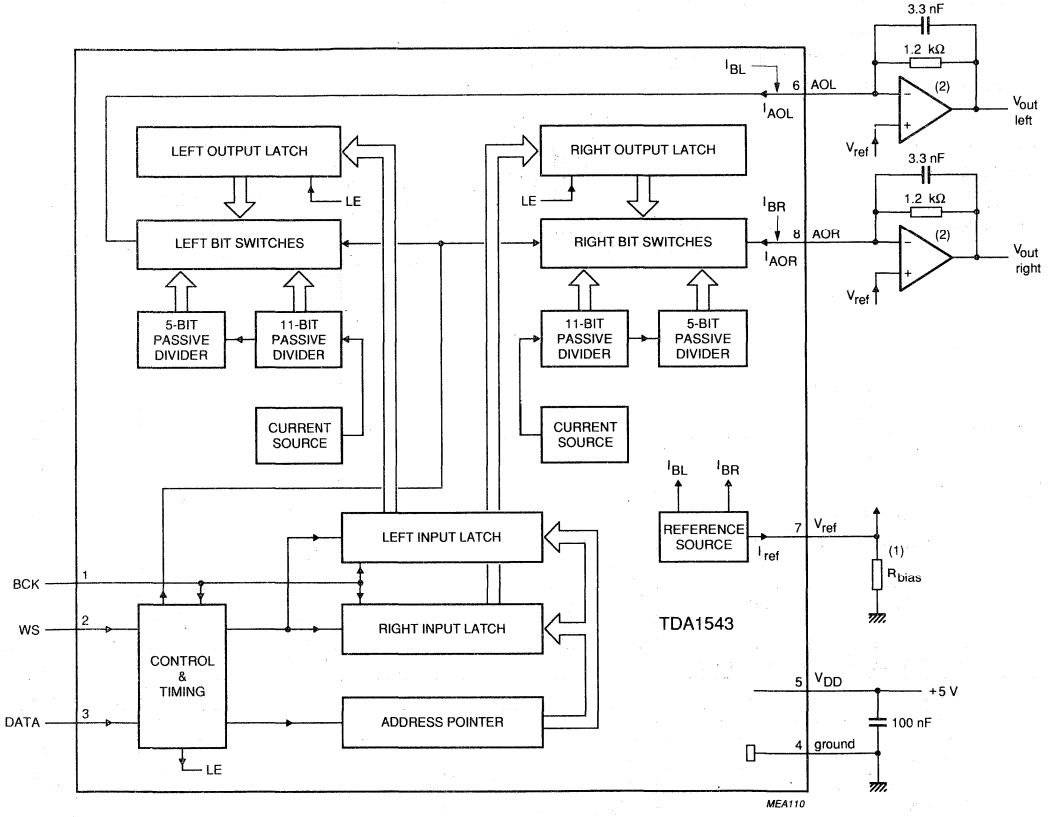
The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	–75	–70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	–30	–23	dB
		at –60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		–30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		–0.6	-	5.0	mA



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

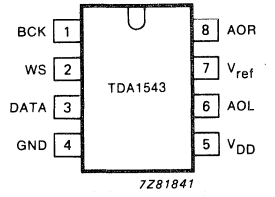


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

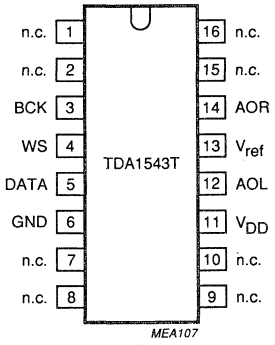
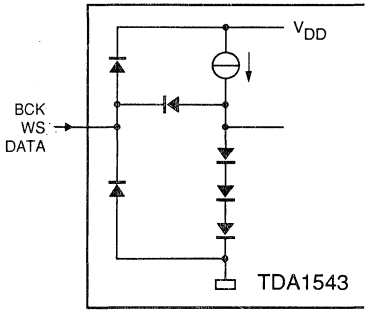
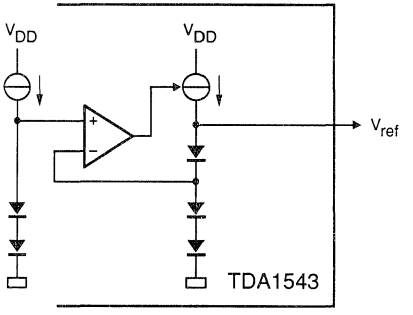


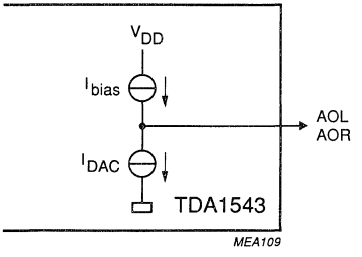
Fig.2(b) Pin configuration TDA1543T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		-55	+150	°C
T_{amb}	operating ambient temperature range		-30	+85	°C
V_{es}	electrostatic handling*		-2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

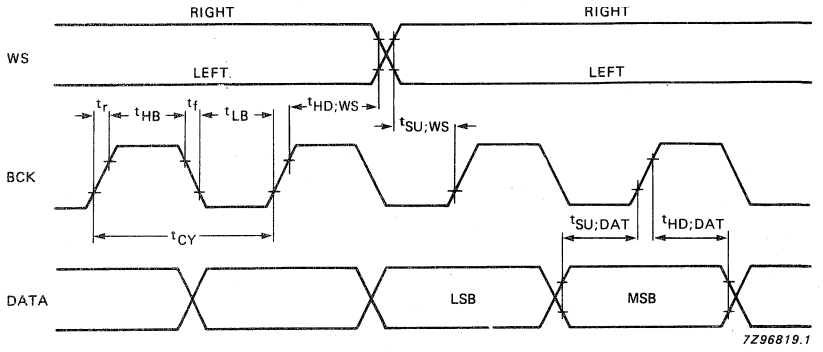


Fig.4 Format of input signals (I²S format).

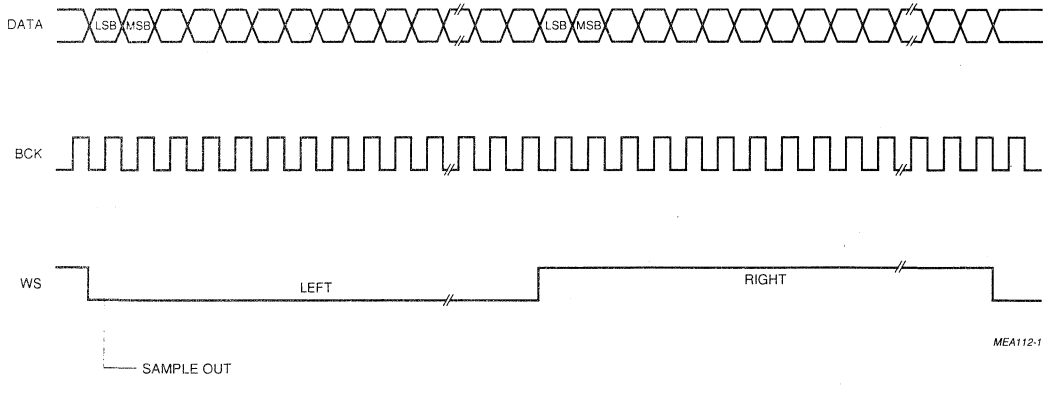
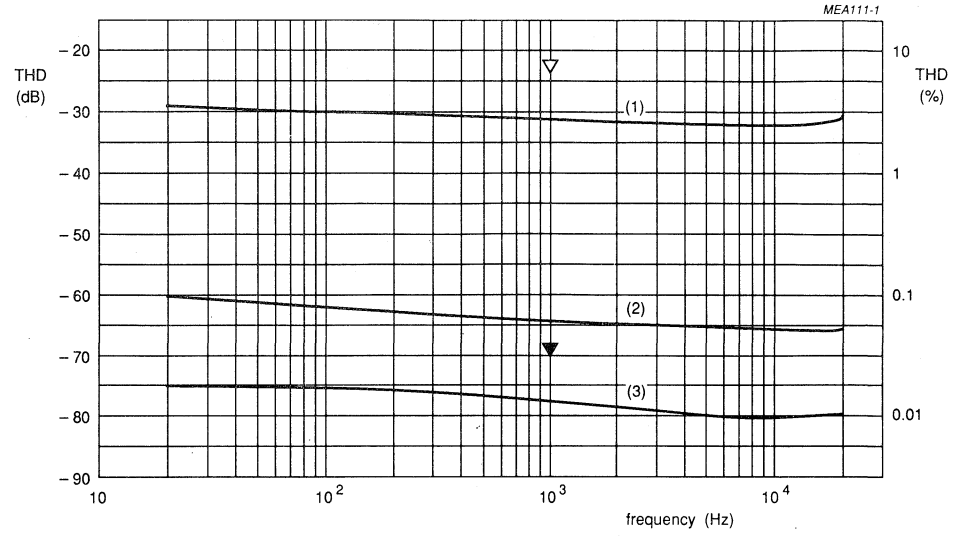


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543A

Dual 16-bit DAC (economy version) (Japanese input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders and in digital amplifiers.

ORDERING INFORMATION

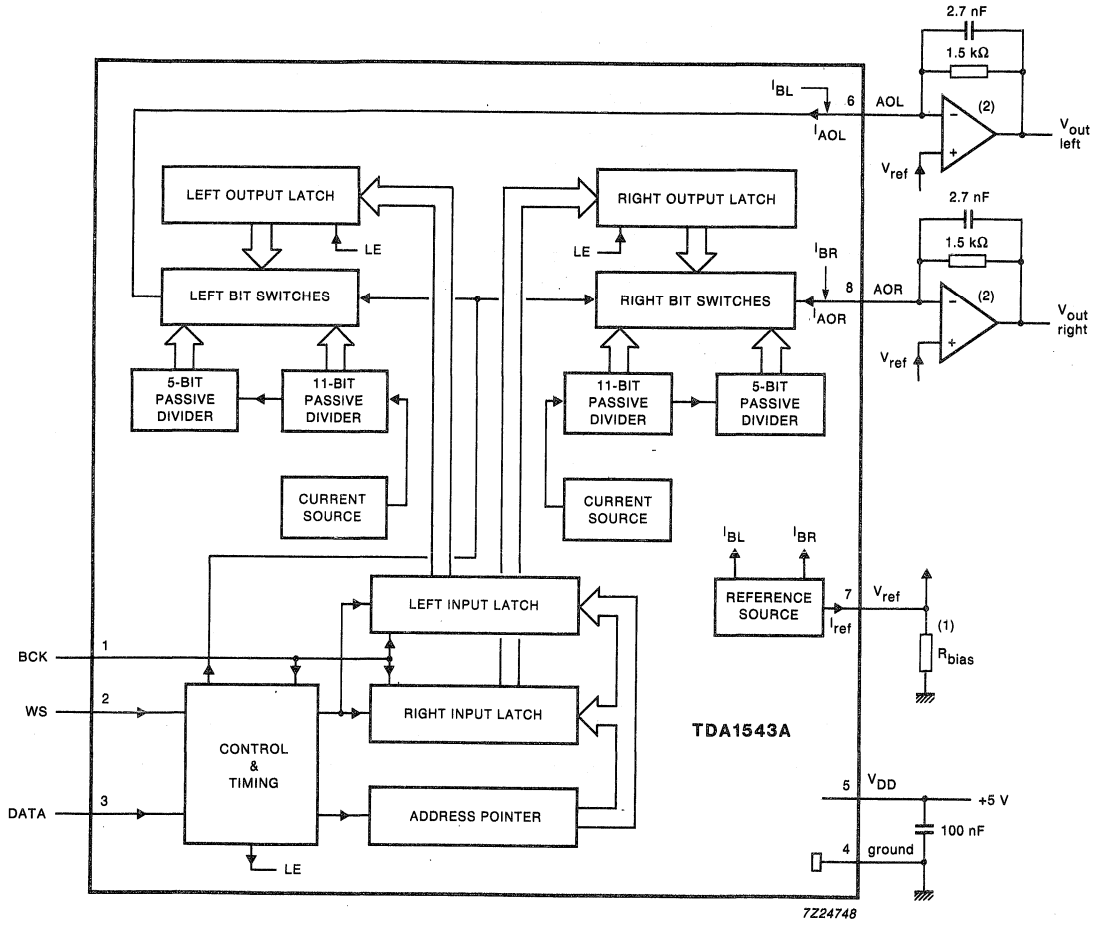
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543A	8	DIL	plastic	SOT97
TDA1543AT	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

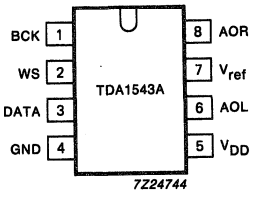


Fig.2(a) Pin configuration TDA1543A.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

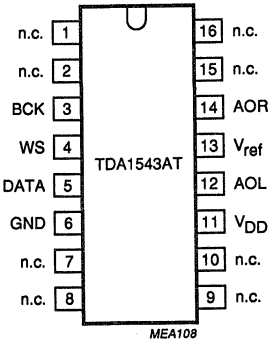
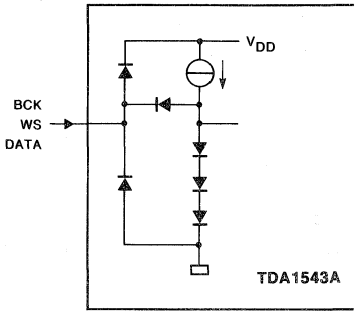
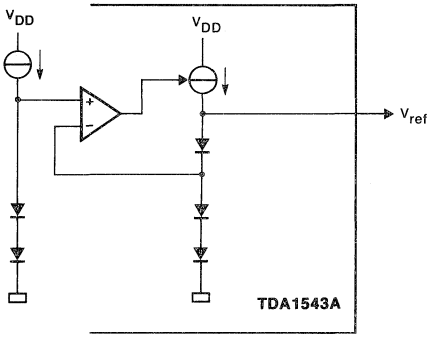


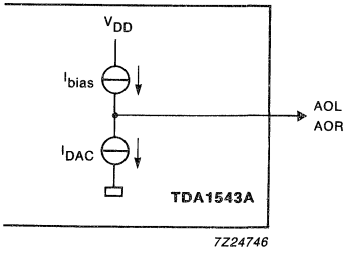
Fig.2(b) Pin configuration TDA1543AT.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (Japanese) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

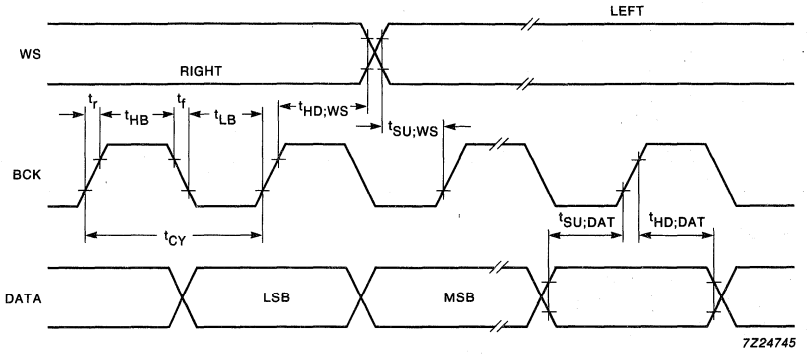


Fig.4 Format of input signals (Japanese format).

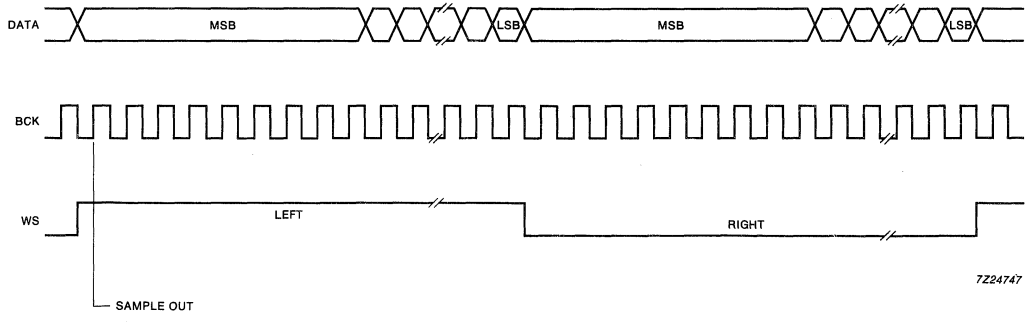
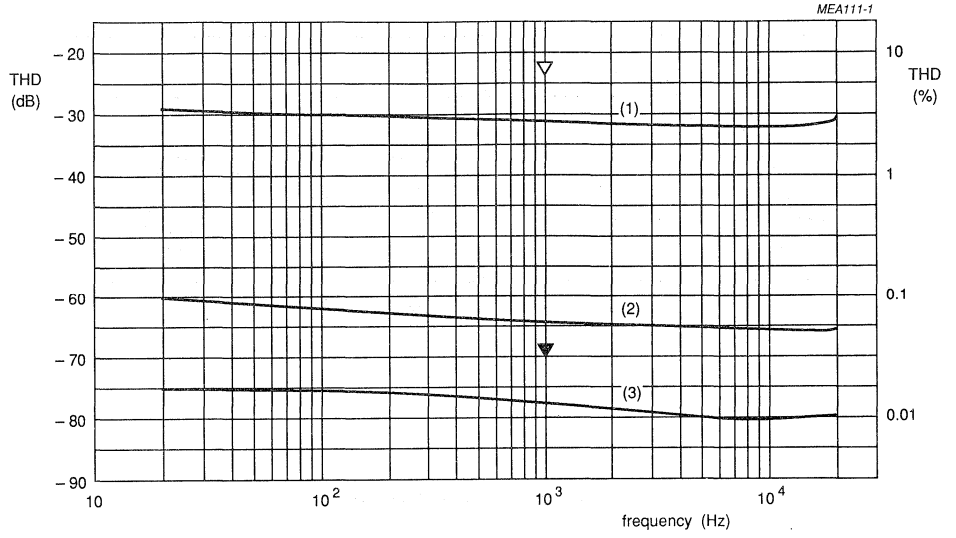


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543(A)/S6

Dual 16-bit low-cost economy DAC (relaxed version of TDA1543A)

GENERAL DESCRIPTION

The TDA1543(A)/S6 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as a low-cost economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in television systems and digital amplifiers.

The S6 version is a relaxed version of the TDA1543(A). The differences in performance between the S6 selection and the standard version are limited to only three parameters:

QUICK REFERENCE VALUES STANDARD VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–70	dB
T_{amb}	operating ambient temperature range		–30	+85	°C
AI_{bias}	bias current gain		1.9	2.1	

QUICK REFERENCE VALUES S6 VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	–60	dB
T_{amb}	operating ambient temperature range		–20	+75	°C
AI_{bias}	bias current gain		1.85	2.1	

The other characteristics of the S6 version can be found in the data sheets of the TDA1543 and the TDA1543A.

Philips Components

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1544
Dual 16-bit low-noise DAC

FEATURES

- 16-bit resolution and 4 x oversampling
- High performance: low distortion, wide dynamic range and high signal-to-noise ratio
- Single 5 V power supply
- No external components required
- Adjustable bias current
- Japanese-input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1544 is a dual 16-bit digital-to-analog converter (DAC) and is designed for use in hi-fi digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1544	8	DIL	plastic	SOT97
TDA1544T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		2.7	3.0	3.3	mA
THD	total harmonic distortion	including noise	-	–75	–70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	–33	–23	dB
		at –60 dB	-	2.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio		99	101	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		–30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		–0.6	-	5.0	mA

Dual 16-bit low-noise DAC TDA1544

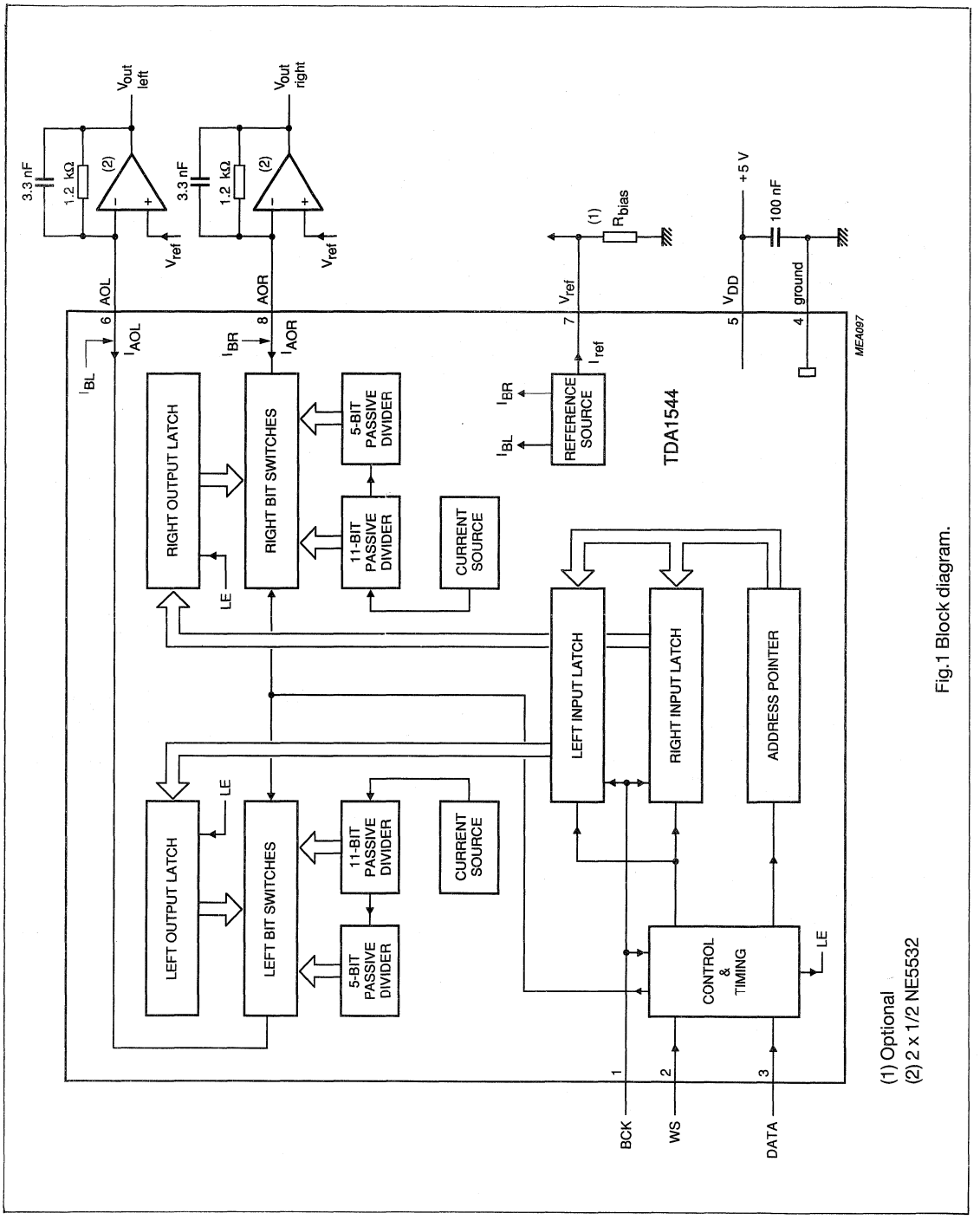


Fig.1 Block diagram.

(1) Optional
(2) 2 x 1/2 NE5532

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

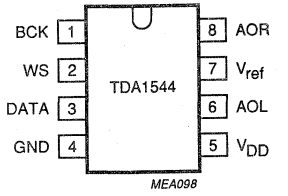


Fig.2(a) Pin configuration TDA1544.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

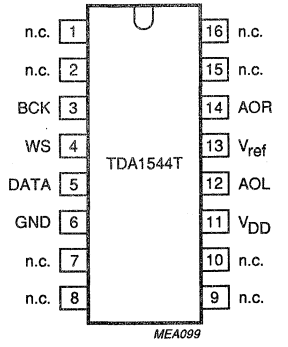
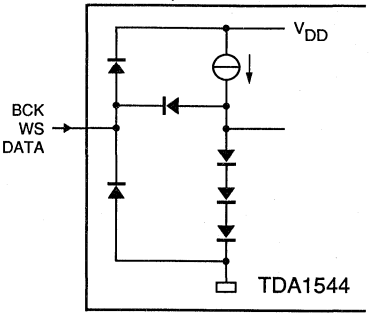
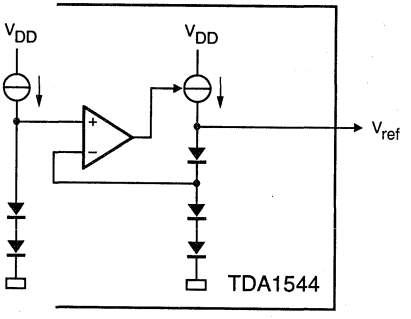


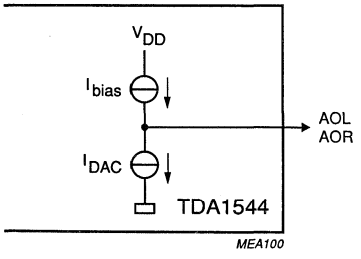
Fig.2(b) Pin configuration TDA1544T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1544 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Dual 16-bit low-noise DAC TDA1544

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
$V_{OC(AC)}$	output voltage compliance AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		2.7	3.0	3.3	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA V_{AO} = V_{ref}	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		0.95	1.00	1.05	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.05	2.20	2.35	V
I_{ref}	reference current output		−0.6	-	5.0	mA
THD	total harmonic distortion	including noise		−75	−70	dB
		at 0 dB; note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB; note 3, Fig.6	-	2.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio at bipolar zero	note 5	99	101	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

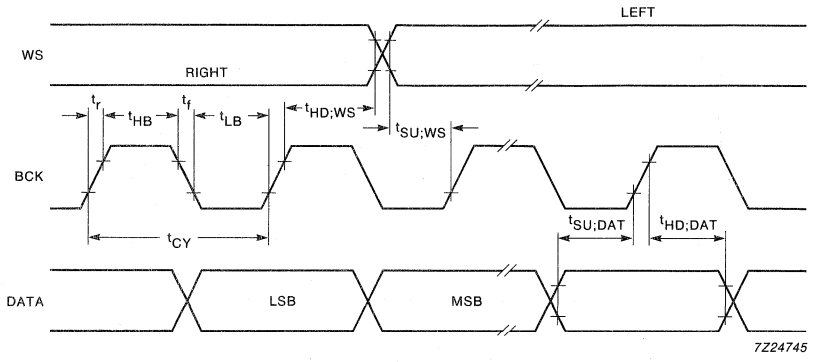


Fig.4 Format of input signals (Japanese format).

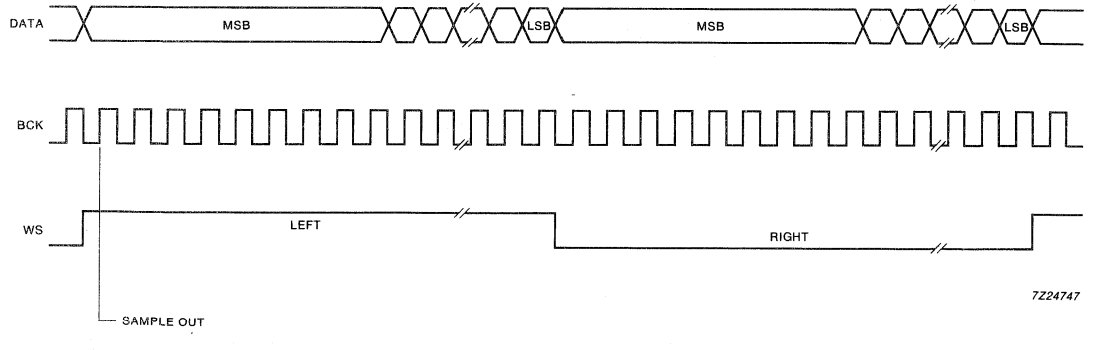
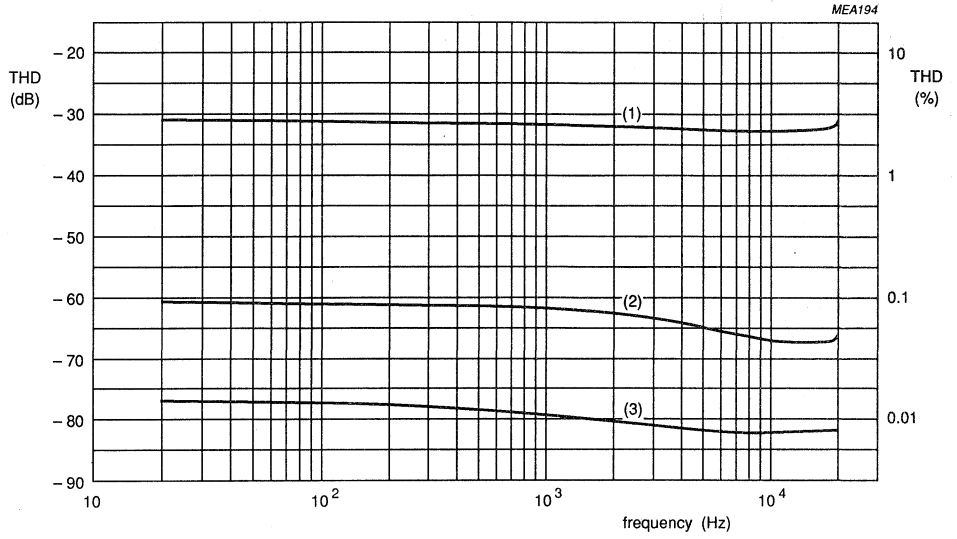


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.

PAL – NTSC ENCODER

GENERAL DESCRIPTION

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Features

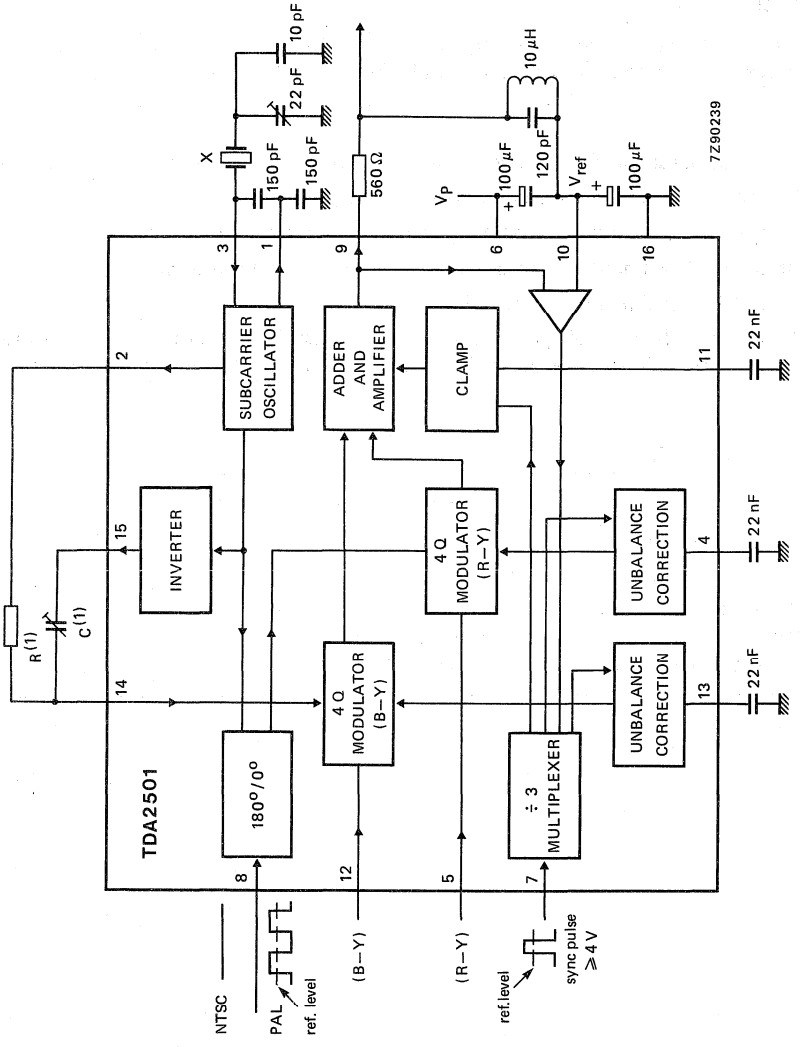
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output DC level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6)	V_P	5.5	6.8	10	V
Supply current range (pin 6)	I_P	28	40	64	mA
Chrominance output voltage (pin 9) (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2501 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2501T: 16-lead mini-pack; plastic (SO16L; SOT162A).



(1) R = 0.885 (2 π fC); for PAL f = 4.433 619 MHz, R = 963 Ω and C = 33 pF.

Fig.1 Block diagram; also test and application diagram.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1.4 volt are to be applied at pin 12 and pin 5. DC-coupling of the input signals is allowed if their DC levels are within specified limits from the DC level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input DC (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)**	reference voltage ▲ V_{10-16} (V)		
			min	typ.	max.
5.5	2.4	3.3	2.3	3.0	3.5
6.0	$> V_{ref} - 1.4$ V	3.8	2.4	3.3	3.9
7.0	$> V_{ref} - 1.4$ V	4.8	2.6	4.0	4.7
8.0	$> V_{ref} - 1.4$ V	5.8	2.8	4.8	5.5
9.0	$> V_{ref} - 1.4$ V	6.8	3.0	5.5	6.3
10.0	$> V_{ref} - 1.4$ V	7.8	3.2	6.3	7.1

* Minimum 2.4 V.
** At $V_S - 2.2$ V.
▲ Minimum values at $0.2\ V_S + 1.2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0.8\ V_S - 0.9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) DC-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is achieved by applying a HIGH level to pin 7 within the (LB–BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the DC components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to –150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is 0.885 (2π fC).

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this event the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generates the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the DC level must be the same as that of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 16)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.2		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

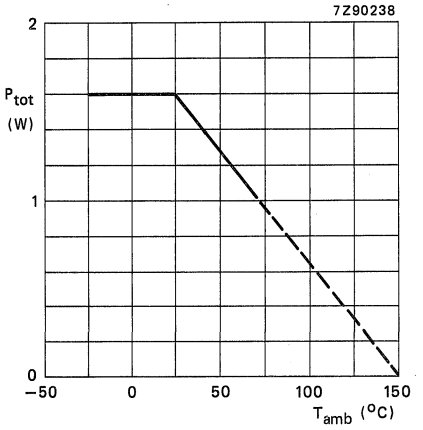


Fig.2 Power derating curve.

CHARACTERISTICS

$V_P = V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Single supply voltage	V_{6-16}	5.5	6.8	10	V
Dual supply voltage					
positive (pin 6)	V_{6-10}	2.0	3.0	5.0	V
negative (pin 16)	$-V_{16-10}$	2.3	3.0	5.0	V
Supply current (pin 10)	I_{10}	−1	0	3.5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 16)	$-I_{16}$	28	40	64	mA
Limitation DC level					
oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal (peak-to-peak value)					
pin 5	$V_{5(p-p)}$	–	1	1.4	V
pin 12	$V_{12(p-p)}$	–	1	1.4	V
Input voltages (R-Y) and (B-Y) zero DC level					
pin 5	V_5	2.4	3.3	3.9	V
pin 12	V_{12}	2.4	3.3	3.9	V
Required level of sync input					
HIGH	V_7	4	–	V_P	V
LOW	V_7	–	–	V_{10}	V
Required level of PAL pulse (H/2)					
HIGH	V_8	$V_{10}+0.8$	–	V_P	V
LOW	V_8	$-V_P$	–	0	V
Sync input current					
$V_7 = V_P + 1$ V	I_7	–	4	15	μA
PAL input current (H/2)					
$V_8 = V_{10} + 0.8$ V	I_8	–	1.5	5	μA
Chrominance output voltage swing (R-Y) = (B-Y) = 1.4 V; subcarrier pulse = 0.5 V (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Amplitude of suppressed subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1.5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1.5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1.5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2.3$ V	I_{14}	–	6	–	μA
Input impedance					
(R-Y)	Z_5	–	160	–	kΩ
(B-Y)	Z_{12}	–	160	–	kΩ

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506/T converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; $D'_R = -1{,}9$ (R-Y) and $D'_B = +1{,}5$(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506/T may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}		−25 to +70 °C
Storage temperature range	T_{stg}		−55 to +150 °C

PACKAGE OUTLINES

TDA2506: 24-lead DIL; plastic (with internal heat spreader) (SOT101B).
TDA2506T: 24-lead mini-pack; plastic (SO24; SOT137A).

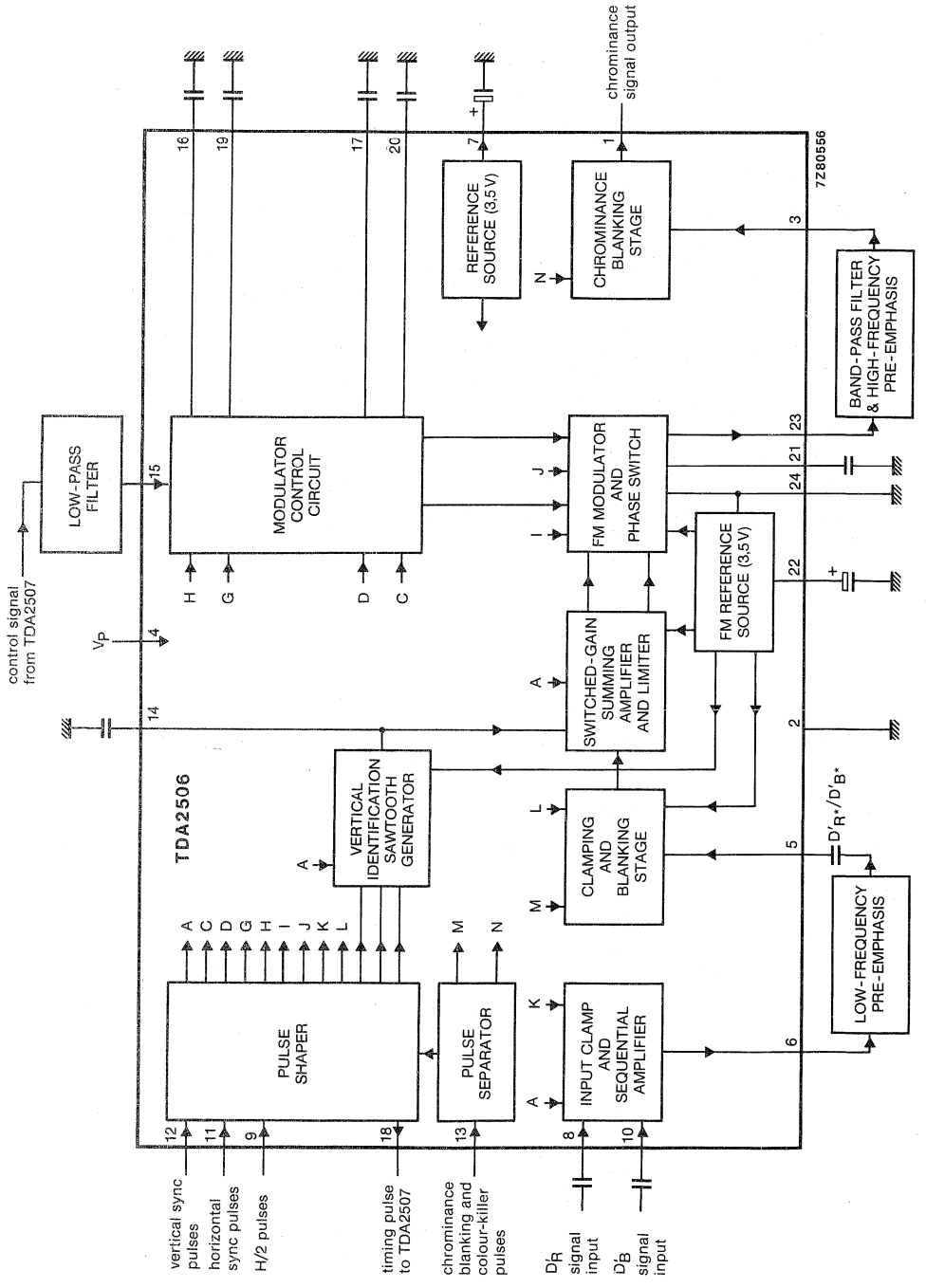


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired; should be connected to ground if not used).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz hold capacitor.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz hold capacitor.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential D'_R* and D'_B* signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

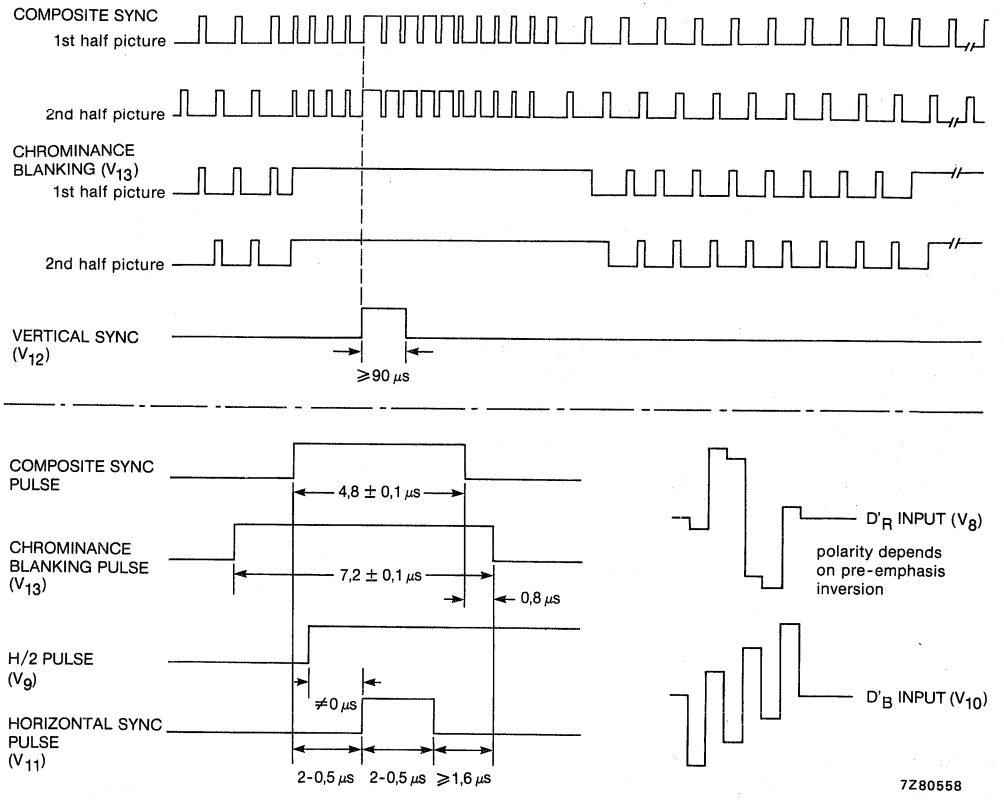


Fig. 2 Survey of input signals in relation to composite sync.

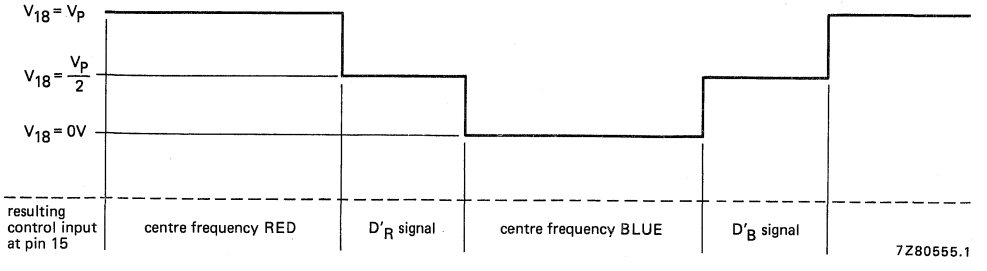


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,000 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0°, 180°, 0°, 180°, repeating;

horizontal scan (line to line) 0°, 0°, 180°, 0°, 0°, 180°, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

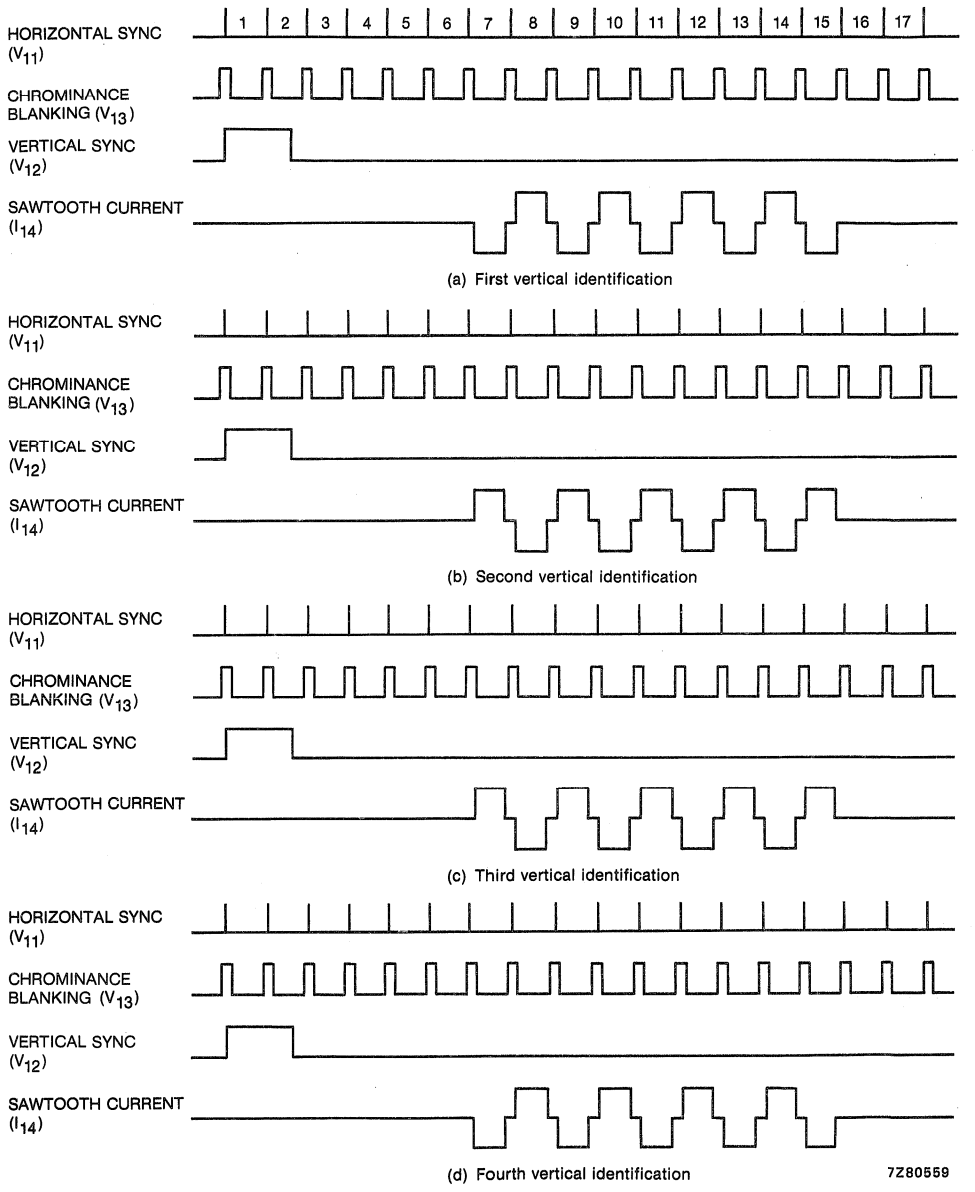


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Figs 5 and 6
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +150 °C

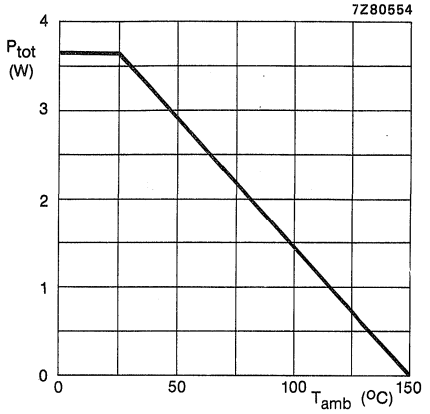


Fig. 5 Power derating curve for DIL package (SOT-101B).

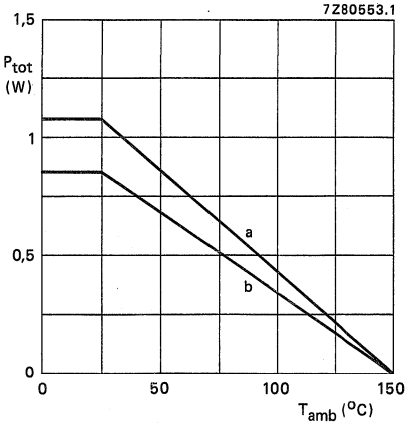


Fig. 6 Power derating curve.

a = device mounted on a ceramic substrate.
b = device mounted on a printed circuit board.

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4.75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3.4	3.55	3.7	V
Reference voltage (pin 22)	V_{22-24}	3.35	3.5	3.65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pins 9 and 12)	I_9, I_{12}	–	–	10	μA
Bias current (pin 11)	I_{11}	–	–	15	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2.5	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4.7	–	–	V
intermediate ($V_p/2$) level	V_{18}	2.2	2.5	2.8	V
low level	V_{18}	–	–	0.4	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3.6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1.7	1.8	1.9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level ($I_{14} = \pm 50$ μA	V_{14}	$V_{22}-15$ mV	V_{22}	$V_{22}+15$ mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	45	65	85	μA
Maximum voltage level	V_{14}	$V_{22}+0.5$	$V_{22}+0.7$	$V_{22}+0.8$	V
Minimum voltage level	V_{14}	$V_{22}-0.8$	$V_{22}-0.7$	$V_{22}-0.5$	V
Voltage level during line blanking	V_{14}	$V_{22}-7$ mV	V22	$V_{22}+7$ mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7-25 mV	V7	V_7+25 mV	V
Input bias current	I_8, I_{10}	–	–	1.5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 AC coupled to fixed DC voltage)					
DC output	V_6	1.6	$\frac{V_7}{2}$ − 10 mV	1.85	V
Output resistance	R_6	–	8	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10-6}$	1.4	1.5	1.6	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	V_{22} − 12 mV	V_{22}	V_{22} + 12 mV	V
Input bias current ($V_5 = V_{22}$)	I_5	–	–	2.5	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current ($V_{15} = V_7$)	I_{15}	–	–	1.25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4.3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	80	Ω
High DC output level at V_{21} = 3.8 V	V_{23}	V_{22} − 0.85	–	V_{22} − 0.7	V
Output signal amplitude	V_{23}	0.9	1.0	1.15	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current ($V_3 = V_7$)	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required DC level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	10	Ω
Temperature coefficient of output DC level	V_1/T	–	1.8	—	mV/K
Amplifier gain	$\Delta V_1/\Delta V_3$	1.69	1.75	1.79	
Output DC level during blanking(V_{13} = HIGH)	V_1	V_7–0.88	V_7–0.79	V_7–0.70	V
Output DC level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0.88	V_7–0.79	V_7–0.70	V

A.C. CHARACTERISTICS

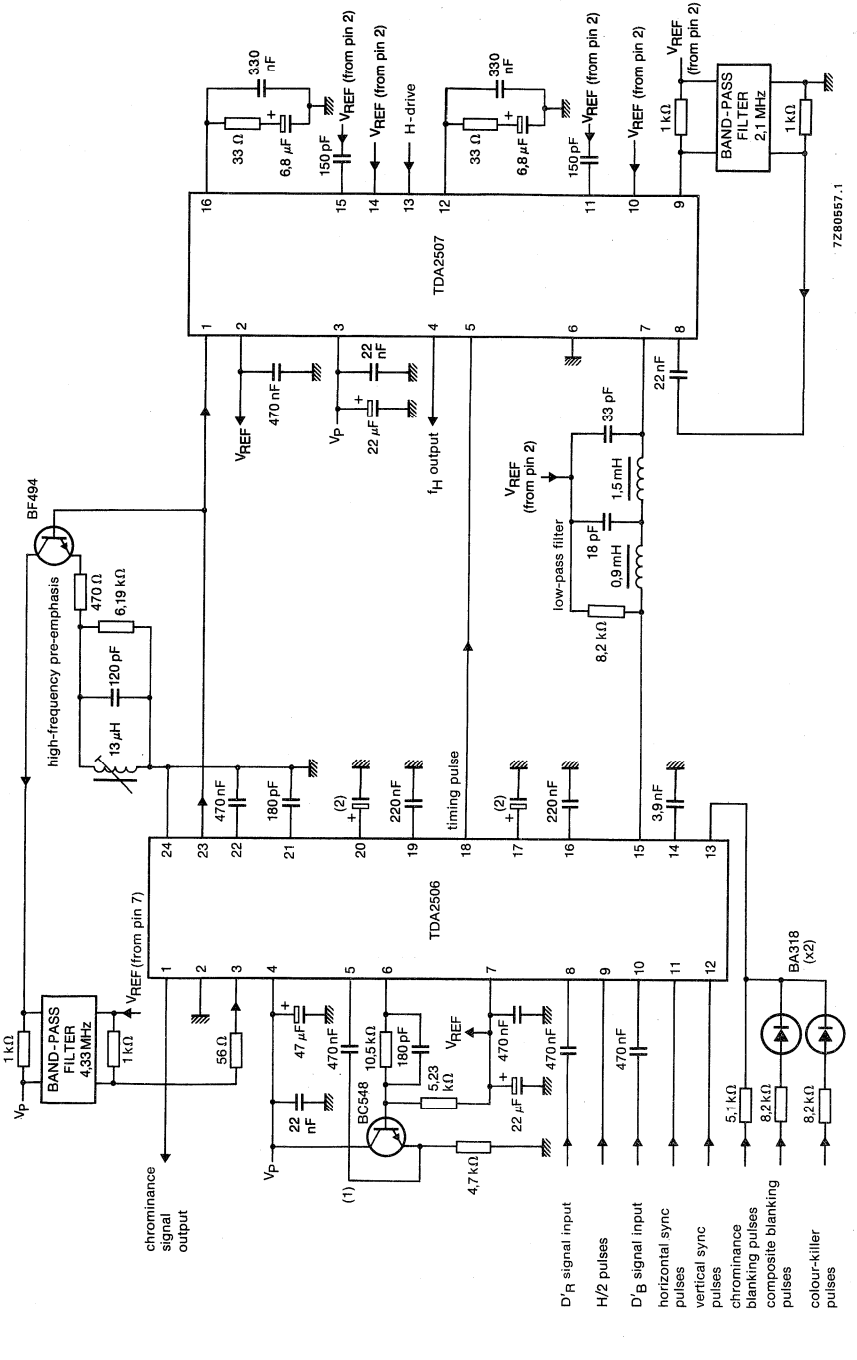
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 12	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 12	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 12	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 12	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 7 Application using TDA2507 with PLL tuning: $V_P = 5$ V.

FM MODULATOR CONTROLLER

GENERAL DESCRIPTION

The TDA2507 accepts FM signals that are sequentially modulated by two alternating subcarrier frequencies (SECAM signals) and provides sequential DC output levels to control the FM modulator.

The IC is intended for use with the SECAM encoder TDA2506 but can be adapted for other applications. Timing reference pulses from the modulator are required.

Two frequency reference phase-lock loops are contained within the IC; one for 4.40625 MHz, and one for 4.250 MHz. Other frequencies can be accomplished by using external reference sources.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-6}$	4.75	5.0	7.0	V
Supply current	V_P = 5 V; both PLL circuits on	I_3	–	40	–	mA
Reference voltage		V_{2-6}	3.34	3.45	3.56	V
Storage temperature range		T_{stg}	−55	–	+150	°C
Operating ambient temperature range		T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2507 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2507T: 16-lead mini-pack; plastic (SO16L; SOT162A).

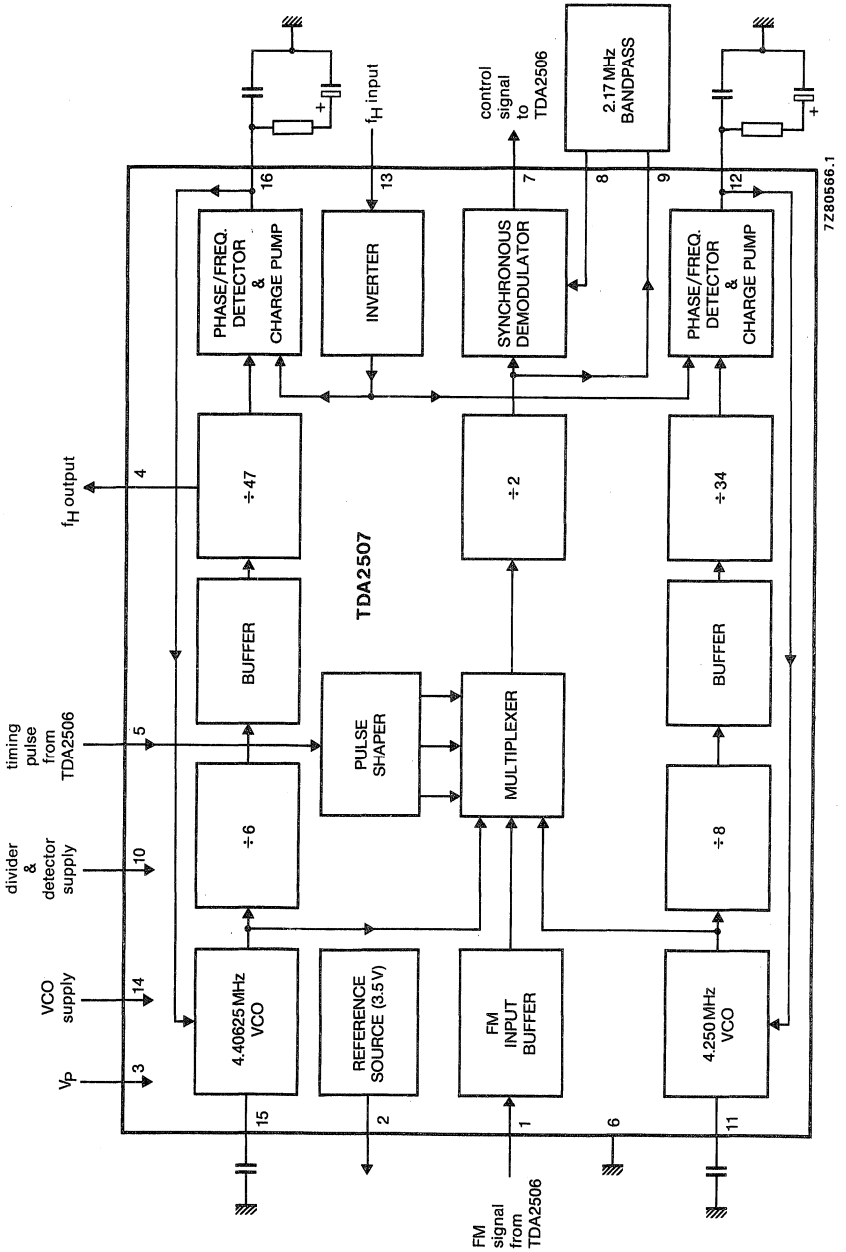


Fig.1 Block diagram.

PINNING

Pin functions

pin	description
1	FM signal input (from TDA2506)
2	Reference voltage output
3	Positive supply voltage
4	Horizontal sync output (f_H = 4 406.250/282 = 15.625 kHz)
5	Timing pulse input (from TDA2506)
6	Ground
7	Control signal output to TDA2506 via low-pass filter
8	Input to synchronous demodulator from band-pass filter
9	Output to band-pass filter
10	Supply voltage for the divider stages and phase/frequency detectors of the two phase-lock loops (PLL)
11	Tuning capacitor for the 4.250 MHz reference oscillator
12	Filter for the phase/frequency detector of the 4.250 MHz phase-lock loop
13	Horizontal sync input (f_H)
14	Supply voltage for the two reference oscillators
15	Tuning capacitor for the 4.40625 MHz reference oscillator
16	Filter for the phase/frequency detector of the 4.40625 MHz phase-lock loop.

FUNCTIONAL DESCRIPTION

Phase-lock loops

The two phase-lock loops each comprise a voltage-controlled reference oscillator, two frequency divider stages and a phase/frequency detector circuit. The loops are closed by charge pumping the reference oscillators from the phase/frequency detector outputs. The centre frequencies of the loops are set by external capacitors at pin 15 (4.40625 MHz) and pin 11 (4.250 MHz). The divider stages which follow the reference oscillators reduce the frequencies of both the loops to 15.625 kHz (f_H) at their respective inputs to the phase/frequency detectors. The reference signals to both phase/frequency detectors are obtained from the horizontal sync input at pin 13.

The divider and phase/frequency detector circuits can be switched off by connecting pin 10 to ground. This leaves only the VCO of each PLL in circuit and allows external signals to be injected at pins 15 and 11, or crystals to be used for tuning the oscillators.

The accuracy of crystal tuning using only one crystal can be obtained by connecting pins 10, 14 and 16 to the reference voltage at pin 2 and connecting a 4.40625 MHz crystal to pin 15. The 4.250 MHz PLL will follow the crystal-derived f_H reference from pin 4 via pin 13 and its phase/frequency detector.

Multiplexer and pulse shaper

The multiplexer receives the 4.40625 and 4.250 MHz reference frequencies from the two VCOs and the FM signals $D'_R{}^*$ and $D'_B{}^*$ from the TDA2506 modulator. The signals are gated one at a time to the multiplexer output in a sequence determined by the timing pulses from TDA2506. The levels of the timing pulses (pin 5) are used in the pulse shaper to generate enable pulses for the multiplexer (see Figs 2 and 3). The multiplexer output sequence is as follows:

4.40625 MHz (2 lines); $D'_R{}^*$ FM signal (1 line); 4.250 MHz (2 lines); $D'_B{}^*$ FM signal (1 line); repeating. The selection of $D'_R{}^*$ or $D'_B{}^*$ FM signal is a feature of the timing of the input at pin 5.

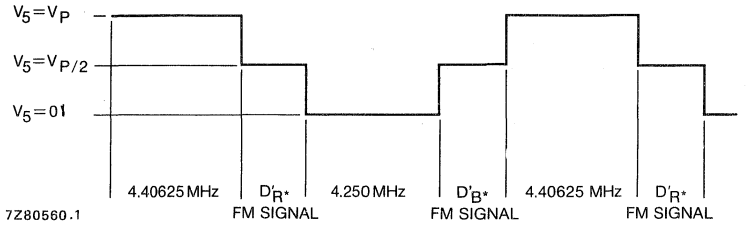


Fig.2 Timing pulse waveform for multiplexer output sequence.

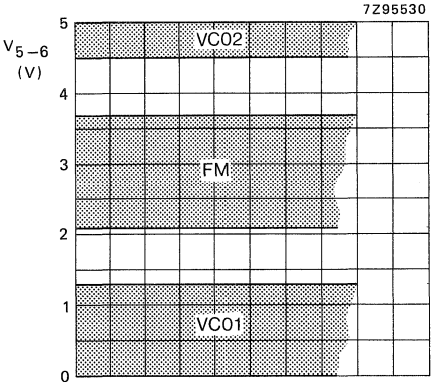


Fig.3 Switching levels of the timing pulse at pin 5.

Divide-by-two stage and synchronous demodulator

The divide-by-two stage halves the frequencies present in the multiplexer output and equalizes the amplitude and pulse shapes of the sequential signals.

Demodulation of the multiplexed signal is performed by filtering the signal via a 2.17 MHz band-pass filter (between pins 8 and 9) and using this filtered signal as a synchronous switch for the main signal. The DC level of the signal from pin 9 is referred externally to the reference voltage from pin 2. An external low-pass filter is required for the output signal from pin 7.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.4		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

CHARACTERISTICS

$V_P = V_{3-6} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3)		V_P	4.75	5.0	7.0	V
Supply current	$V_{14} = V_{10} = V_2$	I_P	–	35	–	mA
Supply current	$V_{14} = V_2$	I_P	–	20	–	mA
Reference voltage (pin 2)		V_{2-6}	3.34	3.45	3.56	V
Phase-lock loops						
DC voltage output level						
pin 11		V_{11-6}	2.4	2.6	2.8	V
pin 15		V_{15-6}	2.4	2.6	2.8	V
Amplitude of oscillation (peak-to-peak value)						
pin 11		$V_{11(p-p)}$	–	130	–	mV
pin 15		$V_{15(p-p)}$	–	130	–	mV
Input current	see Fig.5					
pin 11	$V_{12-6} = 1.5$ V	I_{11}	–	130	–	μA
pin 15	$V_{16-6} = 1.5$ V	I_{11}	–	130	–	μA
Limiting values for VCO control voltages						
pin 12		V_{12}	0.8	–	1.9	V
pin 16		V_{16}	0.8	–	1.9	V
Output resistance at pin 4	V_4 = HIGH	R_4	5.1	6.8	8.5	kΩ
Input resistance at pin 13		R_{13}	200	–	–	kΩ
Amplitude of f_H pulse required at pin 13	note 1	V_{13}	2	–	–	V
FM input buffer (pin 1)						
Input resistance		R_1	180	–	–	kΩ
Switching level of FM input		V_1	2.2	2.3	2.4	V
Required input amplitude		V_1	0.5	–	2.0	V
Pulse shaper input (pin 5)						
Input resistance		R_5	200	–	–	kΩ
Demodulator						
Sink current at pin 9 into divide-by-two circuit	V_9 = LOW	I_9	0.6	0.9	1.2	mA
Demodulator input bias voltage at pin 8		V_8	1.60	1.68	1.76	V
Demodulator output current from pin 7	see Fig.6					
output current at A		$-I_7$	0.6	0.9	1.2	mA
output current at B		I_7	1.2	0.9	0.6	mA

Note to the characteristics

1. Duty factor and timing not important.

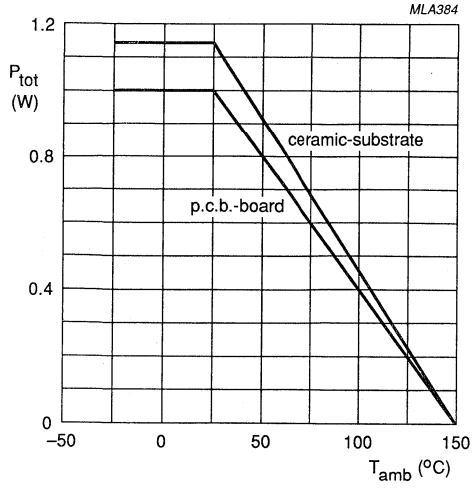


Fig.4a Power derating curve (TDA2507).

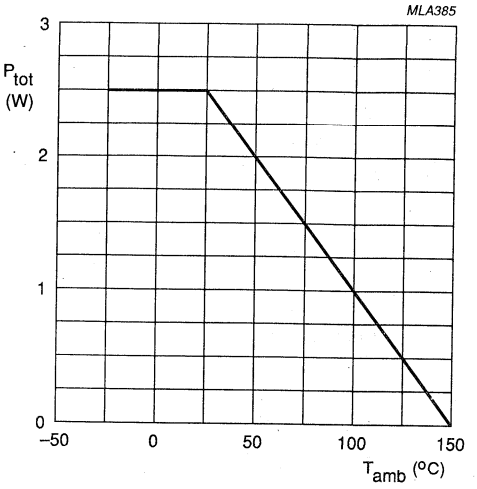


Fig.4b Power derating curve (TDA2507T).

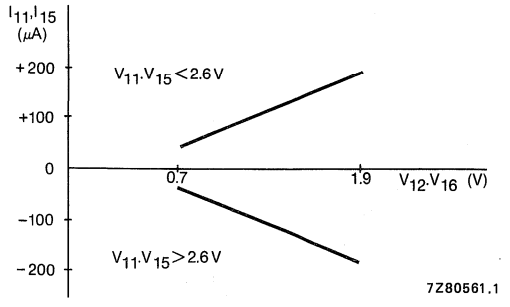


Fig.5 Current input to pins 11 and 15 as a function of voltage at pins 12 and 16 (typical values).

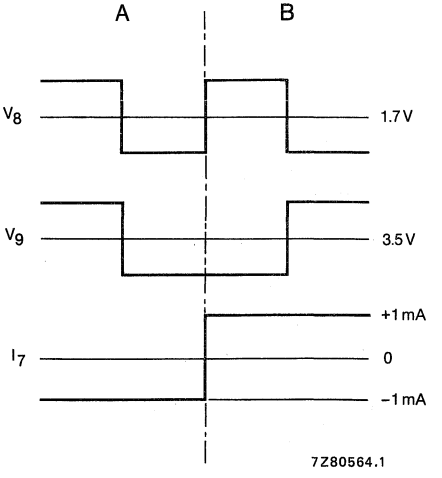


Fig.6 Demodulator output current from pin 7 (typical values).

APPLICATION INFORMATION (continued)

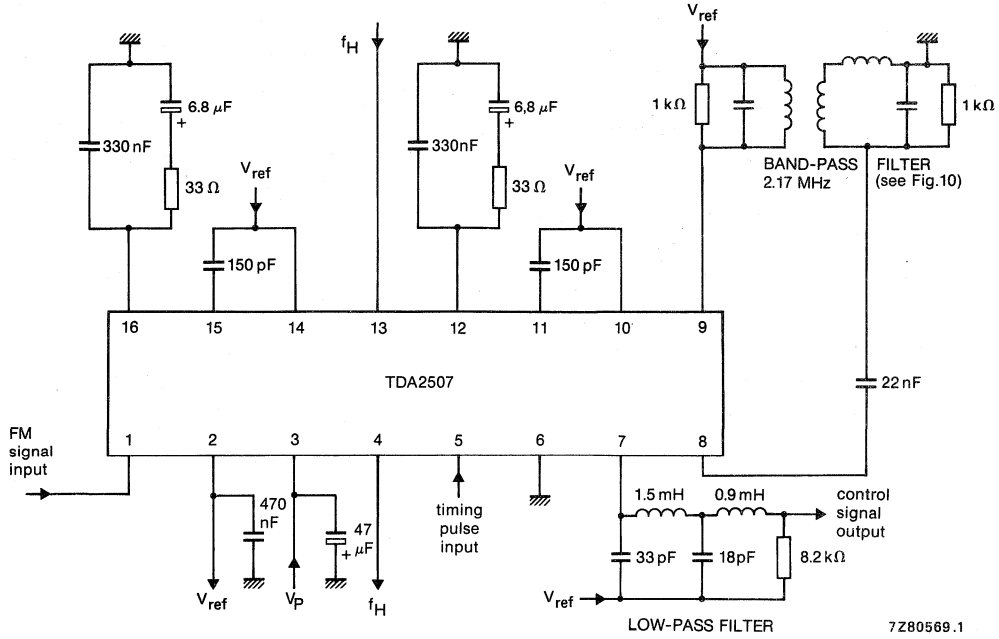


Fig.7 Application diagram using PLL tuning; V_P = 5 V.

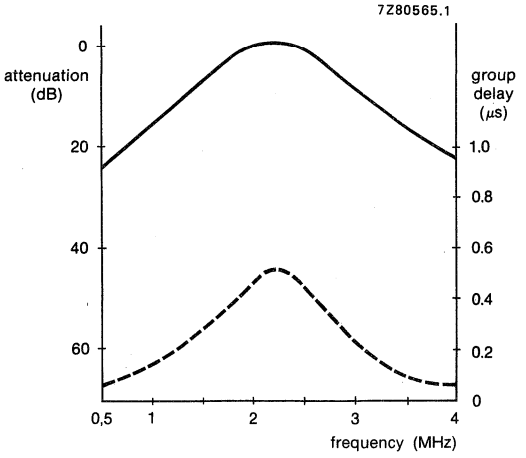


Fig.8 Typical response of 2.17 MHz band-pass filter.

DUAL FM MODEM FOR VHS HIFI AUDIO SYSTEM

GENERAL DESCRIPTION

The TDA2515 is a dual FM modulator/demodulator for processing the FM audio signal (stereo or bilingual) in VHS video recorders. The device has two channels, A and B, which are tested at 1.4 and 1.8 MHz respectively.

Features

The following features (in sequence) are used for recording and apply to both channels.

- An AF buffer amplifier
- An adjustable AF limiter
- An AF driven Current Controlled Oscillator (CCO)
- An HF output buffer

The following features (in sequence) are used for playback and also apply to both channels.

- An HF amplifier limiter
- A Phase Locked Loop (PLL) detector with CCO and filter section
- A voltage to current converter
- An AF amplifier with Sample and Hold (S & H) circuit

Further features are:

- An internal voltage stabilizer
- An HF level detector (in channel A)
- A mute timing and delay circuit (in channel A)
- A record/playback switch (connected to channels A and B)
- A logic circuit for mute and mute enable
- A pulse shaper, driven by the Head Identification (HID) signal, to generate the hold pulse for the S & H circuits (channels A and B)

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Operating supply voltage		V_P	4.75	5	5.25	V
Supply current						
playback	$V_{22} \leqslant 1.5$ V	I_P	–	50	60	mA
recording	$V_{22} \geqslant 3.5$ V	I_P	–	35	40	mA

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

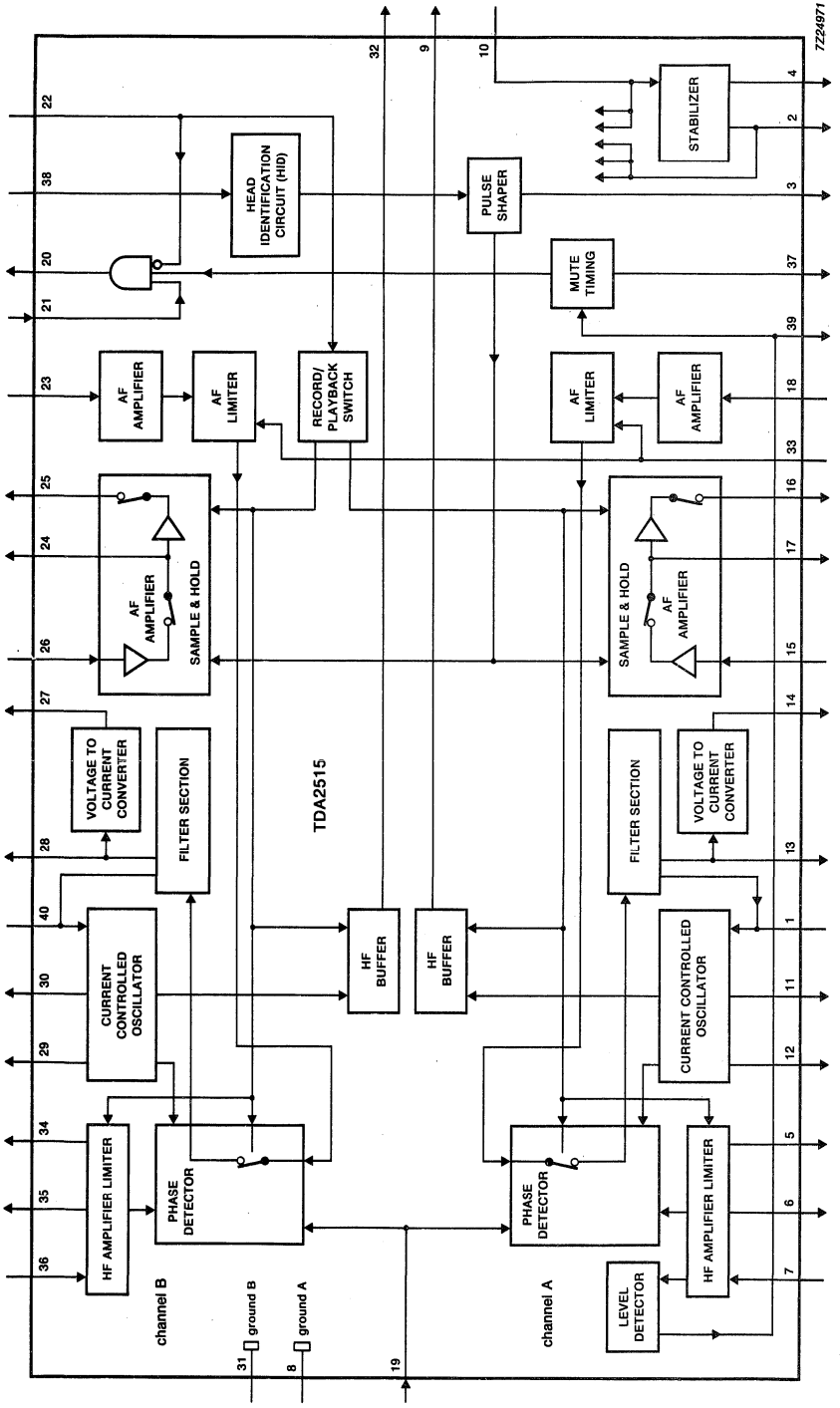


Fig.1 Block diagram.

PINNING

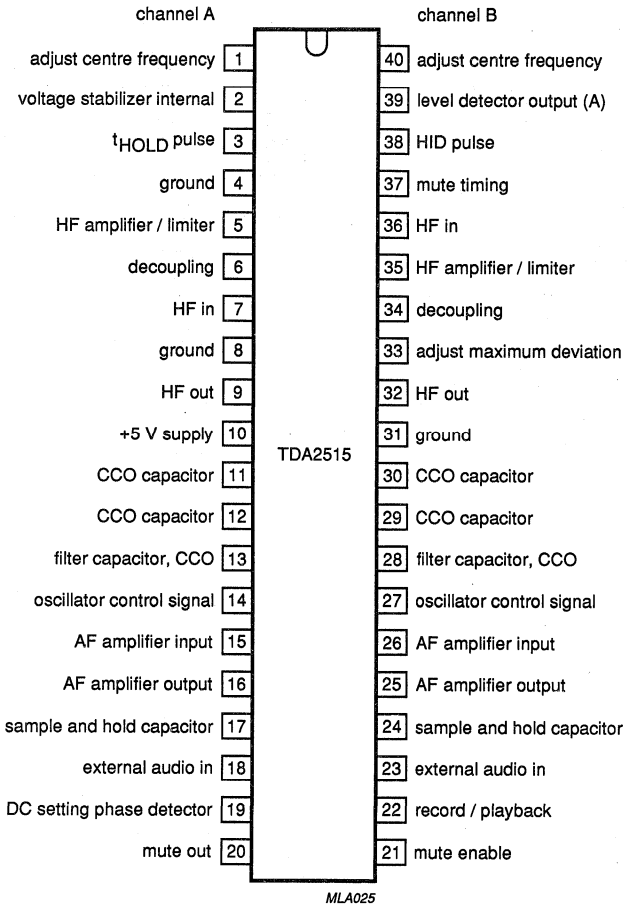


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134). All voltages with reference to pin 8; all currents positive into the device.

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 10)	V_P	0	–	6	V
Voltage on all pins	V	0	–	V_P	V
Total power dissipation	P_{tot}		see Fig.3		
Operating ambient temperature range	T_{amb}	−20	–	+70	°C
Storage temperature range	T_{stg}	−65	–	+150	°C

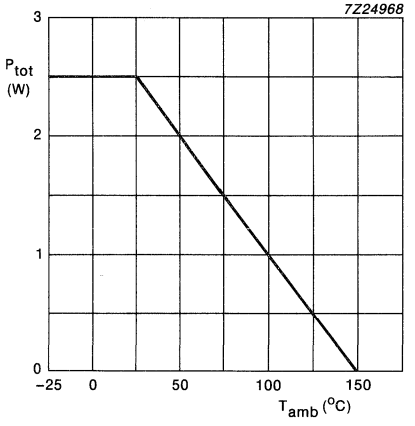


Fig.3 Power derating curve.

DC CHARACTERISTICS

According to the test set-up illustrated by Fig.4; V_P = 5 V; T_{amb} = 25 °C; unless otherwise specified; pins 31 and 4 connected to pin 8. All voltages with respect to pin 8.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_P	4.75	5	5.25	V
Supply current						
playback	$V_{22} \pm 1.5$ V	I_P	–	50	60	mA
record	$V_{22} \pm 3.5$ V	I_P	–	35	40	mA
difference playback/recording		$\lvert\Delta I_P\rvert$	–	15	25	mA
Total power dissipation						
playback	$V_{22} \pm 1.5$ V	P_{tot}	–	250	–	mW
record	$V_{22} \pm 3.5$ V	P_{tot}	–	175	–	mW
Voltage on pins 1 and 40		$V_{1,40}$	–	1.9	–	V
Voltage on pin 2	note 1	V_2	2.4	2.5	2.6	V
Voltage on pins 5 and 34	note 2	$V_{5,34}$	–	3.3	–	V
Voltage on pins 6 and 35	note 2	$V_{6,35}$	–	3.3	–	V
Voltage on pins 13 and 28		$V_{13,28}$	–	1.9	–	V
Voltage on pins 15 and 26		$V_{15,26}$	–	2.5	–	V
Voltage on pins 16 and 25	note 2	$V_{16,25}$	–	2.4	–	V
Voltage on pins 18 and 23		$V_{18,23}$	–	2.5	–	V
Voltage on pin 19		V_{19}	–	1.9	–	V
Voltage on pins 14 and 27		$V_{14,27}$	–	1.2	–	V
Voltage on pin 33		V_{33}	–	2.5	–	V
Current supplied from pin 2		$-I_2$	–	–	1	mA

Notes to DC characteristics

1. Temperature drift V_{ref} = typically 50 μV/°C.
2. Playback ($V_{22} \leqslant 1.5$ V).

AC CHARACTERISTICS

All voltages with reference to pin 8.

parameter	conditions	symbol	min.	typ.	max.	unit
Recording circuit	AF input frequency = 1 kHz; $V_{22} \geqslant 3.5$ V					
Overall performance						
Total harmonic distortion of HF	Δf = 50 kHz	THD	–	0.2	–	%
	Δf = 150 kHz; note 1	THD	–	0.4	0.6	%
External audio current (pins 18 and 23)	Δf = 150 kHz	I_I	25	30	33	μA
Maximum deviation setting (pin 33)	R13 = V_{ref}/I_I	Δf	–	150	–	kHz
difference (in channel)		$\pm\Delta f$	–	–	7.5	kHz
difference of channels A and B		$\pm\Delta f$	–	–	7.5	kHz
High frequency output stage						
Output voltage (pin 9) (peak-to-peak)		V_O	0.43	0.5	0.57	V
Output voltage (pin 32) (peak-to-peak)		V_O	1.3	1.51	1.73	V
Current difference	$I_{32}/I_9 = 3\,(1+\Delta)$	$\lvert\Delta\rvert$	–	–	6	%
Output resistance (pin 9)		$R_{9\text{-}10}$	400	500	600	Ω
Output resistance (pin 32)		$R_{32\text{-}10}$	400	500	600	Ω
Second harmonic suppression			–	48	–	dB
Intermodulation						
channel B to A		IM	–	–40	–	dB
channel A to B		IM	–	–40	–	dB
Ripple rejection	note 2	RR	–	40	–	dB
Playback circuit	input frequency = 1.4 or 1.8 MHz; Δf = 150 kHz and f_{mod} = 1 kHz; $V_{22} \leqslant 1.5$ V					
HF amplifier/limiter/PLL						
Input conductance		g_{ie}	–	1	–	μS
Input capacitance		C_{ie}	–	4	–	pF
Sensitivity	PLL locked	V_{IHF}	–	100	300	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Signal-to-noise ratio	note 3					
	V_{IHF} = 300 μV	S/N	–	50	–	dB
	V_{IHF} = 10 mV	S/N	–	60	–	dB
AM rejection	note 4					
	V_{IHF} = 1 mV	AMR	–	53	–	dB
	V_{IHF} = 10 mV	AMR	–	58	–	dB
Current controlled oscillator (CCO)						
CCO frequency (adjustable)	note 5	f_{CCO}	–	1.4	–	MHz
		f_{CCO}	–	1.8	–	MHz
Input current (internal)	Δf = 150 kHz	I_{p-p}	25	30	33	μA
Lock range (deviation from f_{CCO}, channels A and B)	V_I = 10 mV	Δf_{CCO}	–	±550	–	kHz
Temperature coefficient		TC	–	−250	–	$10^{-6}/^{o}C$
PLL demodulator circuit						
Phase response time	Δφ = 90 deg	t_s	–	4.5	–	μs
Phase detector current		$\|I_{PD}\|$	–	106	–	μA
Ratio of $+I_{PD}$/(sum of loop filter resistors)			6	10	14	nA/Ω
Output voltage at pins 14 and 27 (RMS value)	±Δf = 150 kHz	V_O	–	105	–	mV
Buffer amplifier and sample and hold circuit						
Input resistance		$R_{15,26}$	–	50	–	kΩ
Load resistor		$R_{16,25}$	2.5	–	–	kΩ
Voltage gain		G_v	–	20	–	dB
DC shift during hold pulse		V_{DCpeak}	–	3	8	mV
Hold time pulse from pulse shaper	note 6;Fig.5	t_{HOLD}	3.8	4.5	5.2	μs
Delay of HID pulse to hold pulse	Fig.5	t_D	0.35	1	1.2	μs
HID crosstalk $V_{38-16,25}$		$V_{(p-p)}$	–	0.4	–	mV
Overall performance	without S & H; V_{IHF} = 10 mV					
Output voltage (RMS value)		$V_{16,25}$	0.75	0.85	1.0	V
Signal-to-noise ratio	note 3	S/N	50	60	–	dB
Total harmonic distortion + noise		THD + N	–	0.2	0.6	%

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Level detector circuit						
Level detector output	V_{IHF} = 1 mV	V_{odc}	1.2	1.8	2.8	V
	V_{IHF} = 10 mV	V_{odc}	2.4	3.0	3.7	V
	V_{IHF} = 100 mV	V_{odc}	3.8	4.4	4.9	V
Mute activated		V_{IHF}	1.25	2.2	3.75	mV
Output resistance (internal)		R_{39-8}	–	10	–	kΩ
Head identification circuit	HID pulse = 25 Hz 50% duty factor					
Input voltage (pin 38)						
HIGH		V_{IH}	2.75	–	–	V
LOW		V_{IL}	–	–	2.25	V
Input current (pin 38)						
HIGH	V_I = 5 V	I_{IH}	–	–	0.2	μA
LOW	V_I = 0.3 V	I_{IL}	–	–	10	μA
Logic circuit						
Record, playback (pin 22)						
Playback voltage		V_{IL}	–	–	1.5	V
Playback current	V_I = 0 V	I_{IL}	65	–	400	μA
Record voltage		V_{IH}	3.5	–	–	V
Record current	V_I = 5 V	I_{IH}	–	–	14	μA
Mute enable FM (pin 21)						
HIGH (mute enabled)		V_I	1	–	–	V
Input current	V_I = 1 V	I_I	20	37	60	μA
LOW (mute disabled)	I_I = 0 A	V_I	–	–	0.5	V
Mute output (pin 20)						
HIGH	I_O = –0.4 mA	V_O	4	–	–	V
LOW	I_O = 0.4 mA	V_O	–	–	0.5	V
Level detector mute	$V_{IHF} < 1.25$ mV; V_{21} = 1 V	V_O	4	–	–	V
Mute delay (pin 37)	$V_{21} \geqslant 1$ V; $V_{22} \leqslant 1.5$ V					
Switch off (signal to no signal)		t_{OFF}	–	15	–	ms
Switch on (no signal to signal)		t_{ON}	–	400	–	ms

Notes to AC characteristics

1. Maximum deviation adjusted for 165 kHz.
2. $V_{ripple} = 10\,mV$; with respect to $\Delta f = 150\,kHz$.
3. AF bandwidth of 300 Hz to 15 kHz.
4. FM: f_{mod} = 1 kHz; Δf = 150 kHz
   AM: f_{mod} = 400 Hz; m = 0.3
5. For f_{CCO} = 1.4 MHz, R5 = 5.6 kΩ ± 5%;
   RT = R5 + R7 = 7.7 kΩ (nom.)
   For f_{CCO} = 1.8 MHz, R6 = 3.3 kΩ ± 5%;
   RT = R6 + R8 = 5.8 kΩ (nom.)
   with C7 and C8 = 470 pF ± 5%; R7 and R8 = 4.7 kΩ (potentiometers).
6. With fixed resistor and fixed capacitor (R15 = 10 kΩ; C23 = 680 pF; 1% tolerance).

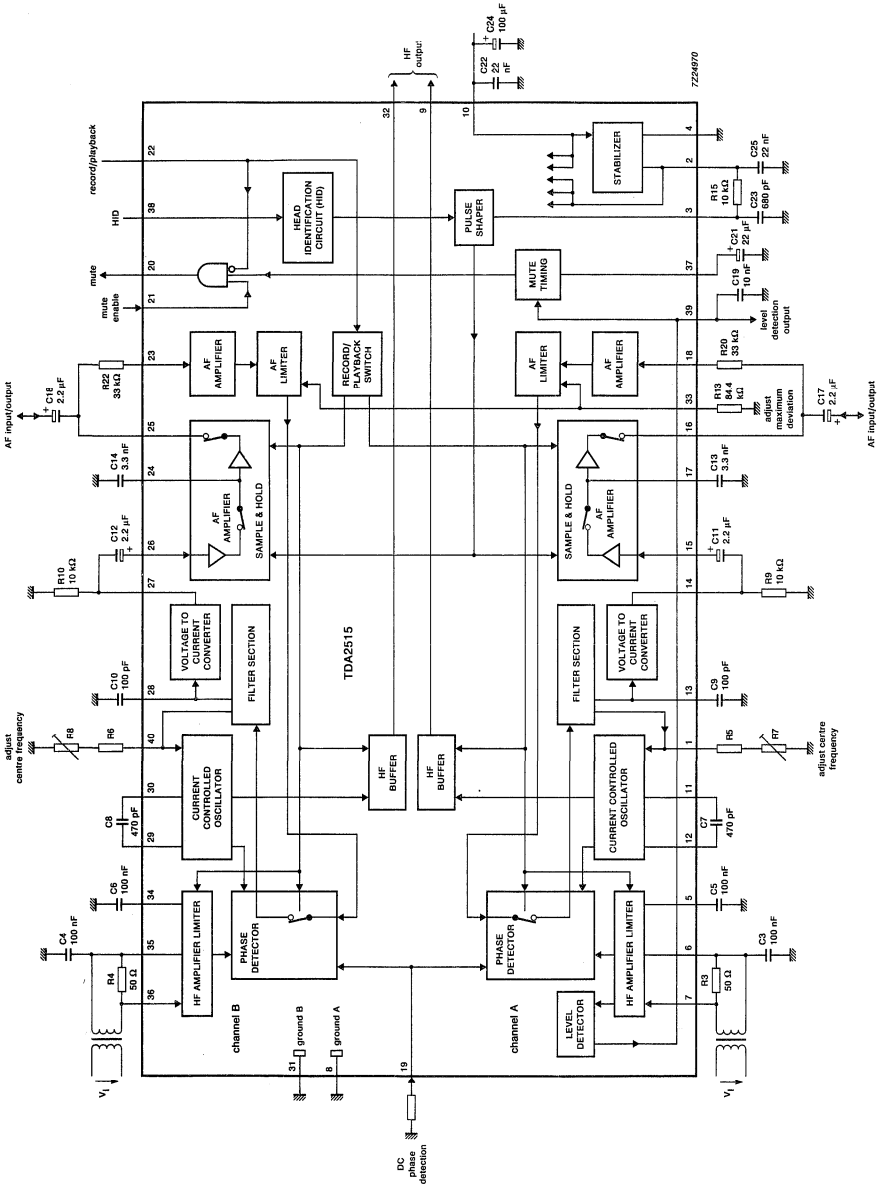


Fig.4 Test set-up diagram.

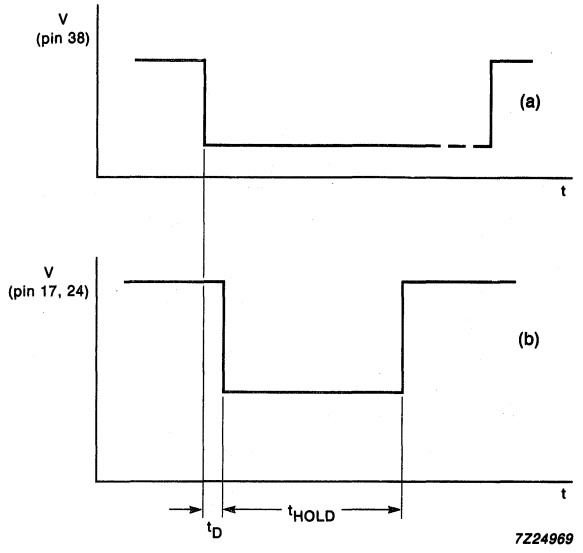


Fig.5 (a) Head identification pulse (HID) (b) Hold pulse.

AM SOUND I.F. CIRCUIT FOR FRENCH STANDARD

GENERAL DESCRIPTION

The TDA2543 is a monolithic integrated AM sound i.f. circuit in television receivers for the French standards L and L'.

The circuit incorporates the following functions:

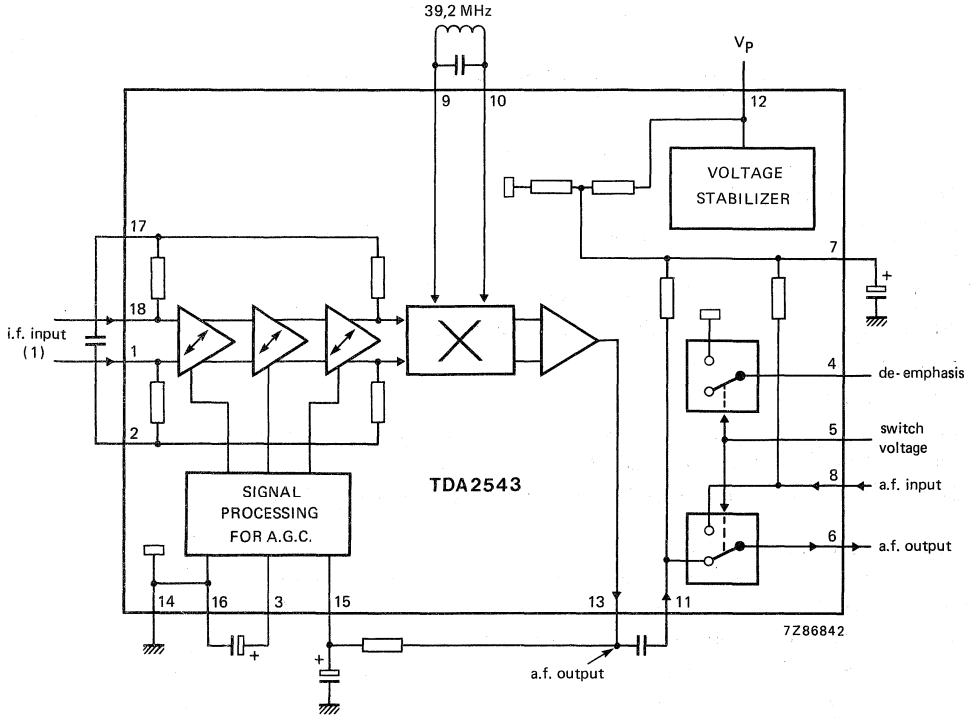
- 3-stage gain controlled i.f. amplifier, providing complete i.f. gain
- Synchronous AM demodulator
- A.G.C. circuit
- Audio input circuit with two external audio inputs and switching facilities to provide for either the demodulated i.f. or an external signal output
- Demodulated i.f. output is available from the input of the switching circuit

QUICK REFERENCE DATA

Supply voltage (pin 12)	$V_{12\text{-}14} = V_P$	typ.	12 V
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)} = 480$ mV	$V_{VC1\text{-}18(rms)}$	max.	30 μV
I.F. control range	ΔG_v	min.	60 dB
A.F. output voltage (r.m.s. value)	$V_{13\text{-}14(rms)}$	typ.	680 mV
Distortion at $V_{VC1\text{-}18(rms)} = 5$ mV	d_{tot}	max.	1 %
Signal-to-weighted-noise ratio according to CCIR 468	S + N/N	min.	50 dB
Maximum signal amplitude for the a.f. switch (r.m.s. value)	$V_{8;11\text{-}14(rms)}$	min.	2 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 12)	$V_{12-14} = V_P$	max.	13,2 V
Switch voltage (pin 5)	V_{5-14}	max.	V_P V
Current at pin 4	I_4	max.	5 mA
	$-I_4$	short-circuit proof	
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; input signal (vision carrier V.C.) with f_{VC} = 39,2 MHz; sound carrier (S.C.) modulated with f_m = 1 kHz and m = 0,8; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range (pin 12)	V_P	10,8	–	13,2	V
Supply current (pin 12)	I_P	–	50	–	mA
I.F. input (pins 1 and 18)					
Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)}$ = 480 mV	$V_{VC1\text{-}18(rms)}$	–	–	30	μV
Maximum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1\text{-}18(rms)}$	–	50	–	mV
Input resistance	$R_{1\text{-}18}$	–	2	–	kΩ
Input capacitance	$C_{1\text{-}18}$	–	2	–	pF
I.F. control range (–3 dB)	ΔG_v	60	–	–	dB
A.F. output (pin 13)					
A.F. output voltage (r.m.s. value) at $V_{VC1\text{-}18(rms)}$ = 5 mV	$V_{13\text{-}14(rms)}$	–	680	–	mV
Output resistance	$R_{13\text{-}14}$	–	100	–	Ω
Distortion at $V_{VC1\text{-}18(rms)}$ = 5 mV	d_{tot}	–	–	1	%
Signal-to-weighted-noise ratio at a.f. output (pin 13) according to CCIR 468 at $V_{VC1\text{-}18(rms)}$ = 5 mV	S + N/N	50	–	–	dB
A.F. switch (pins 8, 11 and 6)					
Maximum input voltage (r.m.s. value)	$V_{8\text{-}14(rms)}$	2	–	–	V
	$V_{11\text{-}14(rms)}$	2	–	–	V
Voltage gain	G_v	–	0 ± 1	–	dB
Amplitude frequency response (–3 dB)	f	20	–	20 000	Hz
Crosstalk between the non-switched input and the output	α	60	–	–	dB
Input resistance	$R_{8;\ 11\text{-}14}$	10	–	–	kΩ
Output resistance	$R_{6\text{-}14}$	–	400	–	Ω
De-emphasis switch (pin 4)					
Input resistance for:					
ON ($V_{5\text{-}14} > 3$ V)	$R_{4\text{-}14}$	–	–	200	Ω
OFF ($V_{5\text{-}14} < 1$ V)	$R_{4\text{-}14}$	100	–	–	kΩ
Switch voltage (pin 5)					
A.F. switch ON (pin 8 switched)	$V_{5\text{-}14}$	3	–	V_P	V
A.F. switch OFF (pin 11 switched)	$V_{5\text{-}14}$	0	–	1	V

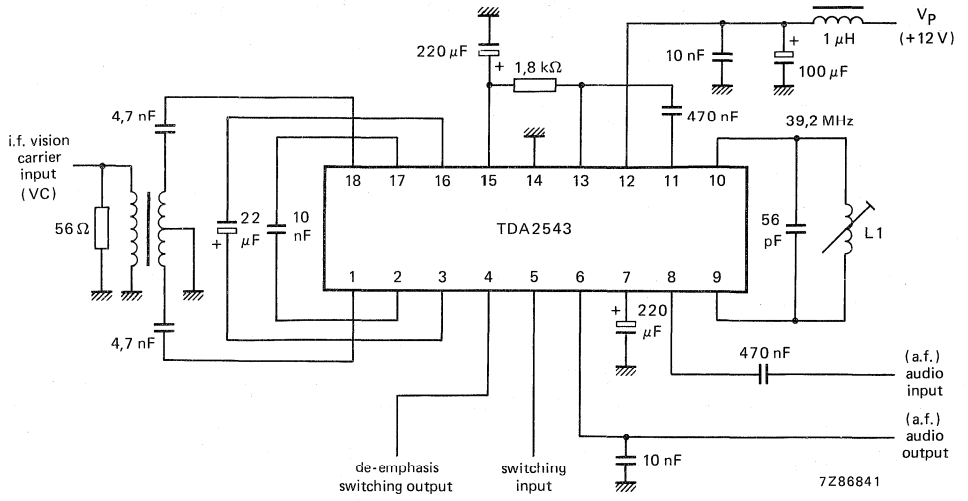


Fig. 2 Measuring circuit; L1 adjusted to minimum distortion at the a.f. output.

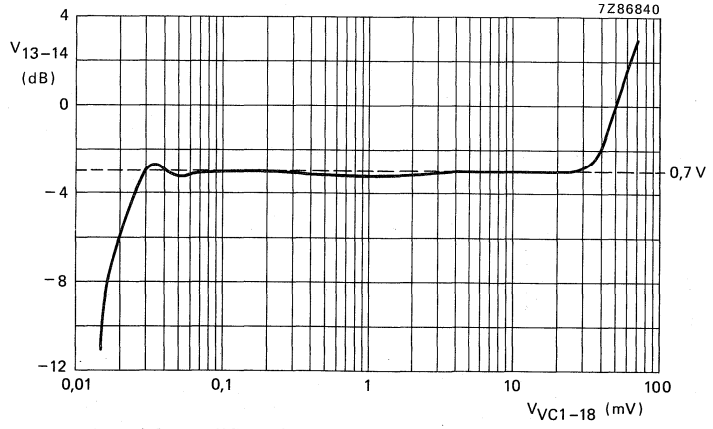


Fig. 3 Control curve of the i.f. amplifier; the r.m.s. a.f. output voltage at pin 13 ($V_{13\text{-}14(rms)}$) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

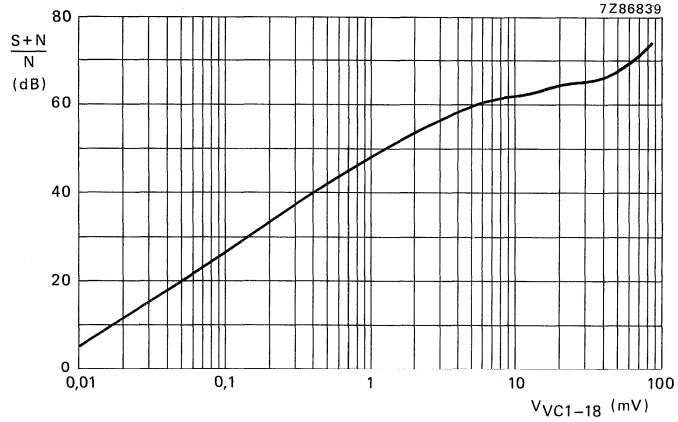


Fig. 4 Signal-to-weighted-noise ratio (S + N/N) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$).

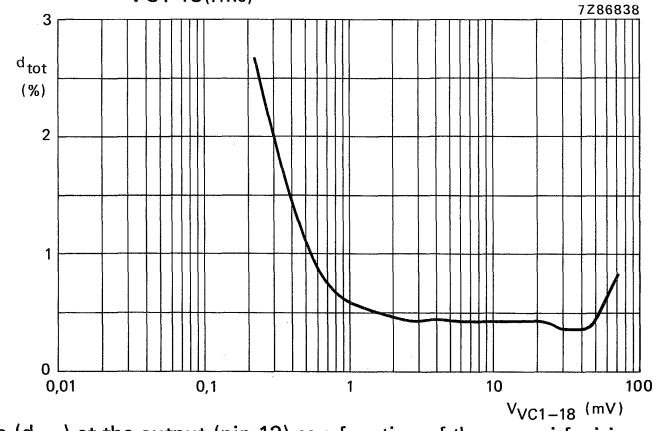


Fig. 5 Distortion (d_{tot}) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at f_m = 1 kHz and m = 0,8.

QUASI-SPLIT-SOUND CIRCUIT

GENERAL DESCRIPTION

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

Features

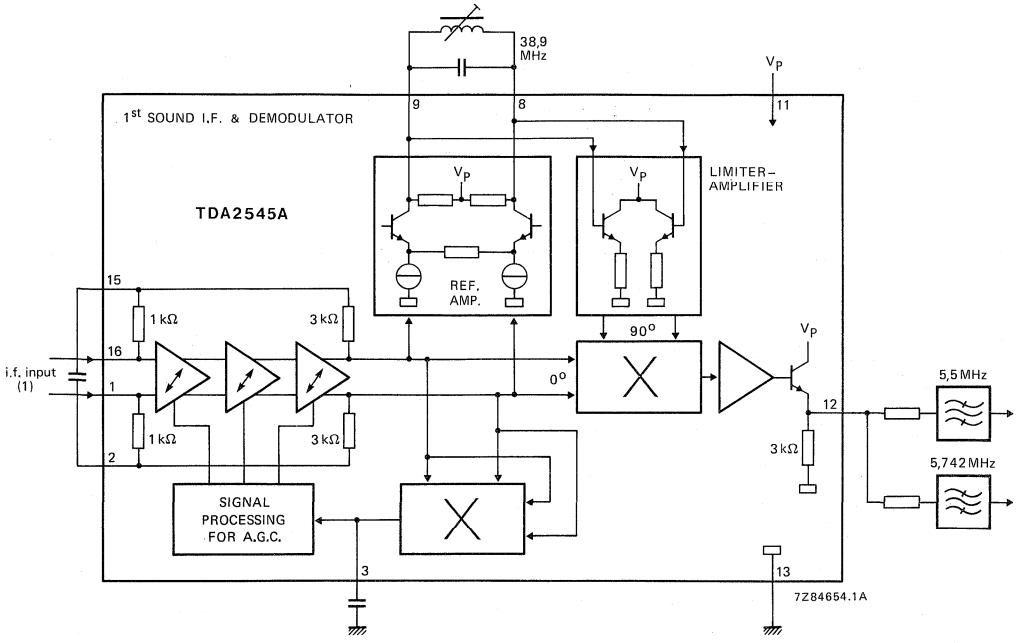
- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

QUICK REFERENCE DATA

Supply voltage (pin 11)	$V_P = V_{11-13}$	typ.	12 V
Supply current (pin 11)	$I_P = I_{11}$	typ.	45 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1-16(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12-13(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12-13(rms)}$	typ.	45 mV
I.F. control range	ΔG_V	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56 dB

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-13}$	max.	13,2	V
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{11-13} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 11)					
Supply voltage	$V_P = V_{11-13}$	10,8	12	13,2	V
Supply current	$I_P = I_{11}$	33	45	55	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-16(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-16(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-13}	4	–	V_p	V
Input resistance	R_{1-16}	–	2,5	–	kΩ
Input capacitance	C_{1-16}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{12-13(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{12-13(rms)}$	27	45	63	mV
D.C. output voltage	V_{12-13}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{12-13}	7	–	–	kΩ
Allowable output current	$-I_{12}$	–	–	1	mA
Intercarrier signal-to-noise (see note 1) (measured behind the FM demodulators) weighted according to CCIR 468-2, quasi-peak					
a. 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
b. 6 kHz sinewave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
c. black level (sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

Note 1.
Incidental phase on the vision carrier, caused by TV transmitter, has to be less than 0,5 degrees for black to white transient (equivalent to S+W/W = 56 dB for 6 kHz sinewave).

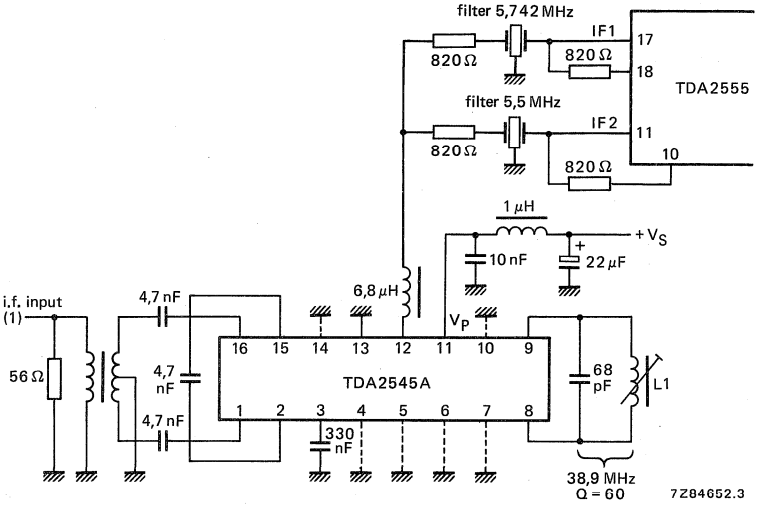


Fig. 2 Measuring circuit for TDA2545A.

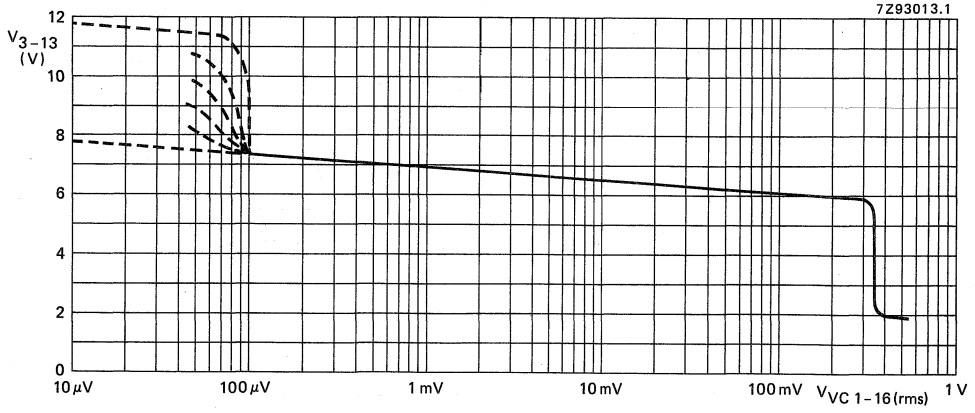


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-16\,(rms)}$.

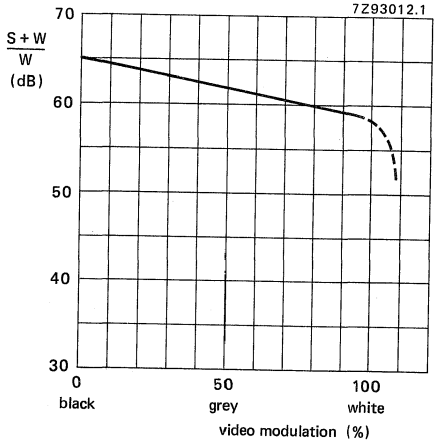


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5,5 MHz signal)

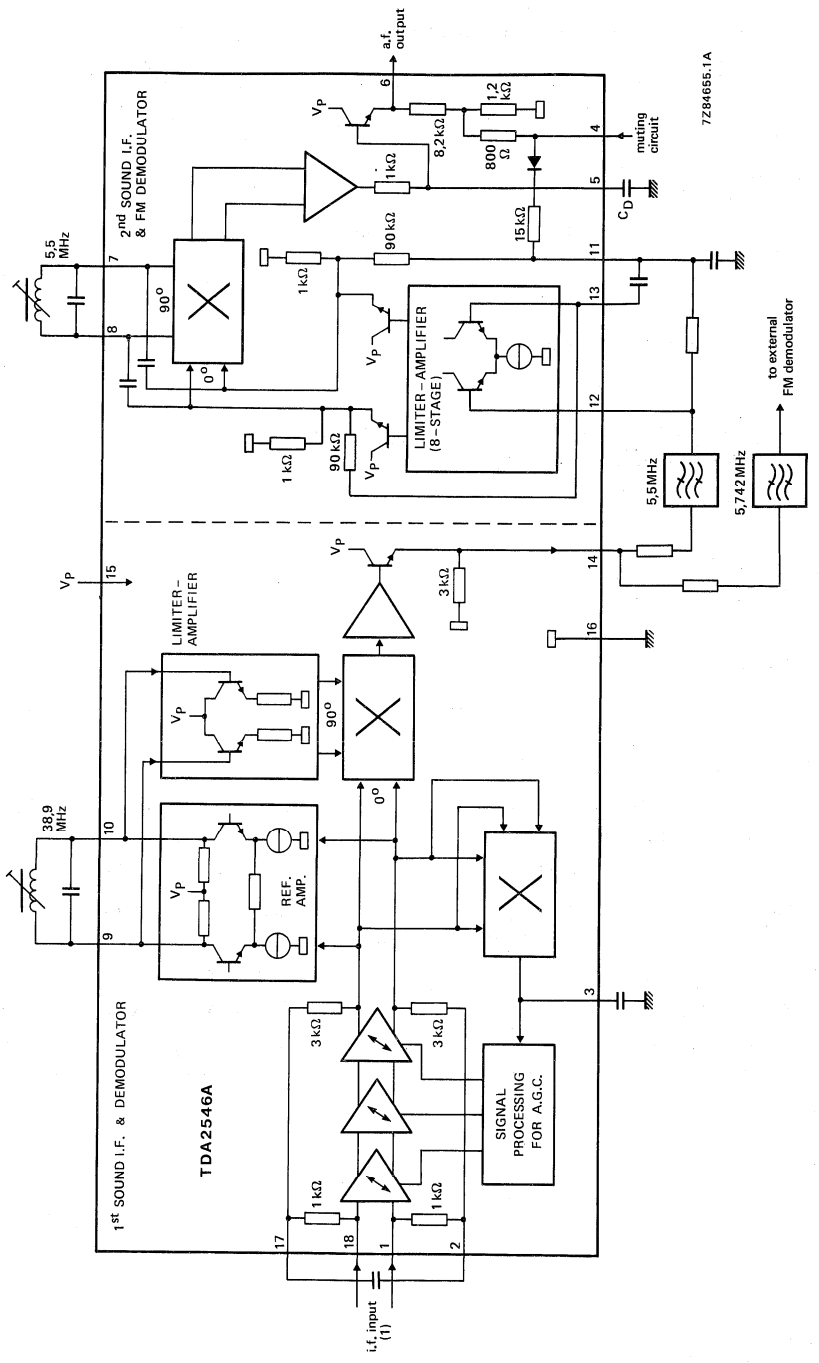
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15-16}$	typ.	12 V
Supply current (pin 15)	$I_P = I_{15}$	typ.	57 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1-18(rms)}$	typ.	150 μV
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14-16(rms)}$	typ.	100 mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14-16(rms)}$	typ.	45 mV
I.F. control range	ΔG_v	typ.	64 dB
Signal-to-weighted-noise ratio (rel. to 1 kHz; 30 kHz deviation)			
at 5,5 MHz for 2T/20T pulses with white bars	S + W/W	typ.	58 dB
at 5,742 MHz	S + W/W	typ.	56 dB
A.F. output voltage (r.m.s. value)	$V_{o6-16(rms)}$	typ.	0,6 V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT102).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-16}$	max.	13,2	V
Input current (pin 4)	I_4	max.	7	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15-16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz:

Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).

Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
Vision-to-sound carrier ratios are VC/SC1 = 13 dB and VC/SC2 = 20 dB.

Sound carriers (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-16}$	10,8	12	13,2	V
Supply current	$I_P = I_{15}$	40	57	75	mA
I.F. amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC1-18(rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC1-18(rms)}$	100	250	–	mV
I.F. gain control range	ΔG_v	60	64	–	dB
Control voltage range (see Fig. 3)	V_{3-16}	4	–	V_p	V
Input resistance	R_{1-18}	–	2,5	–	kΩ
Input capacitance	C_{1-18}	–	1,5	–	pF
Intercarrier generation					
Output voltage; 5,5 MHz (r.m.s. value)	$V_{14-16(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (r.m.s. value)	$V_{14-16(rms)}$	27	45	63	mV
D.C. output voltage	V_{14-16}	–	5,9	–	V
Allowable d.c. load resistance at the output	R_{14-16}	7	–	–	V
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5,5 MHz)					
Input voltage vor start of limiting (r.m.s. value)	$V_{12-16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12-16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13-16}$	–	2,2	–	V

parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	450	600	810	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable d.c. load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Allowable a.c. load impedance at the output	$Z_{6\text{-}16}$	10	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2,5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak 2T/20T pulses with white bars (see also Fig. 4)					
at 5,5 MHz	S+W/W	53	58	–	dB
at 5,742 MHz	S+W/W	51	56	–	dB
6 kHz sine wave					
at 5,5 MHz	S+W/W	50	53	–	dB
at 5,742 MHz	S+W/W	50	53	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5,5 MHz	S+W/W	60	65	–	dB
at 5,742 MHz	S+W/W	58	63	–	dB

NOTES TO THE CHARACTERISTICS

1. Incidential phase on the vision carrier, caused by TV-transmitter, has to be less than 0,5 degrees for black to white transient.
   (Equivalent to S+W/W = 56 dB for 6 kHz sine wave).

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

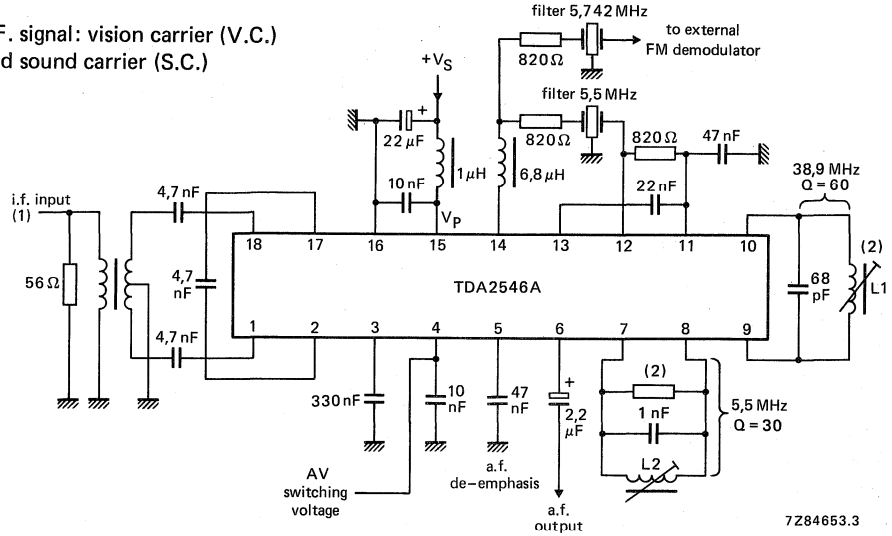


Fig. 2 Measuring circuit for TDA2546A.

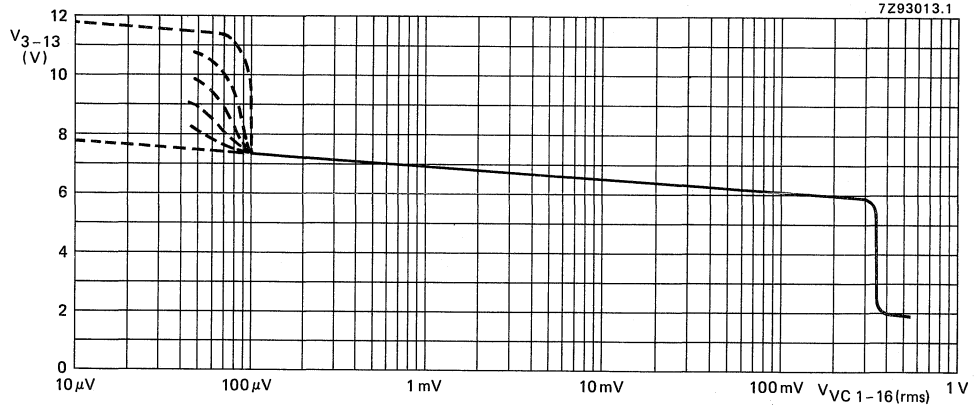


Fig. 3 Control voltage at pin 3 as a function of the input voltage $V_{VC1-18(rms)}$.

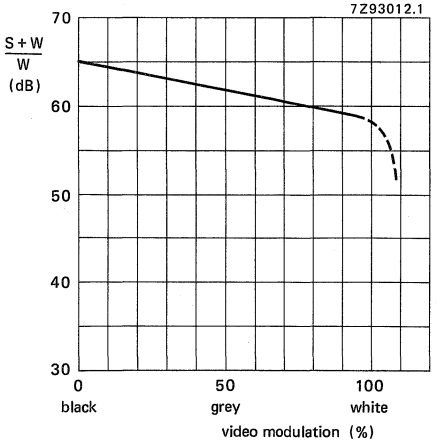


Fig. 4 Signal-to-weighted-noise ratio depending on video modulation.

I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

GENERAL DESCRIPTION

The TDA2549 is a complete i.f. circuit with a.f.c., a.g.c., demodulation and video preamplification facilities for multistandard television receivers. It is capable of handling positively and negatively modulated video signals in both colour and black/white receivers.

Features

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A.G.C. output for controlling MOSFET tuners

QUICK REFERENCE DATA

Supply voltage (pins 13 and 21)	$V_P = V_{13;21-3}$	typ.	12 V
Supply current (pins 13 and 21)	$I_P = I_{13;21-3}$	typ.	82 mA
I.F. input signal at V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	typ.	50 μV
Video output voltage at V_i = 0 V (between pins 22 and 3)			
positive modulation	$V_o = V_{22-3}$	typ.	2 V
negative modulation	$V_o = V_{22-3}$	typ.	4 V
Gain control range	G_v	typ.	74 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	57 dB
A.F.C. output voltage swing (pin 15)	V_{15-3}	min.	10 V
Max. tuner a.g.c. output current (pin 10)	I_{10}	min.	0,3 mA
Video bandwidth (3 dB)	B	typ.	5,5 MHz
Auxiliary video input voltage (pin 12) at V_o = 2 V (peak-to-peak value)	$V_{12-3(p-p)}$	typ.	1 V
Auxiliary video output impedance (pin 14)	$\lvert Z_{14-3} \rvert$	typ.	7 Ω
Auxiliary video output voltage (pin 14)	V_{14-3}	typ.	2 V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

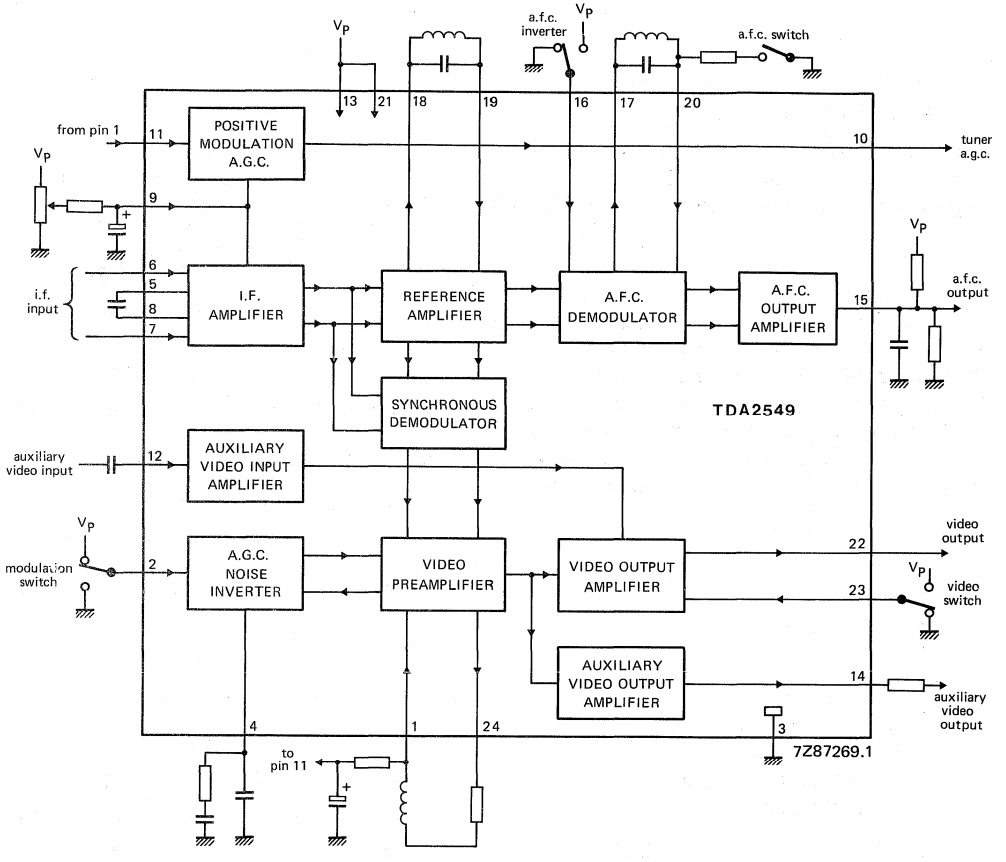


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 21)	V_P	13,8 V
Storage temperature range	T_{stg}	−25 to +125 °C
Operating ambient temperature range	T_{amb}	−25 to +70 °C

CHARACTERISTICS (measured in Fig. 5)

V_P = 12 V; T_{amb} = 25 °C

paramater	symbol	min.	typ.	max.	unit
Supply voltage range	V_P	10,8	12	13,2	V
Supply current (pins 13 and 21)	I_P	–	82	–	mA
I.F. input signal for V_o = 2 V (between pins 6 and 7)	$V_i = V_{6-7}$	–	50	150	μV
Input impedance (differential)	$\|Z_{6-7}\|$	–	2	–	kΩ
Input capacitance (differential)	C_{6-7}	–	2	–	pF
Zero signal output level positive modulation	V_{22-3}	1,6	2	2,3	V
negative modulation	V_{22-3}	3,7	4	4,3	V
Top sync output level	V_{22-3}	1,7	2	2,3	V
Gain control range	G_v	50	74	–	dB
Signal-to-noise ratio at V_i = 10 mV (note 1)	S/N	50	57	–	dB
Maximum video output amplitude for positive modulation (peak-to-peak value)	$V_{22-3(p-p)}$	4,5	–	–	V
Bandwidth of video amplifier (3 dB)	B	–	5,5	–	MHz
Differential gain at V_o = 2 V	dG	–	4	10	%
Differential phase at V_o = 2 V	$d\varphi$	–	2	10	%
Residual carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	10	20	mV
Residual second harmonic of carrier signal (r.m.s. value)	$V_{24-3(rms)}$	–	20	60	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F.C. output voltage swing	V_{15-3}	10	–	–	V
Change of frequency required for a.f.c. output voltage swing of 10 V	Δf	–	70	200	kHz
A.F.C. switch off for a voltage lower than:	V_{17-3}	–	–	1,5	V
A.F.C. inverter switch					
positive a.f.c. (Fig. 2)	V_{16-3}	0	–	1,5	V
negative a.f.c. (Fig. 3)	V_{16-3}	4	–	12	V
Tuner A.G.C.					
Leakage current	I_{10}	–	–	15	μA
Saturation voltage					
I_{10} = 0,3 mA	V_{10-3}	–	0,1	0,3	V
take-over point LOW	V_i	–	–	3	mV
take-over point HIGH	V_i	10	–	–	mV
Signal expansion at G_v = 50 dB	ΔV_{22-3}	–	–	0,5	dB
Negative modulation (Fig. 4)					
white spot inverter threshold level	V_{22-3}	–	4,6	–	V
white spot insertion level	V_{22-3}	–	3,2	–	V
noise inverter threshold level	V_{22-3}	–	0,9	–	V
noise insertion level	V_{22-3}	–	2,5	–	V
Positive modulation a.g.c. detector reference level	V_{11-3}	3,0	3,2	3,4	V
Auxiliary video input signal for $V_{o(p-p)}$ = 2 V	V_{12-3}	0,7	1	1,4	V
Auxiliary video output					
output signal (note 2)	V_{14-3}	–	1	–	V
top sync level	V_{14-3}	1	2	3	V
output impedance	$\lvert Z_{14-3} \rvert$	–	7	–	Ω
Levels for video switches					
positive video	V_{2-3}	–	–	1	V
negative video	V_{2-3}	3	–	–	V
internally demodulated signal	V_{23-3}	–	–	1	V
auxiliary video signal	V_{23-3}	3	–	–	V

Notes to the characteristics

1. Signal-to-noise ratio $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
2. Measured in application of Fig. 5.

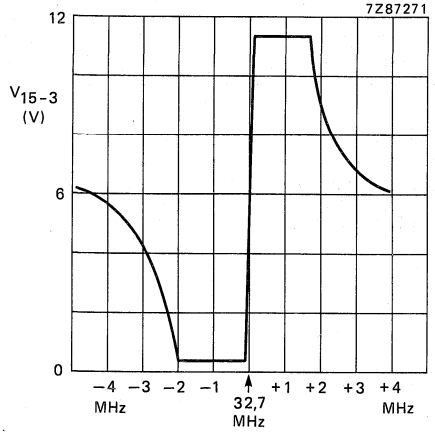


Fig. 2 A.F.C. output voltage V_{15-3} for positive a.f.c.

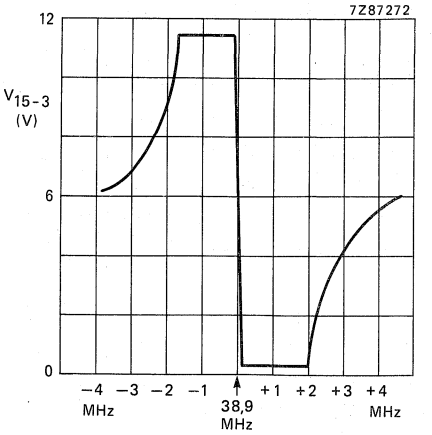


Fig. 3 A.F.C. output voltage V_{15-3} for negative a.f.c.

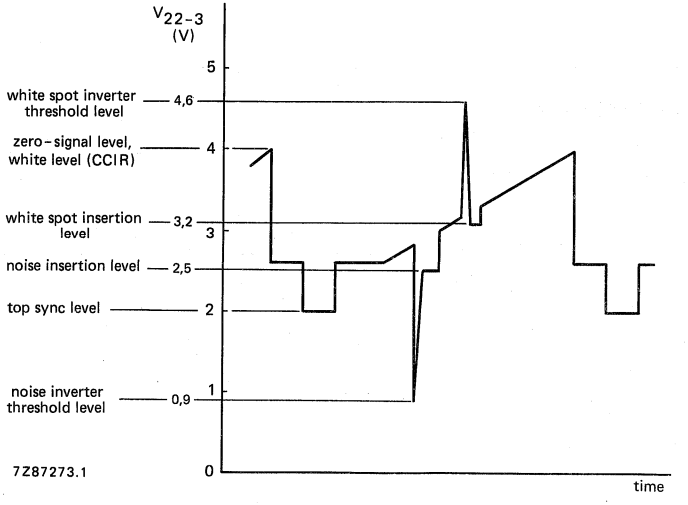


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

APPLICATION INFORMATION

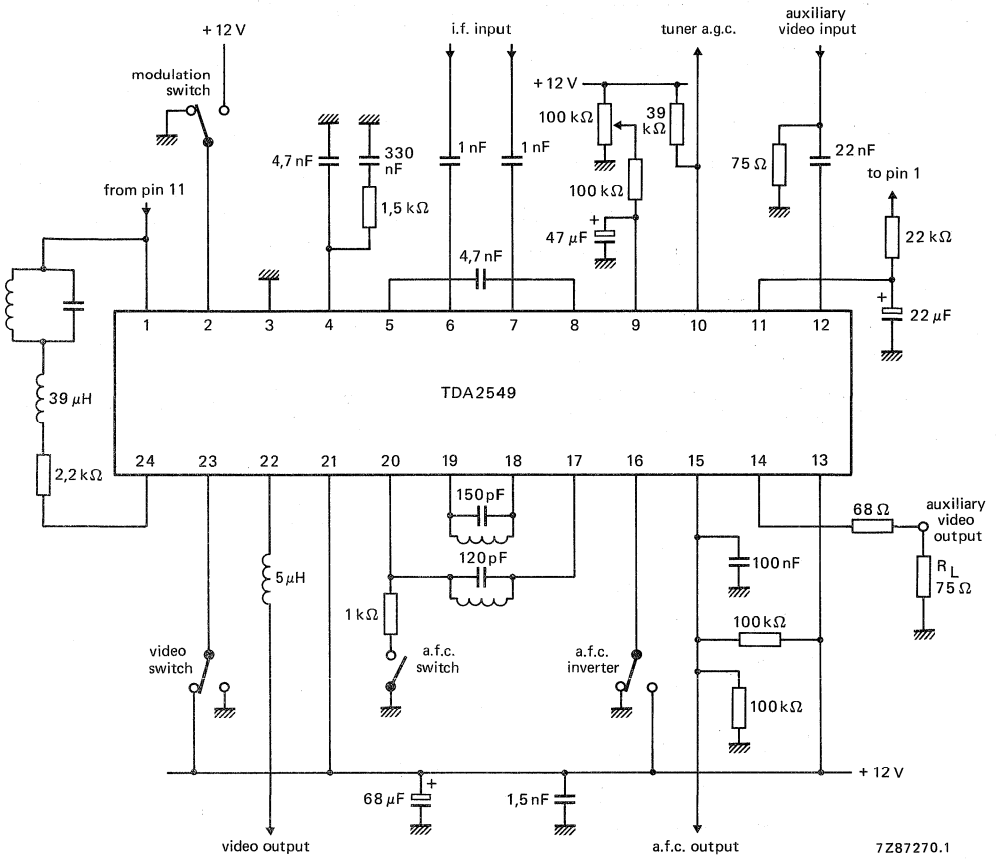


Fig. 5 Application diagram.

DUAL TV SOUND DEMODULATOR CIRCUITS

GENERAL DESCRIPTION

The circuits incorporate two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.
The difference between TDA2555 and TDA2557 is the number of stages of the limiting amplifier.

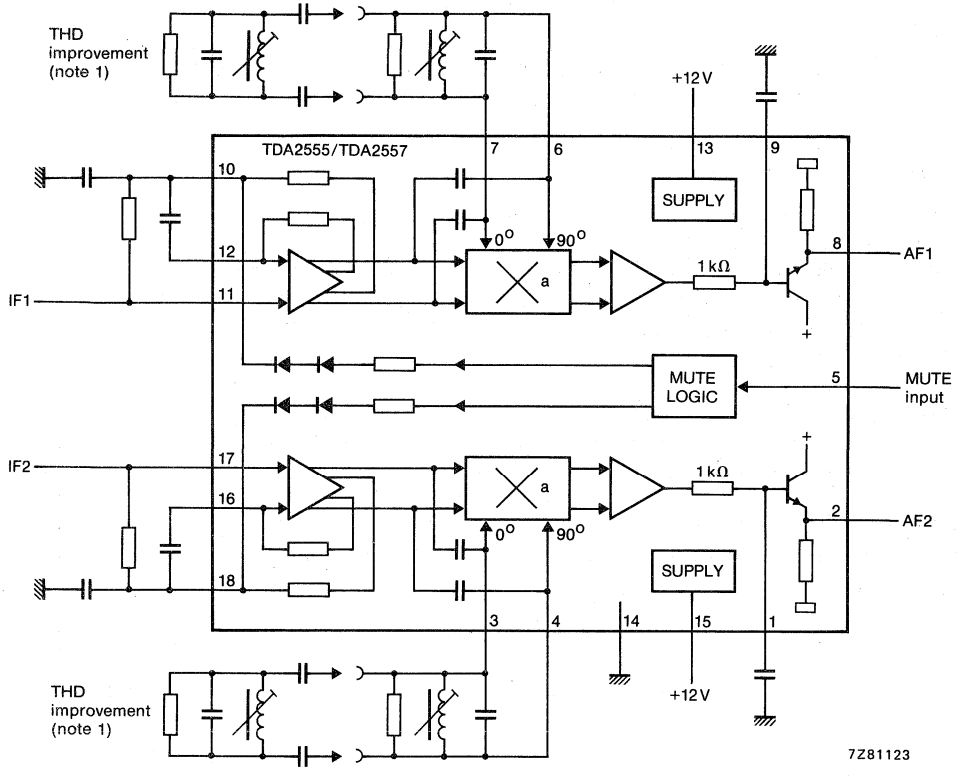
- **Eight** (TDA2555) or **five** (TDA2557) stage limiting amplifier
- Quadrature demodulator for FM detection
- De-emphasis stage
- Output amplifier
- Mute function for each FM demodulator

QUICK REFERENCE DATA

Supply voltage (pins 13 and 15)	V_P	typ.	12	V
Supply current (pins 13 and 15)	I_P	typ.	24,5	mA
AF output voltage (pins 2 and 8)	$V_{o(rms)}$	typ.	600	mV
Total harmonic distortion (note 1)	THD	<	0,1	%
Signal to weighted noise ratio	(S + N)/N	typ.	70	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



a = QUADRATURE DEMODULATOR

Fig. 1 Block diagram.
TDA2555 with 8-stage limiting amplifier;
TDA2557 with 5-stage limiting amplifier.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 15)	V_P	max.	13,2 V
Total power dissipation	P_{tot}	max.	400 mW
Storage temperature range	T_{stg}	−40 to + 150	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

CHARACTERISTICS

$V_P = V_{13, 15-14} = 12$ V; $T_{amb} = 25$ °C; $f_{IF1} = 5{,}5$ MHz; $f_{IF2} = 5{,}74$ MHz; $f_{m1} = 1$ kHz;
$\Delta f = \pm 30$ kHz;
$V_{i(rms)} = 5$ mV for TDA2555;
$V_{i(rms)} = 10$ mV for TDA2557;
see test circuit Fig. 3, voltages with respect to ground (pin 14), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Total current consumption	$I_{13,15}$	18	24,5	30	mA
LIMITING AMPLIFIER					
Maximum input voltage	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	200	–	mV
Input voltage for start of limiting (3 dB AF signal reduction)					
TDA2555	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	50	100	μV
TDA2557	$V_{11\text{-}12(rms)}$ $V_{16\text{-}17(rms)}$	–	250	500	μV
DC voltage (input limiting amplifier) pins 11, 12, 16, 17 to 14	V_i	–	2,0	–	V
DC voltage (feedback loop)	$V_{10,18\text{-}14}$	–	2,0	–	V
FM DEMODULATOR					
IF reference signal voltage	$V_{3\text{-}4(rms)}$ $V_{6\text{-}7(rms)}$	–	200	–	mV
DC voltage	$V_{3,4,6,7\text{-}14}$	–	3,1	–	V
AF output voltage	$V_{2\text{-}14(rms)}$	450	600	750	mV
Difference of output signals	$\frac{V_{2\text{-}14}}{V_{8\text{-}14}}$	–	± 0,1	± 0,5	dB
Total harmonic distortion at outputs AF1 and AF2 (note 1)	THD	–	–	0,5	%
A.M. suppression at outputs AF1 and AF2, $f_{FM} = 70$ Hz; $\Delta f = \pm 50$ kHz; $f_{AM} = 1$ kHz; m = 0,3	AMS	50	–	–	dB

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
FM DEMODULATOR (continued)					
Signal to noise ratio at outputs AF1 and AF2 (CCIR weighted, quasi peak)	$(S+N)/N$	65	70	–	dB
Residual IF-signal without deemphasis	$V_{2,8\text{-}14(rms)}$	–	30	–	mV
Ripple rejection at outputs AF1 and AF2 f = 50 Hz to 20 kHz; $V_{i(rms)}$ = 200 mV	RR	–	40	–	dB
AUDIO OUTPUT STAGE					
emitter follower with 1,0 mA bias current					
DC output voltage	$V_{2,8\text{-}14}$	3,0	4,0	5,0	V
External DC load resistance	$R_{2,8\text{-}14}$	2	–	–	kΩ
AC output current (note 2)	$-I_{2,8\text{-}14(p\text{-}p)}$	–	–	0,5	mA
Deemphasis input resistance (note 3)	$R_{1,9\text{-}14}$	0,8	1,0	1,2	kΩ
DC voltage (deemphasis)	$V_{1,9\text{-}14}$	3,7	4,7	5,7	V
Crosstalk attenuation f = 1 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Crosstalk attenuation f = 10 kHz (note 4)	$\alpha_{12,21}$	60	–	–	dB
Output impedance	$R_{2,8\text{-}14}$	–	25	–	Ω
AF output level (Fig. 2, note 5) MUTE function $V_{i(rms)} < 60$ mV	α	60	–	–	dB
Switching input current					
$V_{5\text{-}14} = 0$ V	$-I_5$	–	–	500	μA
$V_{5\text{-}14} = V_P$	I_5	–	–	500	μA
Internal d.c. voltage no mute (pin 5 not connected)	$V_{5\text{-}14}$	–	6,2	–	V

Notes to the characteristics

1. THD < 0,1% requires a double tuned demodulator circuit (Q_L = 20). With a single tuned circuit a THD of < 0,5% is possible (see Figs 1 and 3).
2. If higher a.c. output current is required an external resistor must be applied from output (pins 2 and 8) to ground (min. 2 kΩ) in order to improve the THD performance ($-I_{2,8} < 4$ mA).
3. The deemphasis time constant is 50 μs.
4. Crosstalk attenuation is defined as:

$$o_{12} = \frac{V_{2\text{-}14} \text{ unmodulated}}{V_{8\text{-}14}} \qquad o_{21} = \frac{V_{8\text{-}14} \text{ unmodulated}}{V_{2\text{-}14}}.$$

5. In the MUTE state the a.f. output level attenuation is more than 60 dB. The MUTE function is only guaranteed for an r.m.s. value of the input voltage lower than 60 mV. See also Fig. 2.

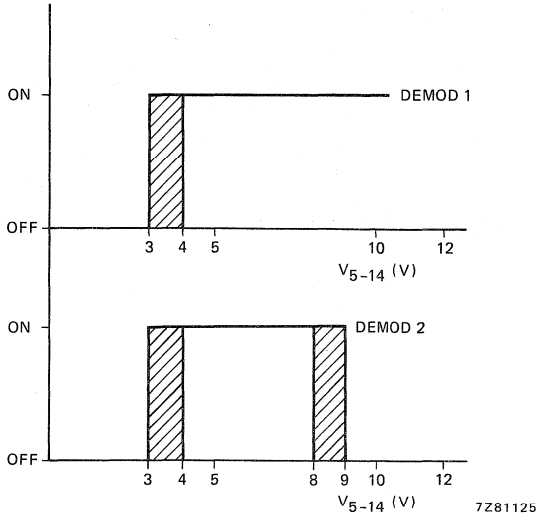


Fig. 2 Mute function.

DEVELOPMENT DATA

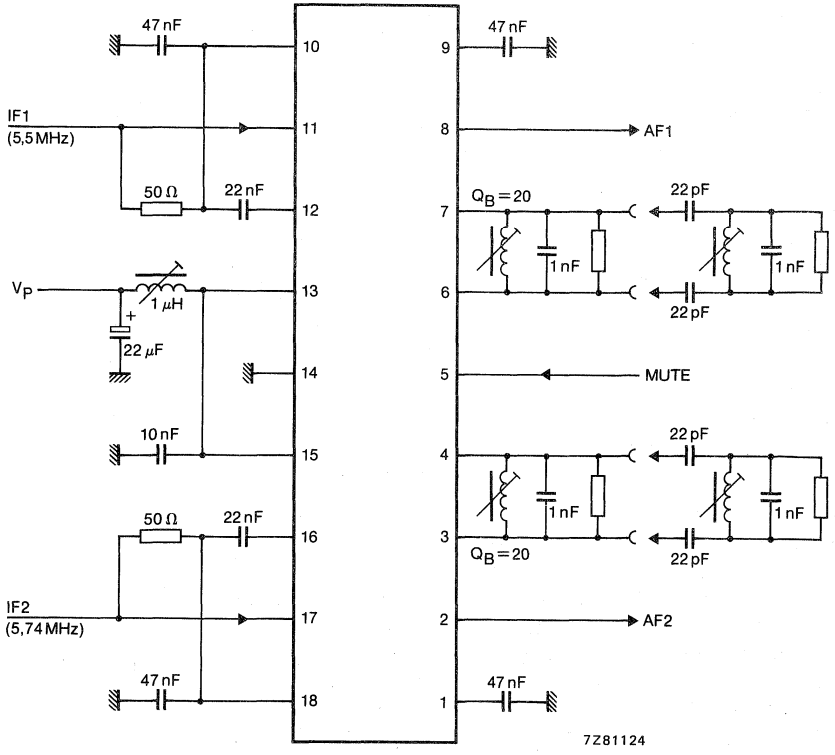


Fig. 3 Test and application circuit.

QUASI-SPLIT-SOUND CIRCUIT WITH DUAL SOUND DEMODULATORS

GENERAL DESCRIPTION

The TDA2556 is a monolithic integrated circuit for quasi-split-sound processing, including two FM demodulators, for two carrier stereo TV receivers and VTR.

Features

First IF (vision carrier plus sound carrier).

- 3 stage gain controlled IF amplifier
- AGC circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

Second IF (two separate channels for both FM sound signals).

- 4-stage-limiting amplifier
- Quadrature demodulator
- AF amplifier with de-emphasis
- Output buffer
- Muting for one or both AF outputs

QUICK REFERENCE DATA

Supply voltage, pin 23	$V_P = V_{23-24}$	typ.	12	V
Supply current, pin 23	$I_P = I_{23}$	typ.	73	mA
Minimum IF vision carrier input voltage (rms value)	$V_{VC} = V_{3-4}$	typ.	150	μV
IF control range	ΔG_V	typ.	64	dB
AF output voltage	$V_{O\ 10,\ 15-24(rms)}$	typ.	600	mV
Signal-to-weighted-noise ratio (relative to 1 kHz; 30 kHz deviation)				
at 5,5 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	58	dB
at 5,74 MHz } for 2T/20T pulses with white bars	S + W/W	typ.	56	dB

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101B).

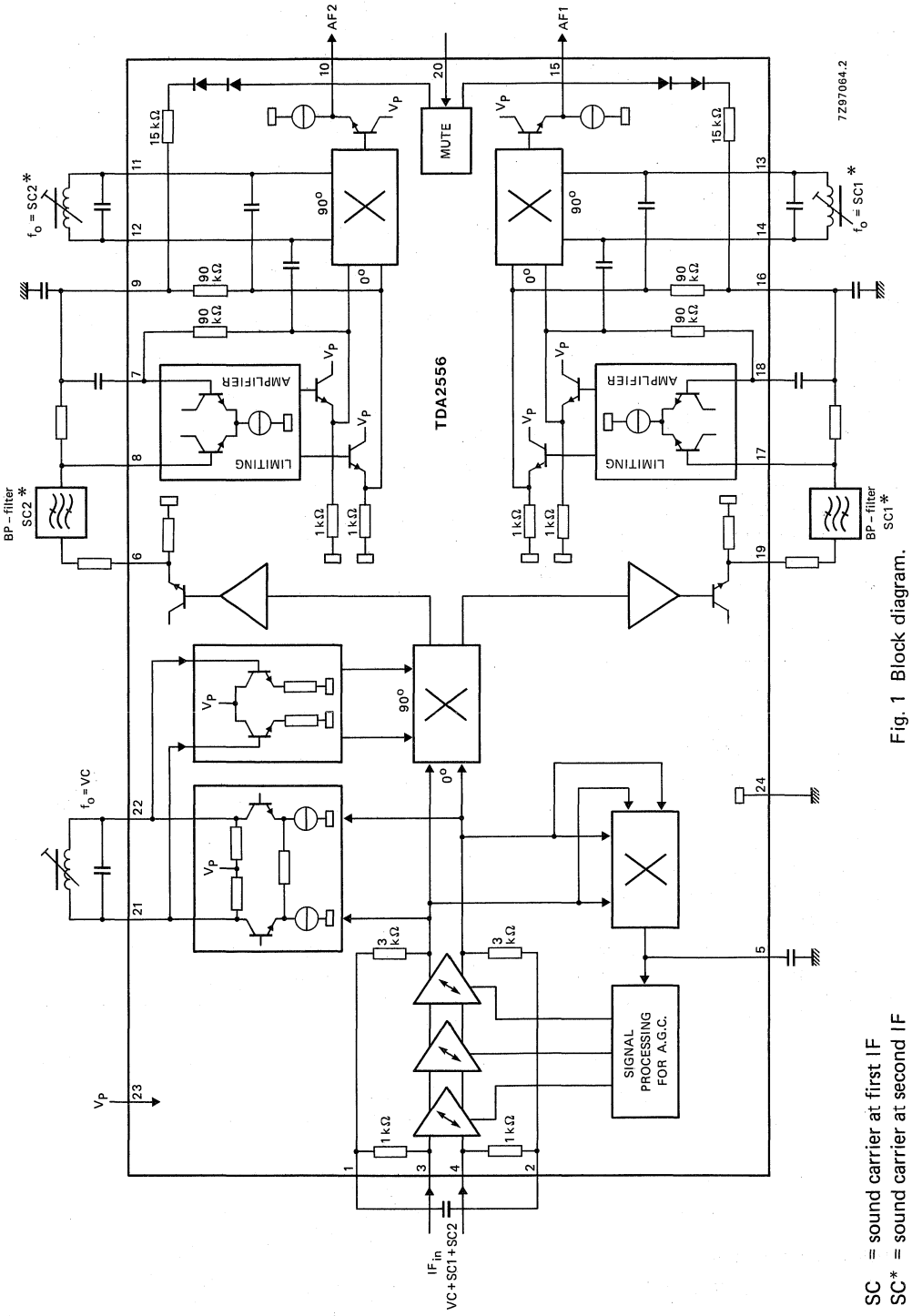


Fig. 1 Block diagram.

SC = sound carrier at first IF
SC* = sound carrier at second IF

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, pin 23	$V_P = V_{23-24}$	max.	13,2	V
Supply current, pin 23	$I_P = I_{23}$	max.	95	mA
Storage temperature range	T_{stg}	−25 to	+ 150	°C
Operating ambient temperature range	T_{amb}	0 to	+ 70	°C

CHARACTERISTICS

$V_P = V_{23-24} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz, $f_{SC1} = 33{,}4$ MHz, $f_{SC2} = 33{,}158$ MHz.
Vision carrier (V.C.) modulated with different video signals (see below); modulation depth 100% (proportional to 10% residual carrier).
Vision carrier amplitude: $V_{VC(rms)} = 10$ mV.
Vision-to-sound carrier ratios: VC/SC1 = 13 dB, VC/SC2 = 20 dB.
Sound carrier (SC1, SC2) modulated with f = 1 kHz and deviation $\Delta f = \pm 30$ kHz.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 23)					
Supply voltage	$V_P = V_{23-24}$	10,8	12	13,2	V
Supply current	$I_P = I_{23}$	–	73	95	mA
First IF amplifier					
Input voltage for start of gain control (intercarrier signals −3 dB)	$V_{VC} = V_{3-4\ (rms)}$	–	150	200	μV
Input voltage for end of gain control (intercarrier signals + 1 dB)	$V_{VC} = V_{3-4\ (rms)}$	100	250	–	mV
Gain control range	ΔG_V	60	64	–	dB
Control voltage range (see Fig. 6)	V_{5-24}	4	–	V_P	V
Input resistance (differential)	R_{3-4}	–	2	–	kΩ
Input capacitance (differential)	C_{3-4}	–	2	–	pF
Intercarrier signal					
Output voltage; 5,5 MHz (SC1*)	$V_{19-24(rms)}$	60	100	140	mV
Output voltage; 5,742 MHz (SC2*)	$V_{6-24(rms)}$	27	45	63	mV
Output voltage d.c. (emitter follower with minimum 1,5 mA bias current)	$V_{6-24/19-24}$	–	5,9	–	V
Allowable d.c. load resistance	$R_{6-24/19-24}$	7	–	–	kΩ
Second IF					
Input voltage for start of limiting	$V_{8-24/17-24(rms)}$	–	700	–	μV
Maximum input voltage	$V_{8-24/17-24(rms)}$	–	200	–	mV
Voltage level d.c.	$V_{7-24/18-24}$	–	2,2	–	V
Voltage level d.c.	$V_{9-24/16-24}$	–	2,2	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Second IF (continued)					
AF output voltage	$V_{10-24/15-24}$	450	600	810	mV
Output voltage d.c. (emitter follower with 1,0 mA bias current)	$V_{10-24/15-24}$	–	4,5	–	V
External d.c. load resistance	$R_{10-24/15-24}$	2	–	–	kΩ
External a.c. load current (note 5)	$I_{10/15}$	–	–	0,5	mA
Total harmonic distortion of $V_{10-24/15-24}$ (note 3)	THD	–	0,4	1	%
(note 4)	THD	–	–	0,1	%
AM suppression; f_{AM} = 1 kHz, M = 0,3; f_{FM} = 70 Hz; f = ± 50 kHz (note 2)		50	60	–	dB
Crosstalk attenuation (note 2)		60	–	–	dB
S/N ratio (second IF) (note 2) f = 1 kHz; f = ± 50 kHz	$V_{10-24/15-24}$	65	70	–	dB
Mute (see Fig. 4)					
Switching voltage for:					
demodulator 1 ON	V_{20-24}	4	–	V_P	V
demodulator 1 OFF	V_{20-24}	0	–	3	V
demodulator 2 ON	V_{20-24}	4	–	8	V
demodulator 2 OFF	V_{20-24}	0 or 9	–	3 or V_P	V
Input current	I_{20}	–500	–	+ 200	μA
Input d.c. potential	V_{20-24}	–	6,3	–	V
AF signal performance, weighted S/N ratio at audio outputs, pins 10, 15; V_{3-4} = 20 mV rms weighted according to CCIR 468-2, quasi-peak, (see note 1)					
(a) 2T/20T pulse with white bars (see also Fig. 5)					
at 5,5 MHz	(S + W)/W	–	58	–	dB
at 5,74 MHz	(S + W)/W	–	56	–	dB
(b) 6 kHz sine wave					
at 5,5 MHz	(S + W)/W	–	52	–	dB
at 5,74 MHz	(S + W)/W	–	50	–	dB
(c) black level (sync pulses only)					
at 5,5 MHz	(S + W)/W	–	65	–	dB
at 5,74 MHz	(S + W)/W	–	63	–	dB

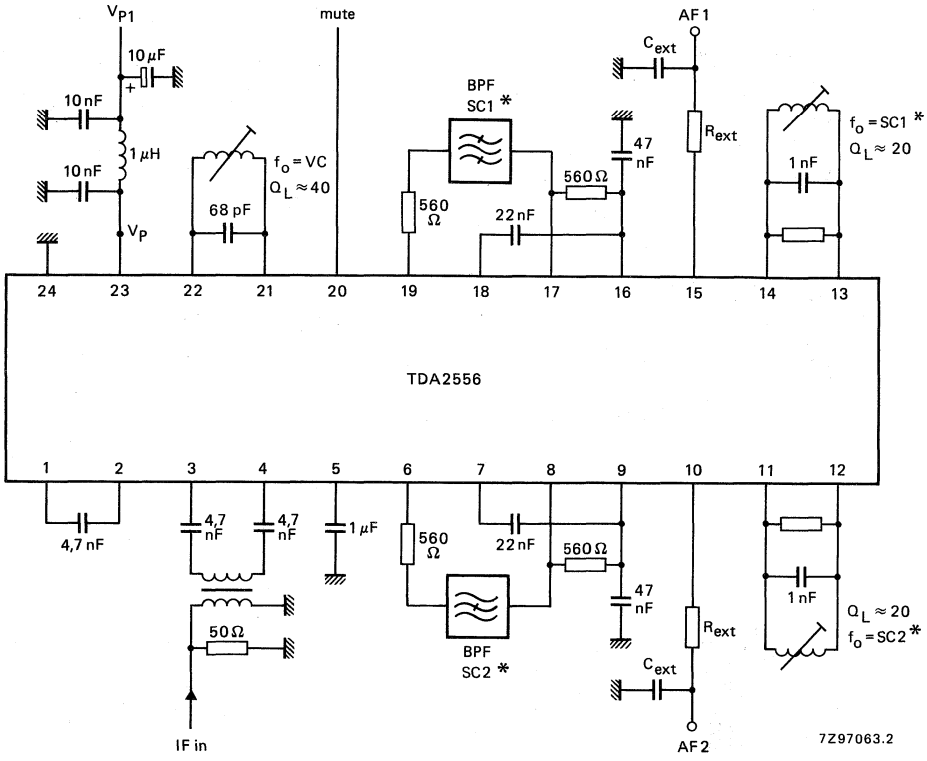


Fig. 2 Application diagram ($\tau_{deemph} = R_{ext} \cdot C_{ext}$)
(Input transformer "IF in" only for testing)

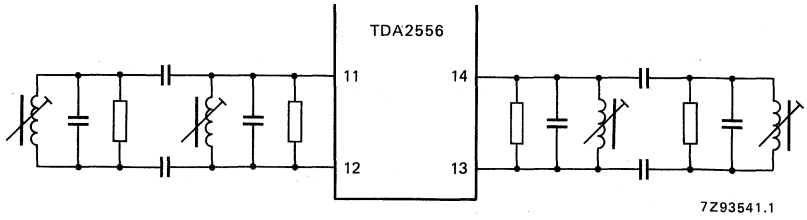


Fig. 3 Distortion improvement (see note 3 and 4).

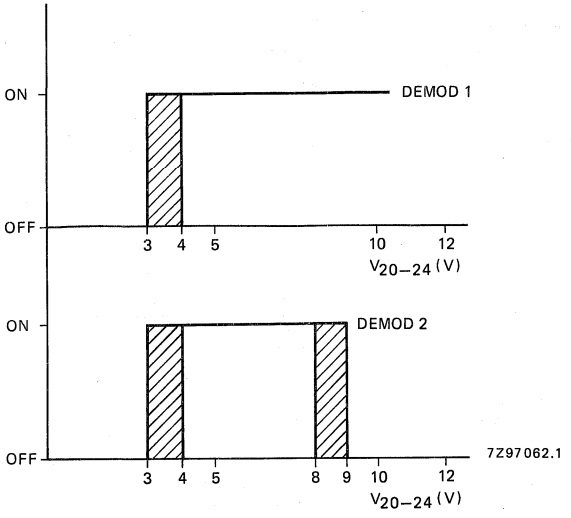


Fig. 4 Mute function.

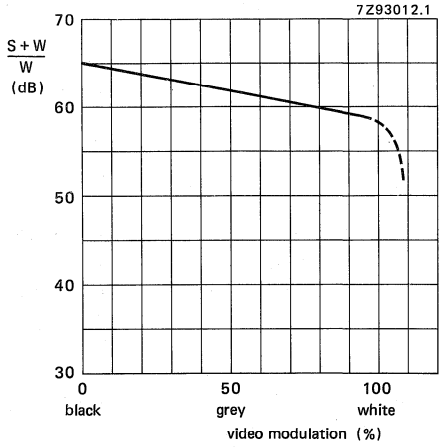


Fig. 5 Signal to weighted noise ratio depending on video modulation.

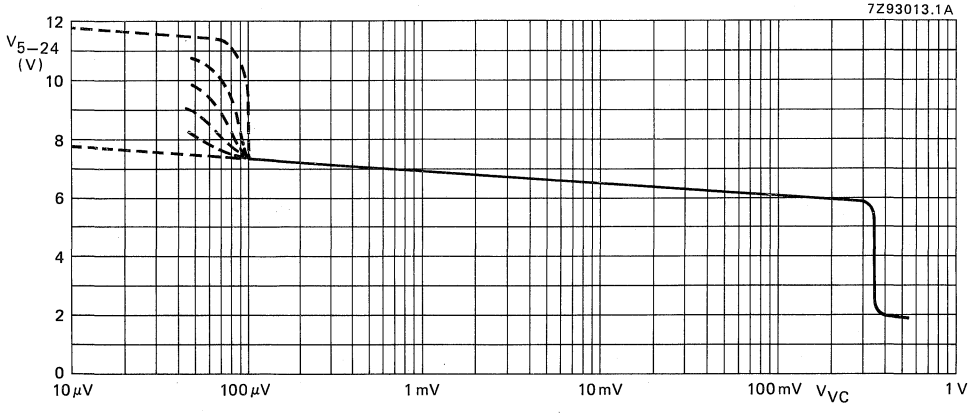


Fig. 6 Control voltage at pin 5 as a function of the input voltage $V_{VC} = V_{3\text{-}4(rms)}$.

Notes to the characteristics

1. Incidential phase on the vision carrier, caused by the TV transmitter, has to be less than 0,5 degrees for black and white transient; this is equivalent to S + W/W = 56 dB for a 6 kHz sine wave.
2. Input signal second IF $V_{8\text{-}24/17\text{-}24}$ = 10 mVrms.
3. THD value is valid for ceramic bandpass filters of SC* and single resonance circuits at pins 11 and 12 and pins 13 and 14.
4. THD value is valid for LC bandpass filters of SC* and double resonance circuits at pins 11 and 12 and pins 13 and 14.
5. If higher a.c. output current is required an external resistor has to be applied from output (pins 10 and 15) to ground (minimum 2 kΩ) in order to improve the THD performance.

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$	0,15 to 1	V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

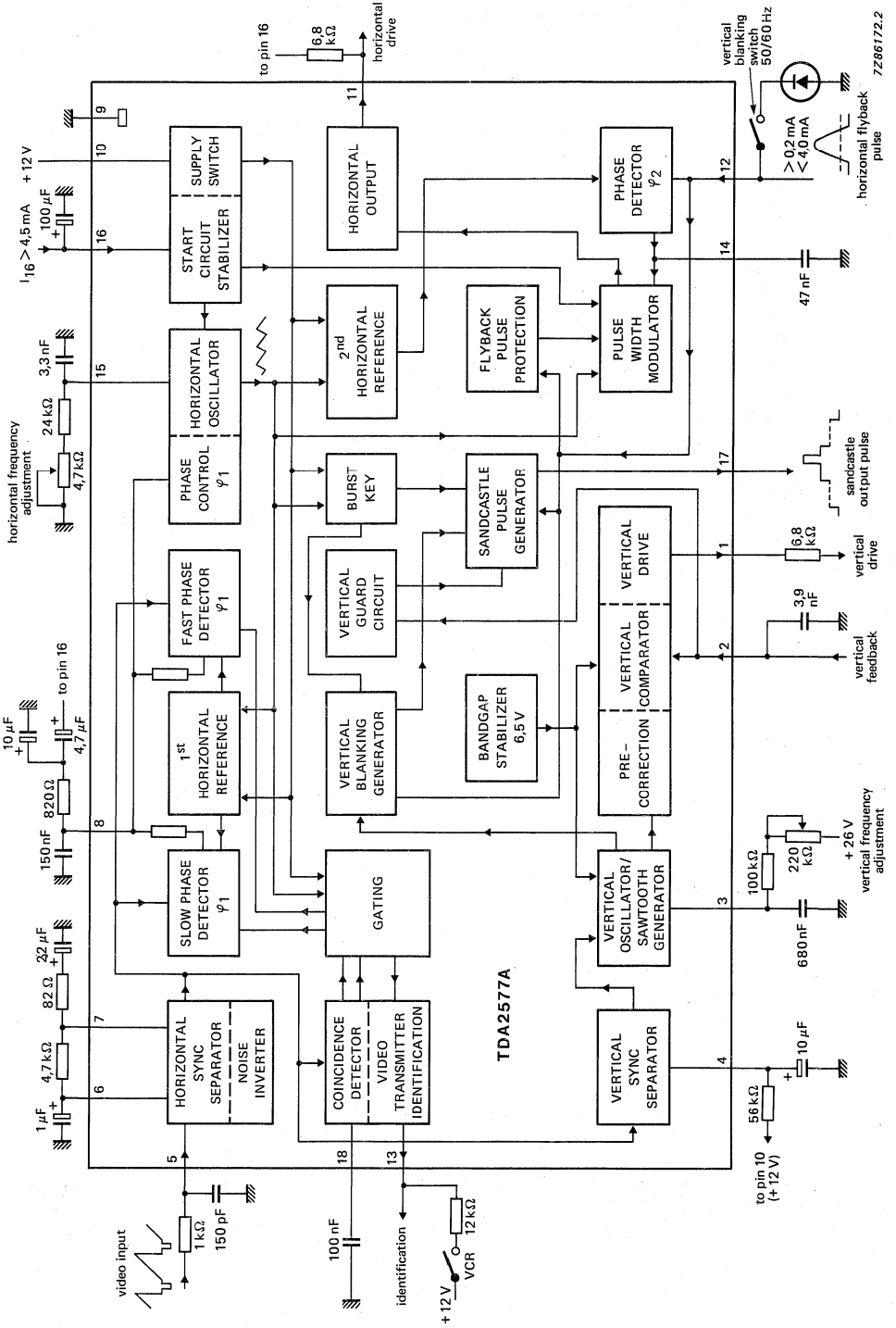


Fig. 1 Block diagram.

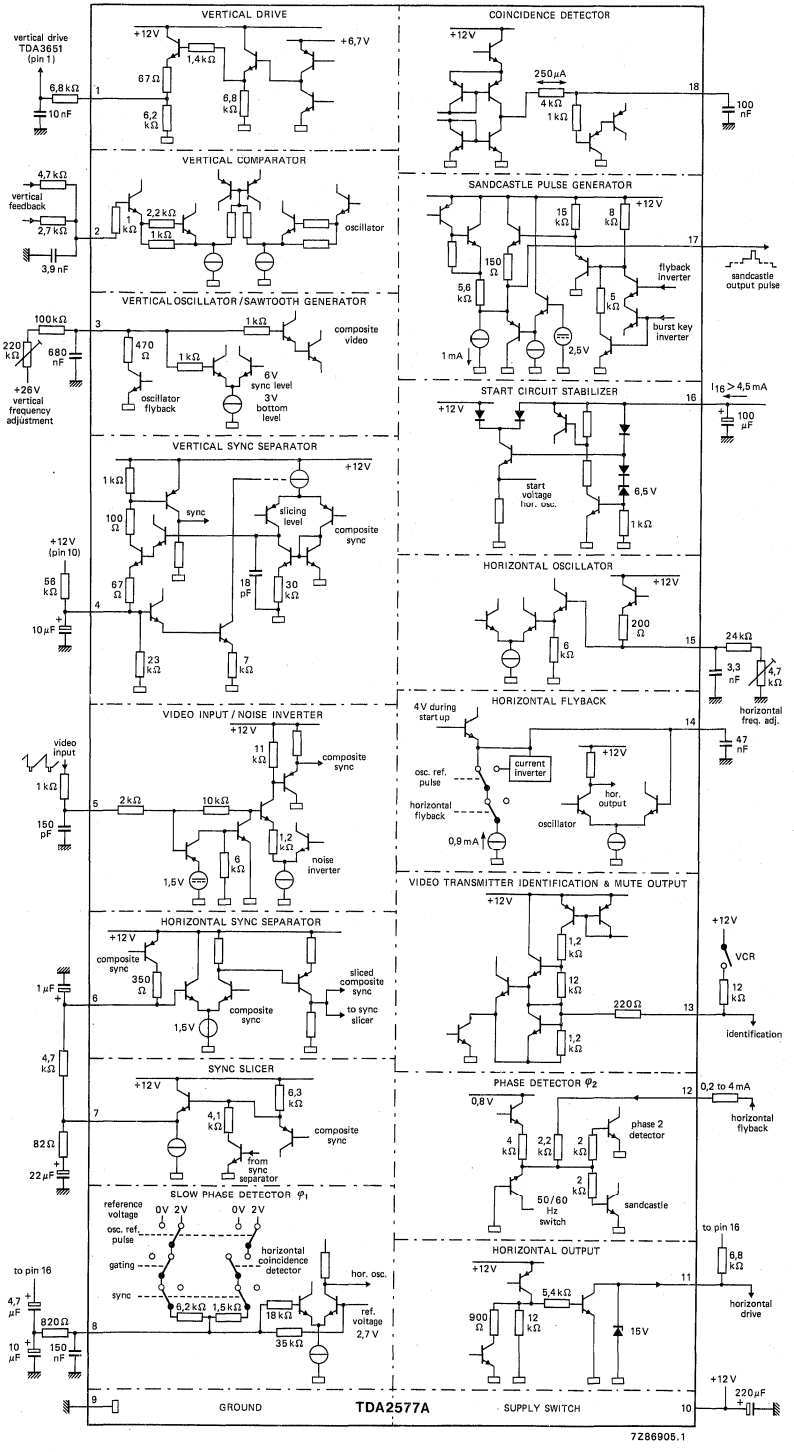


Fig. 2 TDA2577A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)			
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400 μs/μs
Control range	t_d		1 to 50 μs
Controlled edge	negative		
Phase adjustment (via 2nd control loop; pin 14)			
Control sensitivity		typ.	25 μA/μs
Maximum permissible control current	$\pm I_{14}$	<	60 μA
Horizontal oscillator (pin 15)			
Frequency (no sync)	f_{osc}	typ.	15 625 Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ)	Δf_{osc}	<	4 %
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 % 8 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Horizontal output (pin 11)			
Output voltage; high level	V_{11-9}	<	13,2 V
Voltage at which protection starts	V_{11-9}		13 to 15,8 V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 V 0,5 V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 V 0,5 V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65 %
Duty factor of output signal without flyback pulse	δ	typ.	50 % 47 to 57 %
Controlled edge	negative		
Duration of output pulse (see Fig. 3)			$t_d + t_o$ + 2,5 μs
Sandcastle output pulse (pin 17)			
Output voltage during: burst key	V_{17-9}	>	10 V
horizontal blanking	V_{17-9}	typ.	4,6 V 4,2 to 5 V
vertical blanking	V_{17-9}	typ.	2,5 V 2 to 3 V
Pulse duration burst key	t_p	typ.	3,7 μs 3,3 to 4,1 μs
horizontal blanking	flyback pulse (see note 3)		
vertical blanking for 50 Hz application ($-I_{12}$: 0 to 0,1 mA) for 60 Hz application ($-I_{12}$: typ. 0,2 mA)			21 lines 17 lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ. 4,8 to 5,6	5,2 µs µs
Delay between the start of the sync and the trailing edge of the burst key	t_2	typ. 8,1 to 9,3	8,8 µs µs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2			
Detector output current	$\pm I_{18}$	typ.	300 µA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ. 3,2 to 3,8	3,5 V V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ. 1,0 to 1,4	1,2 V V
vertical period counter 3 periods fast	V_{18-9}	typ. 0,08 to 0,16	0,12 V V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ. 1,5 to 1,9	1,7 V V
Switching level fast to slow (locking)	V_{18-9}	typ. 4,7 to 5,3	5,0 V V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ. 8,2 to 9,0	8,6 V V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	$>$ typ.	10 V 11 V
Output voltage active (no sync) at I_{13} = 5 mA	V_{13-9}	$>$ typ.	7 V 10 V
Output voltage inactive	V_{13-9}	$<$ typ.	0,5 V 0,1 V
VCR switching (pin 13)			
Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ. 0,4 to 0,8	0,6 mA mA
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}	0,2 to 4	mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	$<$	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 µs (see also note 2 and Fig. 4)	t_o	typ.	1,3 µs

Duration of vertical blanking pulse (pin 12)

Required input current (negative)			
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0,2 mA
			$>0,15$ to $<0,3$ mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	$<$	0,1 mA
Maximum allowed input current	$-I_{12}$	$<$	0,4 mA

Vertical sawtooth generator (pin 3)

Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	$<$	4 %
Synchronization range		typ.	22 %
Input current at V_{3-9} = 6 V	I_3	$<$	2 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	$<$	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}

Comparator (pin 2)

Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1,5 V
Input current at V_{2-9} = 6 V	I_2	$<$	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3 %

Vertical output stage; emitter follower (pin 1)

Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	$<$	20 mA

Vertical guard circuit

Activating voltage levels (vertical blanking level is 2,5 V)

switching level low	V_{2-9}	typ.	3 V
			2,7 to 3,3 V
switching level high	V_{2-9}	typ.	5,8 V
			5,4 to 6,3 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

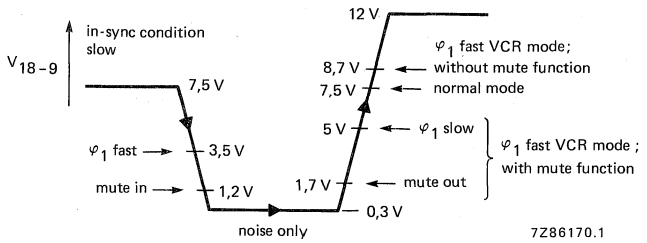


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked
							VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,8 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays

in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

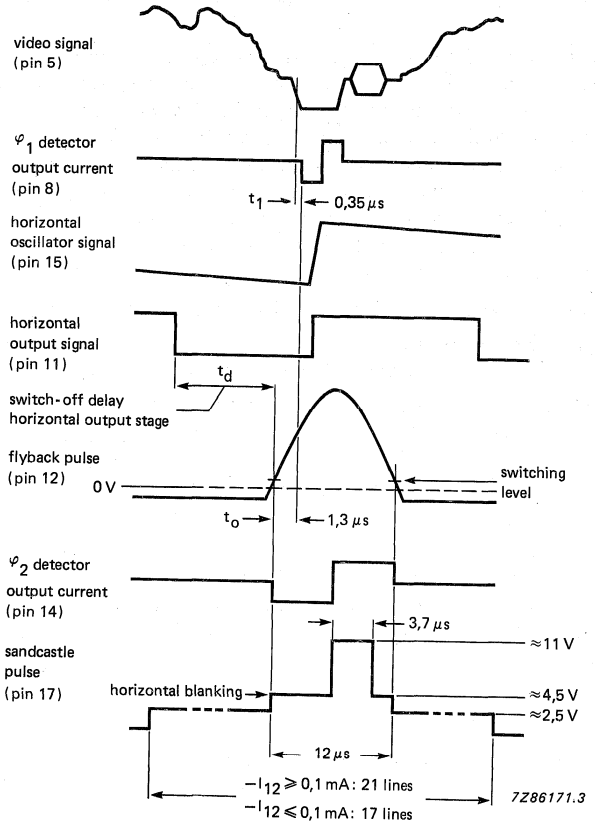


Fig. 4 Timing diagram of the TDA2577A.

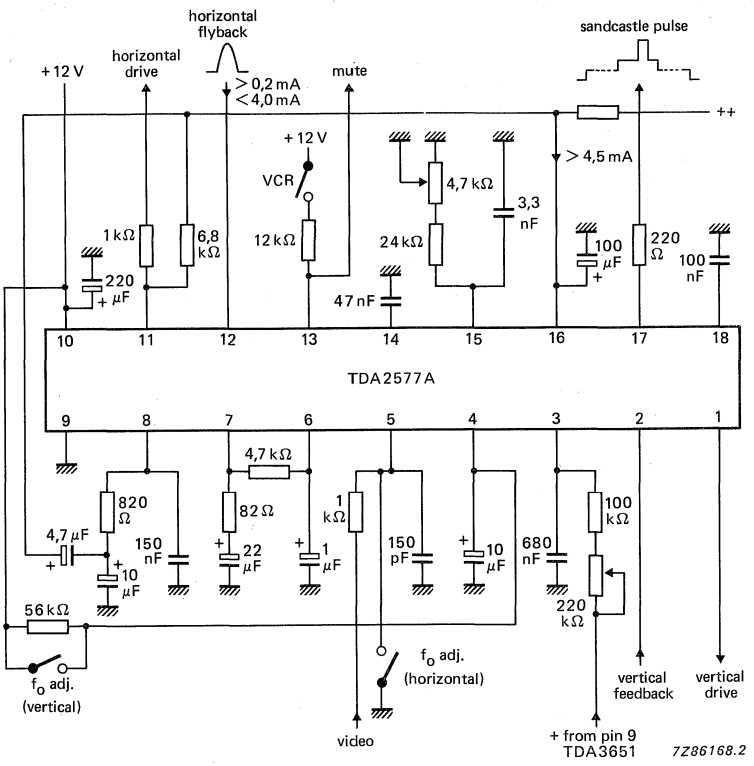


Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

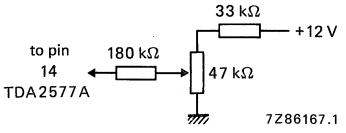


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

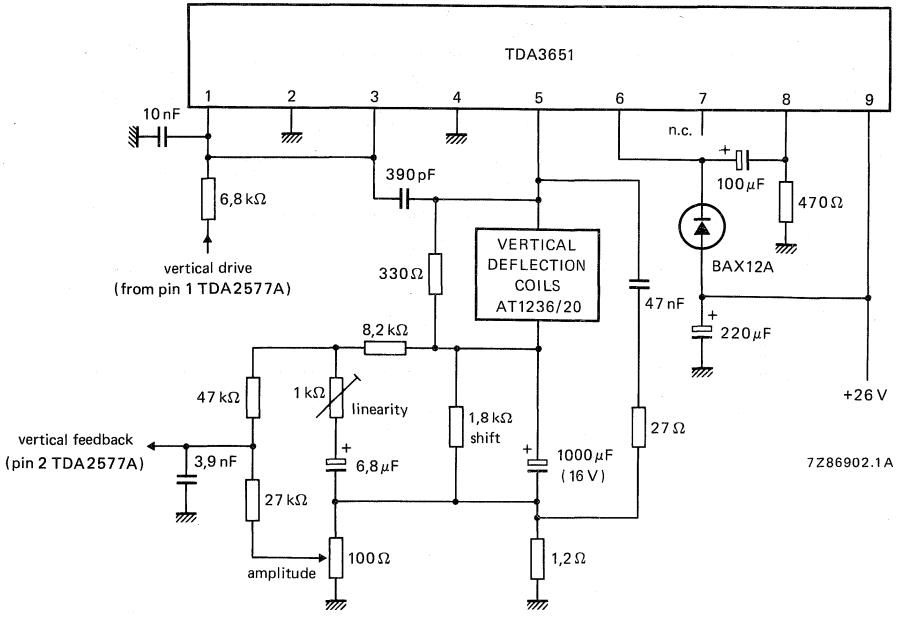


Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4,5 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0,15 to 1 V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0,5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

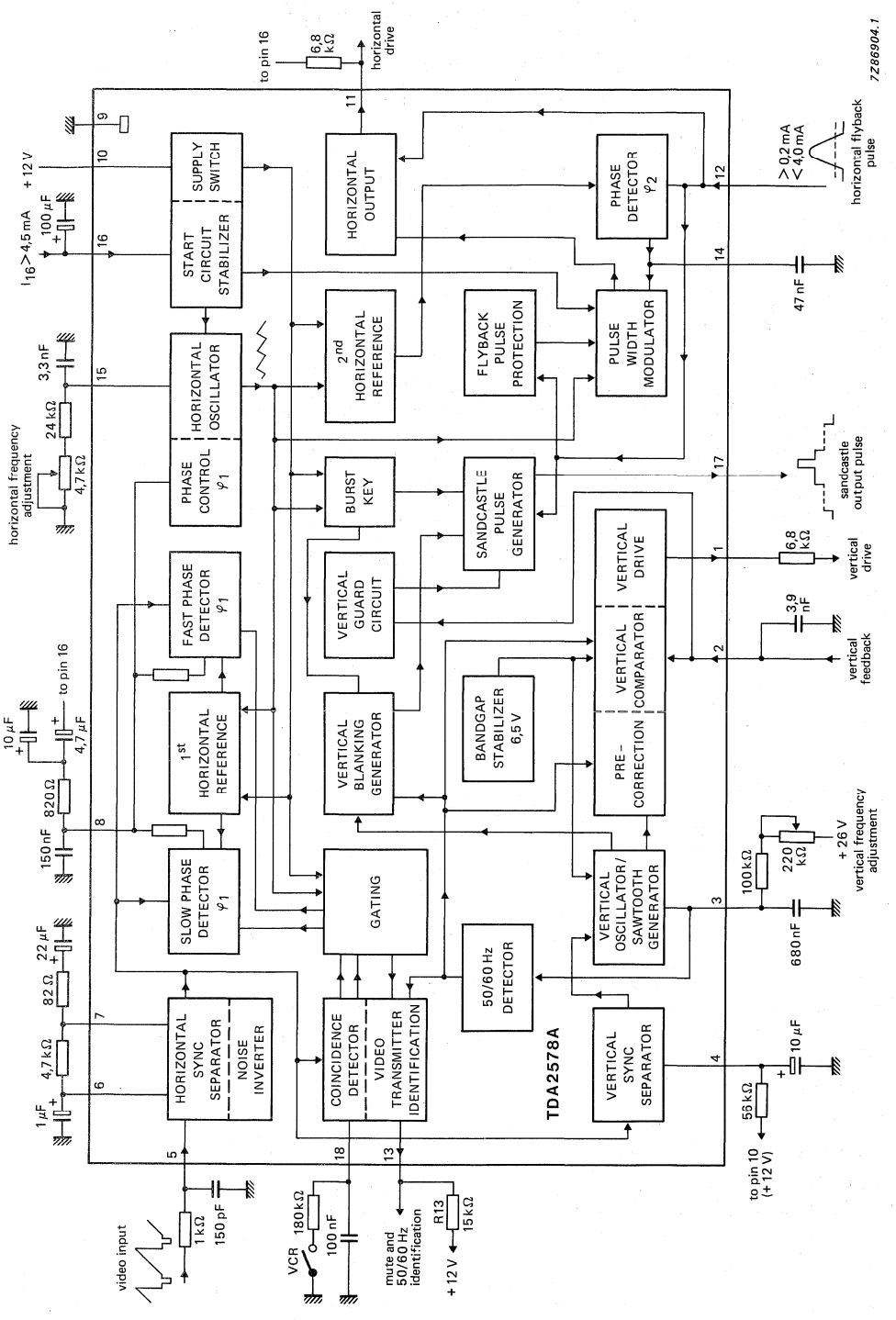


Fig. 1 Block diagram.

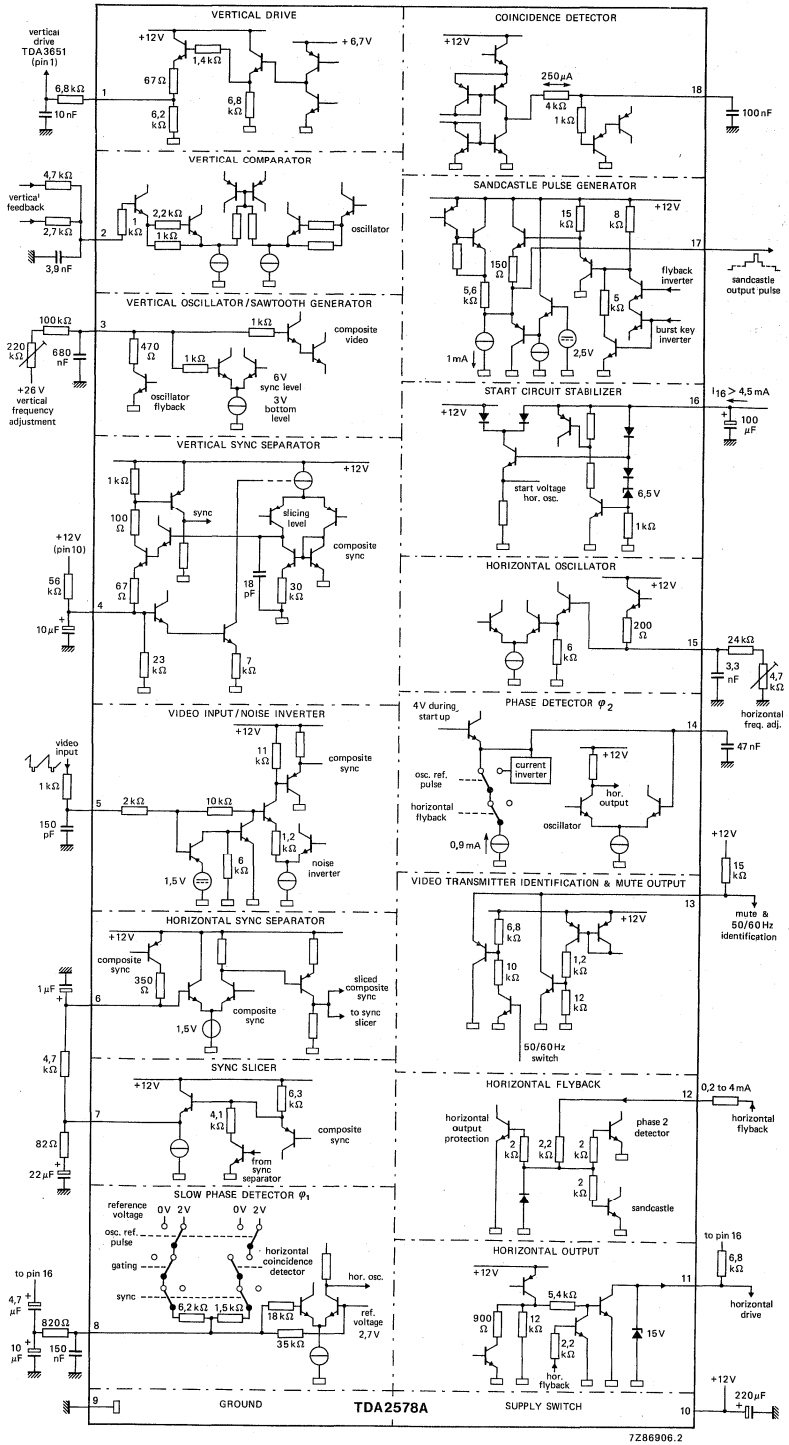


Fig. 2 TDA2578A circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,1	W
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−25 to +	65	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50	K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4,5 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8,7	V
			8,0 to 9,5	V
Supply current (pin 10)	I_{10}	typ.	55	mA
		<	70	mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12	V
			10 to 13,2	V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3,1	V
			1,5 to 3,75	V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0,6	V
			0,15 to 1	V
Slicing level		typ.	50	%
			35 to 65	%
Delay between video input and detector output	t_1	typ.	0,35	μs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0,7	V
		<	1	V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800	Hz
Catching range	Δf	typ.	± 800	Hz
			±600 to ±1100	Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse				
for slow time constant		typ.	1	kHz/μs
for fast time constant		typ.	2,75	kHz/μs

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	60	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 3,3 nF; R_{osc} = 24 kΩ; no sync)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	V_{11-9}	<	13,2	V
Voltage at which protection starts	V_{11-9}		13 to 15,8	V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0,3 0,5	V V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0,3 0,5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ. 	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	V_{17-9}	>	10	V
horizontal blanking	V_{17-9}	typ. 	4,6 4,2 to 5	V V
vertical blanking	V_{17-9}	typ. 	2,5 2 to 3	V V
Pulse duration burst key	t_p	typ. 	3,7 3,3 to 4,1	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking at 50 Hz at 60 Hz	 21 lines 17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	5,2 μs
			4,8 to 5,6 μs
Delay between start of sync and trailing edge of burst key	t_2	typ.	8,8 μs
			8,1 to 9,3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0,3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7,5 V
Switching level slow to fast	V_{18-9}	typ.	3,5 V
			3,2 to 3,8 V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1,2 V
			1,0 to 1,4 V
vertical period counter 3 periods fast	V_{18-9}	typ.	0,12 V
			0,08 to 0,16 V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1,7 V
			1,5 to 1,9 V
Switching level fast to slow (locking)	V_{18-9}	typ.	5,0 V
			4,7 to 5,3 V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8,6 V
			8,2 to 9,0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	<	0,5 V
		typ.	0,3 V
Sink current active (no sync)	I_{13}	⩽	5 mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1 μA
50/60 Hz identification (pin 13)			
R13 = 15 kΩ to + 12 V (note 5) at f = 50 Hz (in sync condition)	V_{13-9}	typ.	V_{10-9} V
at f = 60 Hz (in sync condition)	V_{13-9}	typ.	7,6 V
			7,2 to 8 V
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0,2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2,7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1,3 μs

Vertical sawtooth generator (pin 3)			
Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 187 kΩ; at + 26 V)	Δf_s	<	4 %
Synchronization range (note 6)		typ.	33 %
Input current at V_{3-9} = 6 V	I_3	<	3 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0,2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Comparator (pin 2)			
Input voltage; d.c. level	V_{2-9}	typ.	4,4 V
			4,0 to 4,8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	0,8 V
Input current at V_{2-9} = 6 V	I_2	<	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6 %
Vertical output stage; emitter follower (pin 1)			
Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3,6 V
			3,2 to 5 V
Output current	I_1	<	20 mA
Vertical guard circuit			
Activating voltage levels (vertical blanking level is 2,5 V)			
switching level low	V_{2-9}	typ.	3,35 V
			3,0 to 3,7 V
switching level high	V_{2-9}	typ.	5,15 V
			4,75 to 5,55 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

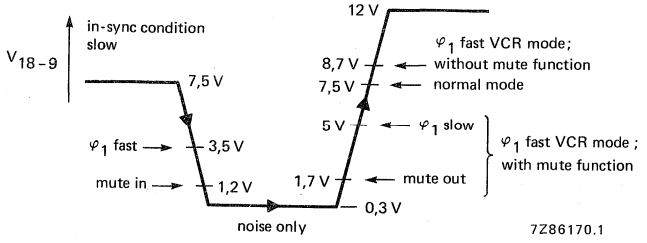


Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4{,}5$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7,5 V	X		X			X	video signal detected
7,5 to 3,5 V	X		X			X	video signal detected
3,5 to 1,2 V		X		X		X	video signal detected
1,2 to 0,1 V	X		X		X		noise only
0,1 to 1,7 V	X	*	X	*	X		new video signal detected
1,7 to 5,0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5,0 to 7,5 V	X		X			X	horizontal oscillator locked
8,7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 4,2 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4{,}5$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

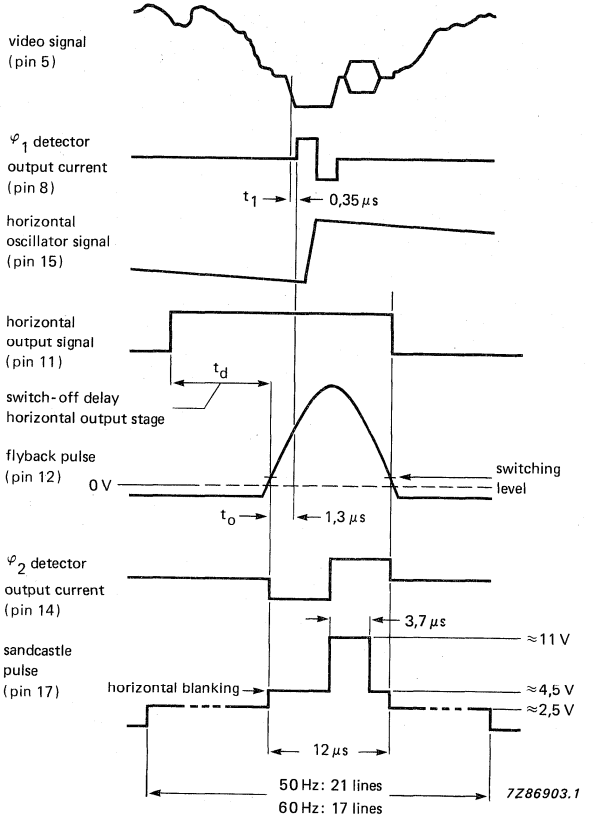
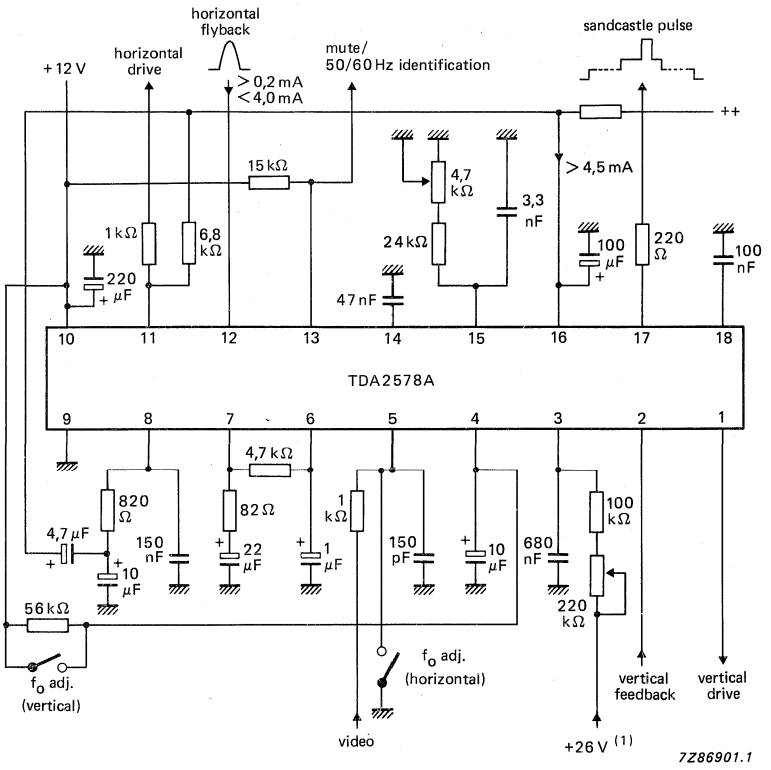


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

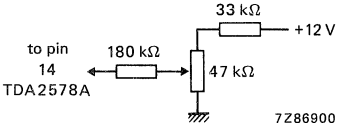


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

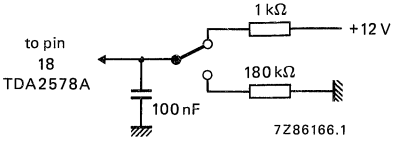


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

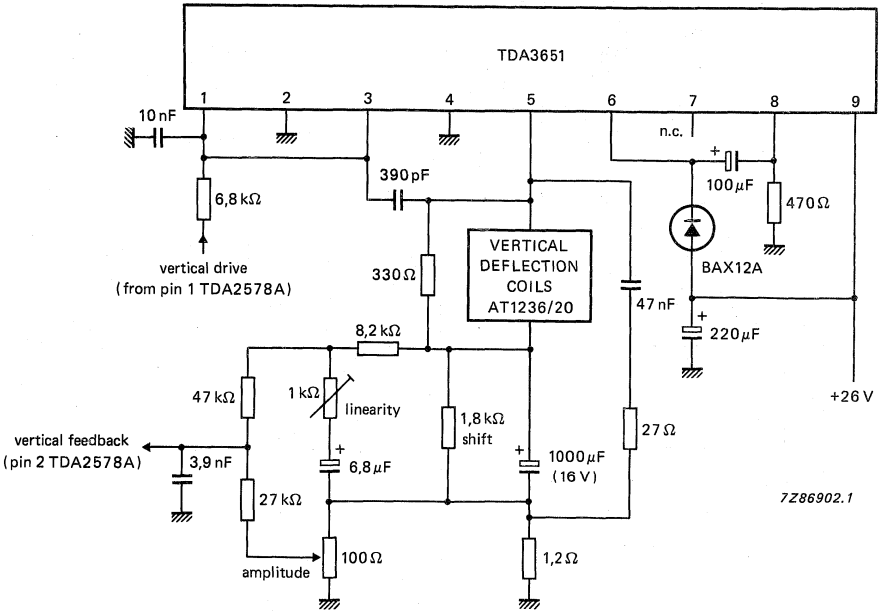


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

HORIZONTAL/VERTICAL SYNCHRONIZATION CIRCUIT

GENERAL DESCRIPTION

The TDA2579B generates and synchronizes horizontal and vertical signals. The device has a 3 level sandcastle output; a transmitter identification signal and also 50/60 Hz identification.

Features

- Horizontal phase detector, (sync to oscillator), sync separator and noise inverter
- Triple current source in the phase detector with automatic selection
- Second phase detector for storage compensation of the horizontal output
- Stabilized direct starting of the horizontal oscillator and output stage from mains supply
- Horizontal output pulse with constant duty cycle value of 29 μs
- Internal vertical sync separator, and two integration selection times
- Divider system with three different reset enable windows
- Synchronization is set to 628 divider ratio when no vertical sync pulses and no video transmitter is identified
- Vertical comparator with a low DC feedback signal
- 50/60 Hz identification output combined with mute function
- Automatic amplitude adjustment for 50 and 60 Hz and blanking pulse duration
- Automatic adaption of the burst-key pulsewidth

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply						
Minimum required current for starting horizontal oscillator and output stage		I_{16}	6.2	–	–	mA
Main supply voltage		V_{10}	–	12	–	V
Supply current		I_{10}	–	70	–	mA
Input signals						
Sync pulse input amplitude		$V_{5(p-p)}$	0.05	–	1.0	V
Horizontal flyback pulse input current		I_{12}	–	1	–	mA
Vertical comparator input signal						
Voltage AC		V_2	–	0.8	–	V
Voltage DC		V_2	–	1	–	V
Output signals						
Horizontal output (open collector) I_{11} = 25 mA		V_{11}	–	–	0.5	V
Vertical output stage driver (emitter follower) I_1 = 1.5 mA		V_1	5	–	–	V
Sandcastle output levels						
V_{17} burst-key		V_{17}	9.8	–	–	V
horizontal blanking		V_{17}	–	4.5	–	V
vertical blanking		V_{17}	–	2.5	–	V
Video transmitter identification output stage (open collector loaded with external resistor to positive supply). No sync. pulse present		V_{13}	–	–	0.5	V
		I_{13}	–	–	5	mA
Sync pulse present						
divider ratio > 576		V_{13}	–	V_{10}	–	V
divider ratio < 576		V_{13}	–	7.65	–	V

PACKAGE OUTLINE

18-lead dual in line; plastic (SOT102).

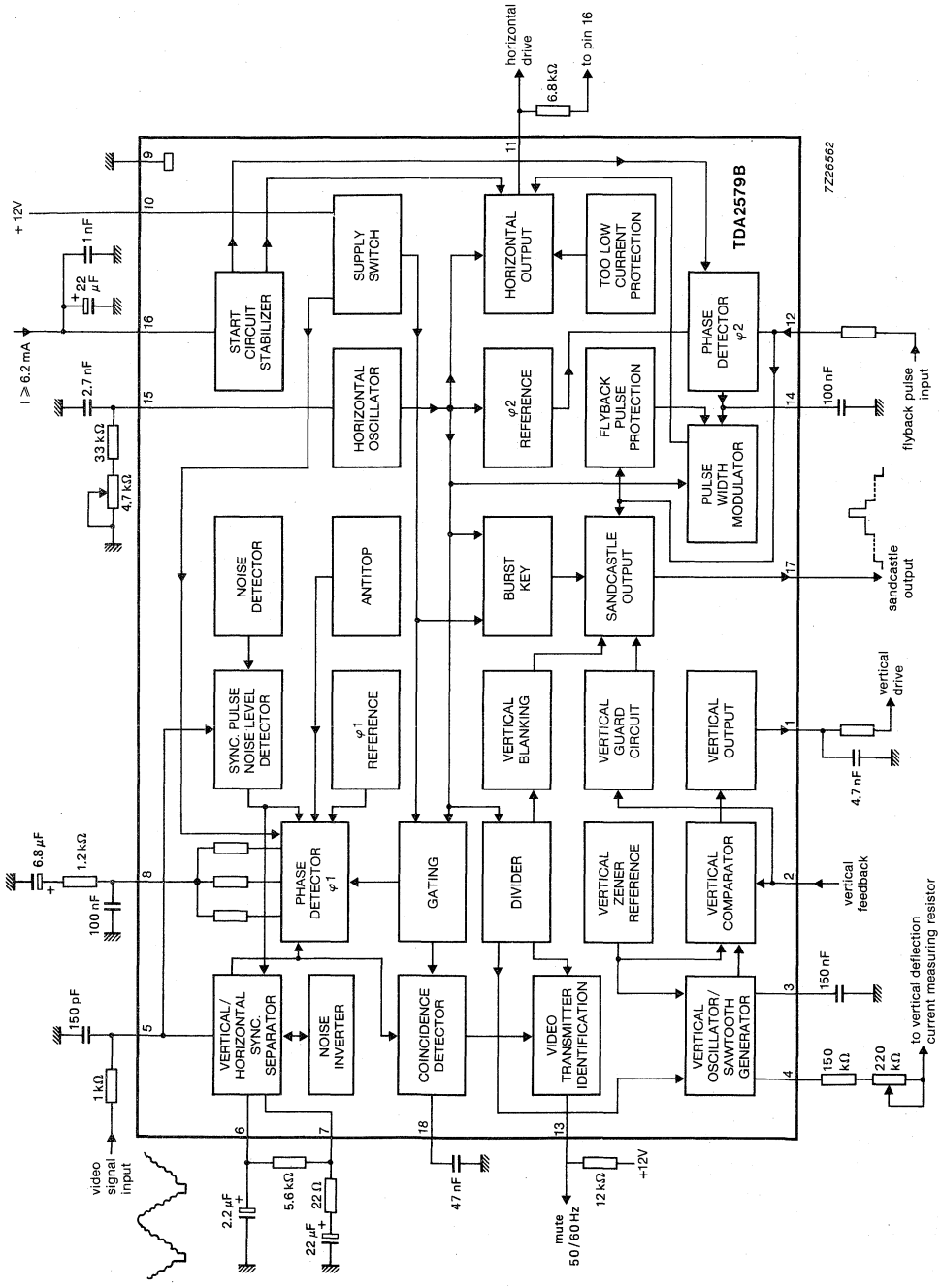


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Vertical part (pins 1,2,3,4)

The IC embodies a synchronized divider system for generating the vertical sawtooth at pin 3. The divider system has an internal frequency doubling circuit, so the horizontal oscillator is working at its normal line frequency and one line period equals 2 clock pulses. Due to the divider system no vertical frequency adjustment is needed. The divider has a discriminator window for automatically switching over from the 60 Hz to 50 Hz system. The divider system operates with 3 different divider reset windows for maximum interference/disturbance protection.

The windows are activated via an up/down counter. The counter increases its counter value by 1 for each time the separated vertical sync pulse is within the searched window. The count is decreased by 1 when the vertical sync pulse is not present.

Large (search) window: divider ratio between 488 and 722

This mode is valid for the following conditions:
1. Divider is looking for a new transmitter.
2. Divider ratio found, not within the narrow window limits.
3. Up/down counter value of the divider system operating in the narrow window mode decreases below count 1.
4. Externally setting. This can be reached by loading pin 18 with a resistor of 220 kΩ to earth or connecting a 3.6 V diode stabistor between pin 18 and ground.

Narrow window: divider ratio between 522-528 (60 Hz) or 622-628 (50 Hz).

The divider system switches over to this mode when the up/down counter has reached its maximum value of 12 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below count 1 the divider system switches over to the large window mode.

Standard TV-norm

When the up/down counter has reached its maximum value of 12 in the narrow window mode, the information applied to the up/down counter is changed such that the standard divider ratio value is tested. When the counter has reached a value of 14 the divider system is changed over to the standard divider ratio mode. In this mode the divider is always reset at the standard value even if the vertical sync pulse is missing. A missed vertical sync pulse decreases the counter value by 1. When the counter reaches the value of 10 the divider system is switched over to the large window mode. The standard TV-norm condition gives maximum protection for video recorders playing tapes with anti-copy guards.

No-TV-transmitter found: (pin 18 < 1.2 V)

In this condition, only noise is present, the divider is rest to count 628. In this way a stable picture display at normal height is achieved.

DEVELOPMENT DATA

Video tape recorders in feature mode

It should be noted that some VTRs operating in the feature modes, such as picture search, generate such distorted pictures that the no-TV-transmitter detection circuit can be activated as pin V_{18} drops below 1.2 V. This would imply a rolling picture (see Phase detector, sub paragraph d). In general VTR-machines use a re-inserted vertical sync pulse in the feature mode. Therefore the divider system has been made such that the automatic reset of the divider at count 628 when V_{18} is below 1.2 V is inhibited when a vertical sync pulse is detected.

The divider system also generates the anti-top-flutter pulse which inhibits the Phase 1 detector during the vertical sync. pulse. The width of this pulse depends on the divider mode. For the divider mode a the start is generated at the reset of the divider. In mode b and c the anti-top-flutter pulse starts at the beginning of the first equalizing pulse. The anti-top-flutter pulse ends at count 8 for 50 Hz and count 10 for 60 Hz. The vertical blanking pulse is also generated via the divider system. The start is at the reset of the divider while the blanking pulse ends at count 34 (17 lines) for 60 Hz, and at count 44 (22 lines) for 50 Hz systems. The vertical blanking pulse generated at the sandcastle output pin 17 is made by adding the anti-top-flutter pulse and the blanking pulse. In this way the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in the b or c mode. For generating a vertical linear sawtooth voltage a capacitor should be connected to pin 3. The recommended value is 150 nF to 330 nF (see Fig. 1).

The capacitor is charged via an internal current source starting at the reset of the divider system. The voltage on the capacitor is monitored by a comparator which is activated also at reset. When the capacitor has reached a voltage value of 5.85 V for the 50 Hz system or 4.85 V for the 60 Hz system the voltage is kept constant until the charging period ends. The charge period width is 26 clock pulses. At clock pulse 26 the comparator is switched off and the capacitor is discharged by an npn transistor current source, the value of which can be set by an external resistor between pin 4 and ground (pin 9). Pin 4 is connected to a pnp transistor current source which determines the current of the npn current source at pin 3. The pnp current source on pin 4 is connected to an internal zener diode reference voltage which has a typical voltage of $\approx$ 7.5 volts. The recommended operating current range is 10 to 75 μA. The resistance at pin R_4 should be 100 to 770 kΩ. By using a double current mirror concept the vertical sawtooth pre-correction can be set on the desired value by means of external components between pin 4 and pin 3, or by connecting the pin 4 resistor to the vertical current measuring resistor of the vertical output stage. The vertical amplitude is set by the current of pin 4. The vertical feedback voltage of the output stage has to be applied to pin 2. For the normal amplitude adjustment the values are DC = 1 V and AC = 0.8 V. Due to the automatic system adaption both values are valid for 50 Hz and 60 Hz.

The low DC voltage value improves the picture bounce behaviour as less parabola compensation is necessary. Even a fully DC coupled feedback circuit is possible.

Vertical guard

The IC also contains a vertical guard circuit. This circuit monitors the vertical feedback signal on pin 2. When the level on pin 2 is below 0.35 V or higher than 1.85 V the guard circuit inserts a continuous level of 2.5 V in the sandcastle output signal of pin 17. This results in the blanking of the picture displayed, thus preventing a burnt-in horizontal line. The guard levels specified refer to the zener diode reference voltage source level.

Driver output

The driver output is at pin 1, it can deliver a drive current of 1.5 mA at 5 V output. The internal impedance is approximately 170 Ω. The output pin is also connected to an internal current source with a sink current of 0.25 mA.

Sync separator, phase detector and TV-station identification (pins 5,6,7,8 and 18)

The video input signal is connected to pin 5. The sync separator is designed such that the slicing level is independent of the amplitude of the sync pulse. The black level is measured and stored in the capacitor at pin 7. The slicing level value is stored in the capacitor at pin 6. The slicing level value can be chosen by the value of the external resistor between pins 6 and 7. The value is given by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100 \quad (R_S \text{ value in } k\Omega)$$

Where R_S is the resistor between pins 6 and 7 and top sync level equals 100%. The recommended resistor value is 5.6 kΩ.

Black level detector

A gating signal is used for the black level detector. This signal is composed of an internal horizontal reference pulse with a duty factor of 50% and the flyback pulse at pin 12. In this way the TV-transmitter identification operates also for all DC conditions at input pin 5 (no video modulation, plain carrier only).
During the frame interval the slicing level detector is inhibited by a signal which starts with the anti-top flutter pulse and ends with the reset vertical divider circuit. In this way shift of the slicing level due to the vertical sync signal is reduced and separation of the vertical sync pulse is improved.

DEVELOPMENT DATA

Noise level detector

An internal noise inverter is activated when the video level at pin 5 decreases below 0.7 V. The IC also embodies a built-in sync pulse noise level detection circuit. This circuit is directly connected to pin 5 and measures the noise level at the middle of the horizontal sync pulse. When a signal-to-noise level of 19 dB is detected a counter circuit is activated. A video input signal is processed as "acceptable noise free" when 12 out of 15 sync pulses have a noise level below 19 dB for two successive frame periods. The sync pulses are processed during a 15 line width gating period generated by the divider system. The measuring circuit has a built-in noise level hysteresis of approximately 3 dB.
When the "acceptable noise free" condition is found the phase detector of pin 8 is switched to not gated and normal time constant. When a higher sync pulse noise level is found the phase detector is switched over to slow time constant and gated sync pulse phase detection. At the same time the integration time of the vertical sync pulse separator is adapted.

$$S/N = 20 \text{ Log} \frac{\text{Video voltage (black to white}_{p\text{-}p})}{\text{Noise}_{rms}}$$

Phase detector

The phase detector circuit is connected to pin 8. This circuit consists of 3 separate phase detectors which are activated depending on the voltage of pin 18 and the state of the sync pulse noise detection circuit. For normal and fast time constants all three phase detectors are activated during the vertical blanking period, this with the exception of the anti-top-flutter pulse period, and the separated vertical sync-pulse time. As a result, phase jumps in the video signal related to the video head, take over of video recorders are quickly restored within the vertical blanking period. At the end of the blanking period the phase detector time constant is increased by 1.5 times. In this way there is no requirement for external VTR time constant switching, and so all station numbers are suitable for signals from VTR, video games or home computers.
For quick locking of a new TV station starting from a noise only signal condition (normal time constant) a special circuit is incorporated. A new TV station which is not locked to the horizontal oscillator will result in a voltage decrease below 0.1 V at pin 18. This will activate a frame period counter which switches the phase detector to fast for 3 frame periods during the vertical scan period.

The horizontal oscillator will now lock to the new TV-station and as a result, the voltage on pin 18 will increase to approximately 6.5 V. When pin 18 reaches a level of 1.8 V the mute output transistor of pin 13 is switched OFF and the divider is set to the large window. In general the mute signal is switched OFF within 5 ms (pin C_{18} = 47 nF) after reception of a new TV-signal. When the voltage on pin 18 reaches a level of 5 V, usually within 15 ms, the frame counter is switched OFF and the time constant is switched from fast to normal during the vertical scan period.

If the new TV station is weak, the sync-noise detector is activated. This will result in a change over of pin 18 voltage from 6.5 V to ≈ 10 V. When pin 18 exceeds the level of 7.8 V the phase detector is switched to slow time constant and gated sync pulse condition. The current is also reduced during the vertical blanking period by 1 mA. When desired, most conditions of the phase detector can also be set by external means in the following way:

a. Fast time constant TV transmitter identification circuit not active, connect pin 18 to earth (pin 9).
b. Fast time constant TV transmitter identification circuit active, connect a resistor of 220 kΩ between pin 18 and ground.
   This condition can also be set by using a 3.6 V stabistor diode instead of a resistor.
c. Slow time constant, (with exception of frame blanking period), connect pin 18 via a resistor of 10 kΩ to + 12 V, pin 10. In this condition the transmitter identification circuit is not active.
d. No switching to slow time constant desired (transmitter identification circuit active), connect a 6.8 V zener diode between pin 18 and ground.

Fig. 2 illustrates the operation of the 3 phase detector circuits.

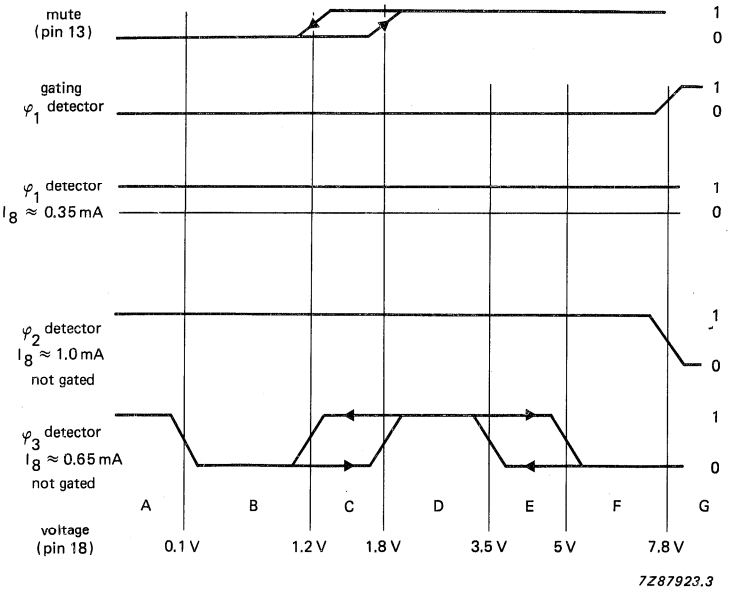


Fig. 2 Timing diagram, phase detectors.

Supply (pins 9, 10 and 16)

The IC has been designed such that the horizontal oscillator and output stage can start operating by application of a very low supply current into pin 16.

The horizontal oscillator starts at a supply current of approximately 4 mA. The horizontal output stage is forced into the non-conducting stage until the supply current has a typical value of 5 mA. The circuit has been designed so that after starting the horizontal output function a current drop of $\approx$ 1 mA is allowed. The starting circuit has the ability to derive the main supply (pin 10) from the horizontal output stage. The horizontal output signal can also be used as the oscillator signal for synchronized switched mode power supplies. The maximum allowed starting current is 9.7 mA (T_{amb} = 25 °C). The main supply should be connected to pin 10, and pin 9 should be used as ground. When the voltage on pin 10 increases from zero to its final value (typically 12 V) a part of the supply current of the starting circuit is taken from pin 10 via internal diodes, and the voltage on pin 16 will stabilize to a typical value of 9.4 V.

In a stabilized condition (pin $V_{10} > 10$ V) the minimum required supply current to pin 16 is $\approx$ 2.5 mA. All other IC functions are switched on via the main supply voltage on pin 10. When the voltage on pin 10 reaches a value of $\approx$ 7 V the horizontal phase detector circuit is activated and the vertical ramp on pin 3 is started. The second phase detector circuit and burst pulse circuit are started when the voltage on pin 10 reaches the stabilized voltage value of pin 16 which is typically 9.4 V.

To close the second phase detector loop, a flyback pulse must be applied to pin 12. When no flyback pulse is detected the duty factor of the horizontal output stage is 50%.

For remote switch-off pin 16 can be connected to ground (via a npn transistor with a series resistor of $\approx$ 500 Ω) which switches off the horizontal output.

Horizontal oscillator, horizontal output transistor, and second phase detector (pins 11, 12, 14 and 15)

The horizontal oscillator is connected to pin 15. The frequency is set by an external RC combination between pin 15 and ground, pin 9. The open collector horizontal output stage is connected to pin 11. An internal zener diode configuration limits the open voltage of pin 11 to $\approx$ 14.5 V.
The horizontal output transistor at pin 11 is blocked until the current into pin 16 reaches a value of $\approx$ 5 mA.
A higher current results in a horizontal output signal at pin 11, which starts with a duty factor of $\approx$ 40% HIGH.

The duty factor is set by an internal current-source-loaded npn emitter follower stage connected to pin 14 during starting. When pin 16 changes over to voltage stabilization the npn emitter follower and current source load at pin 14 are switched OFF and the second phase detector circuit is activated, provided a horizontal flyback pulse is present at pin 12. When no flyback pulse is detected at pin 12 the duty factor of the horizontal output stage is set to 50%.

The phase detector circuit at pin 14 compensates for storage time in the horizontal deflection output stage. The horizontal output pulse duration is 29 μs HIGH for storage times between 1 μs and 17 μs (flyback pulse of 12 μs). A higher storage time increases the HIGH time. Horizontal picture shift is possible by forcing an external charge or discharge current into the capacitor at pin 14.

Mute output and 50/60 Hz identification (pin 13)

The collector of an npn transistor is connected to pin 13. When the voltage on pin 18 drops below 1.2 V (no TV-transmitter) the npn transistor is switched ON.
When the voltage on pin 18 increases to a level of $\approx$ 1.8 V (new TV-transmitter found) the npn transistor is switched OFF.

Pin 13 has also the possibility for 50/60 Hz identification. This function is available when pin 13 is connected to pin 10 (+ 12 V) via an external pull-up resistor of 10 to 20 kΩ. When no TV-transmitter is identified the voltage on pin 13 will be LOW ($<$ 0.5 V). When a TV-transmitter with a divider ratio $>$ 576 (50 Hz) is detected the output voltage of pin 13 is HIGH (+ 12 V).
When a TV-transmitter with a divider ratio $<$ 576 (60 Hz) is found an internal pnp transistor with its emitter connected to pin 13 will force this pin output voltage down to $\approx$ 7.6 V.

Sandcastle output (pin 17)

The sandcastle output pulse generated at pin 17, has three different voltage levels. The highest level, (10.4 V), can be used for burst gating and black level clamping. The second level (4.5 V) is obtained from the horizontal flyback pulse at pin 12, and is used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived via the vertical divider system. For 50 Hz the blanking pulse duration is 44 clock pulses and for 60 Hz it is 34 clock pulses started from the vertical divider reset. For TV-signals which have a divider ratio between 622 and 628 or between 522 and 528 the pulse is started at the first equalizing pulse. With the 50/60 Hz information the burst-key pulse width is switched to improve the behaviour in multi-norm concepts.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Start current	I_{16}	–	9.7	mA
Supply voltage	V_{10}	–	13.2	V
Total power dissipation	P_{tot}	–	1.2	W
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−25	+ 70	°C

Thermal resistance

From junction to ambient in free air $R_{th\ j\text{-}a}$ 50 K/W

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = 25 °C; I_{16} = 6.2 mA; V_{10} = 12 V; unless otherwise specified
Voltage measurements are taken with respect to pin 9 (ground)

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current (pin 16)						
V_{10} = 0 V		I_{16}	6.2	–	9.7	mA
V_{10} = 10 V		I_{16}	2.5	–	9.7	mA
Stabilized voltage (pin 16)		V_{16}	8.8	9.3	9.7	V
Current consumption (pin 10)		I_{10}	–	70	85	mA
Supply voltage range (pin 10)		V_P	10	12	13.2	V
Video input (pin 5)						
Top sync level		V_5	1.5	3.1	3.75	V
Sync pulse amplitude (peak-to-peak value)	note 1	$V5_{(p-p)}$	0.05	0.6	1.0	V
Slicing level	note 2		35	50	65	%
Delay between video input and detector output (see also Fig. 3)			0.2	0.3	0.55	µs
Sync pulse noise level detector circuit active	note 3	S/N	–	19	–	dB
Sync pulse						
Noise level detector circuit hysteresis			–	3	–	dB
Noise gate (pin 5)						
Switching level		V_5	–	+ 0.7	+ 1	V
First control loop (pin 8) (horizontal oscillator to sync)						
Holding range		Δf	–	± 800		Hz
Catching range		Δf	± 700	± 800	± 1100	
Control sensitivity video with respect to burst-key and flyback-pulse						
Slow time constant			–	2	–	kHz/µs
Normal time constant			–	5	–	kHz/µs
Fast time constant			–	3	–	kHz/µs
Phase modulation due to hum on the supply line (pin 10)	note 4		–	0.2	–	µs/Vtt
Phase modulation due to hum on input current (pin 16)	note 4		–	0.08	–	µs/Vtt

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Second control loop (pin 14) (horizontal flyback to horizontal oscillator)						
Control sensitivity	t_d = 10 µs	$\Delta t_d/\Delta t_o$	200	300	600	µs
Control range		t_d	1	—	>45	µs
Control range for constant duty factor horizontal output		t_d	1	29 (−t flyback pulse)		µs
Controlled edge of horizontal output signal (pin 11)				positive		
Phase adjustment (pin 14) (via second control loop)						
Control sensitivity	t_d = 10 µs		—	25	—	µA/µs
Maximum allowed control current		I_{14}	—	—	± 60	µA
Horizontal oscillator (pin 15)	C = 2.7 nF; R_{osc} = 34.8 kΩ					
Frequency (no sync)		f	—	15625	—	Hz
Spread (fixed external component, no sync)		Δf	—	—	± 4	%
Frequency deviation between starting point output signal and stabilized condition		Δf	—	+ 5	+ 8	%
Temperature coefficient		T_C	—	-1.10^{-4}	—	/K
Horizontal output (pin 11) (Open collector)						
Output voltage high		V_{11}	—	—	13.2	V
Start voltage protection (internal zener diode)		V_{11}	13	—	15.8	V
Low input current (pin 16) protection output enabled		I_{16}	—	5.0	6.2	mA
Output voltage low start condition	I_{11} = 10 mA	V_{11}	—	0.1	0.5	V
Duty factor output current during starting	I_{16} = 6.2 mA		50	60	70	%
Output voltage low normal condition	I_{11} = 25 mA	V_{11}	—	0.3	0.5	V
Duty factor output current without flyback pulse (pin 12)			45	50	55	%
Duration of the output pulse HIGH	t_d = 10 µs		27	29	31	µs
Controlled edge				positive		
Temperature coefficient horizontal output pulse			—	-5.10^{-2}	—	µs/°C
Influence of delay time on pulse width of the horizontal output signal		$\Delta H_W/t_d$	—	0.16	—	µs/µs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Sandcastle output signal (pin 17)	I_L = 1 mA					
Output voltage during:						
burst-key		V_{17}	9.8	10.4	–	V
horizontal blanking		V_{17}	4.1	4.5	4.9	V
vertical blanking	I_L = 0.3 mA	V_{17}	2.1	2.5	2.9	V
Zero level output voltage	I_{sink} = 0.5 mA	V_{17}	–	–	0.7	V
Pulse width:						
burst-key (50 Hz)		t_p	3.85	4.15	4.6	µs
burst-key (60 Hz)		t_p	3.40	3.65	4.0	µs
Horizontal blanking		V_{12}	–	1.0	–	V
Vertical blanking	note 5					
Phase position burstkey time between middle sync pulse at pin 5 and start of burst pulse at pin 17			2.3	2.7	3.1	µs
Time between start sync pulse and end of burst pulse at pin 17						
(50 Hz)			–	9.3	9.7	µs
(60 Hz)			–	8.8	9.2	µs
Coincidence detector, video transmitter identification circuit and time constant switching levels (see also Fig. 1)						
Detector output current		I_{18}	–	0.25	–	mA
Voltage level for in sync condition (φ_1 normal)		V_{18}	5.8	6.5	7.0	V
Voltage for noisy sync pulse (φ_1 slow and gated)		V_{18}	9	10	–	V
Voltage level for noise only	note 6	V_{18}	–	0.3	–	V
Switching level normal to fast		V_{18}	<3.2	3.5	3.8	V
Switching level mute output active and fast to normal		V_{18}	<1.0	1.2	1.4	V
Switching level frame period counter (3 periods fast)		V_{18}	<0.08	0.12	0.16	V
Switching level: normal to fast (locking) mute output inactive		V_{18}	>1.5	1.75	2.0	V
Switching level fast to normal (locking)		V_{18}	>4.7	5.0	5.3	V
Switching level normal to slow (gated sync pulse)		V_{18}	7.4	7.8	8.2	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Video transmitter identification output (pin 13)						
Output voltage active (no sync)	I_{13} = 1 mA	V_{13}	–	0.15	0.32	V
Sink current active (no sync)	$V_{13} < 1$ V	I_{13}	–	–	5	mA
Output current inactive (sync 50 Hz)		I_{13}	–	–	1	μA
50/60 Hz identification (pin 13) (R_{13} positive supply 12 kΩ)						
Emitter follower, pnp:						
60 Hz: $\frac{2 \times f_H}{f_V} < 576$ voltage		V_{13}	7.2	7.65	8.1	V
50 Hz: $\frac{2 \times f_H}{f_V} > 576$ voltage		V_{13}	–	V_{10}	–	V
Flyback input pulse (pin 12)						
Switching level		V_{12}	–	+1	–	V
Input current		I_{12}	+0.2	–	+3	mA
Input pulse		V_{12}	–	–	12	V_P
Input resistance			–	3.5	–	kΩ
Phase position without shift time between the middle of the sync pulse at pin 5 and the middle of the horizontal blanking pulse at pin 17		t_d	2.1	2.5	2.9	μs
Vertical ramp generator (pin 3)						
Pulse width charge current		–	–	26	–	clock pulses
Charge current		I_3	–	3	–	mA
Top level ramp signal voltage						
Divider in 50 Hz mode	note 7	V_3	5.5	5.85	6.3	V
Divider in 60 Hz mode	note 7	V_3	4.55	4.85	5.25	V
Ramp amplitude	C_3 = 150 nF,					
R_4 = 330 kΩ 50 Hz	note 7		–	3.1	–	V_P
R_4 = 330 kΩ 60 Hz	note 7		–	2.5	–	V_P
Temperature coefficient	I_4 = 30 μA	I_3	–	+ 100	–	10^{-6}/K

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Current source (pin 4)						
Output voltage	$I_4 = 20\ \mu A$	V_4	7.0	7.5	7.9	V
Allowed current range		I_4	10	–	75	μA
Temperature coefficient output voltage	$I_4 = 30\ \mu A$	TC	–	+ 50	–	$10^{-6}/K$
Comparator (pin 2)	$C_3 = 150$ nF; $R_4 = 330\ k\Omega$					
Input voltage						
DC level	note 7	V_2	0.97	1.07	1.17	V
AC level		V_2	–	0.8	–	V_P
Deviation amplitude 50/60 Hz			–	1.75	2.5	%
Vertical output stage (pin 1) (npn emitter follower)						
Output voltage	I_O pin 1 = +1.5 mA note 7	V_1	5.0	5.5	6.3	V
R_S, sync separator resistor			–	170	–	Ω
Continuous sink current			–	0.25	–	mA
Vertical guard circuit (pin 2)						
Active ($V_{17} = 2.5$ V)						
Switching level LOW	note 7	V_2	> 1.7	1.85	2.0	V
Switching level HIGH	note 7	V_2	< 0.25	0.35	0.45	V

Notes to the characteristics

1. Up to 1 V peak-to-peak the slicing level is constant, at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. The slicing level is fixed by the formula:

$$P = \frac{R_S}{5.3 + R_S} \times 100\% \quad (R_S \text{ value in } k\Omega)$$

3. $S/N = 20 \log \frac{\text{video voltage black to white (p-p)}}{\text{noise (rms)}}$

   measured with 1 V_{p-p} video input
4. Measured between pin 5 and sandcastle output pin 17.
5. Divider in search (large) mode:

   start: reset divider = start vertical sync plus 1 clock pulse

   stop: $\frac{n = 2 \times f_H}{f_V} > 576$ clock pulse 44

   $\frac{n = 2 \times f_H}{f_V} < 576$ clock pulse 34

   Divider in small window mode:

   start: clock pulse 517 (60 Hz) clock pulse 618 (50 Hz)

   stop: clock pulse 34 (60 Hz) clock pulse 44 (50 Hz)
6. Depends on DC level of pin 5, given value is valid for $V_5 \approx 5$ V.
7. Value related to internal zener diode reference voltage source spread includes the complete spread of reference voltage.

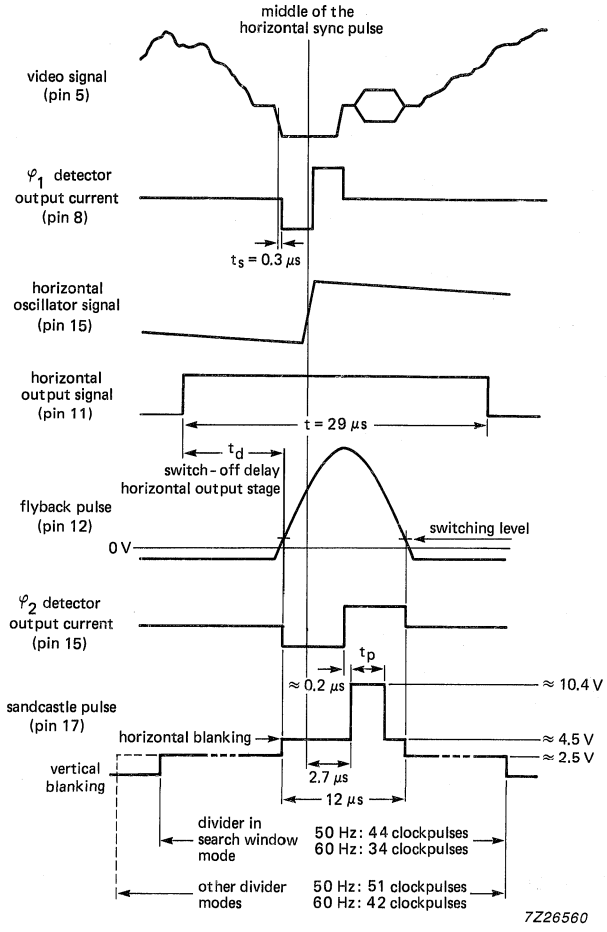


Fig.3 Timing diagram of the TDA2579B.

APPLICATION INFORMATION

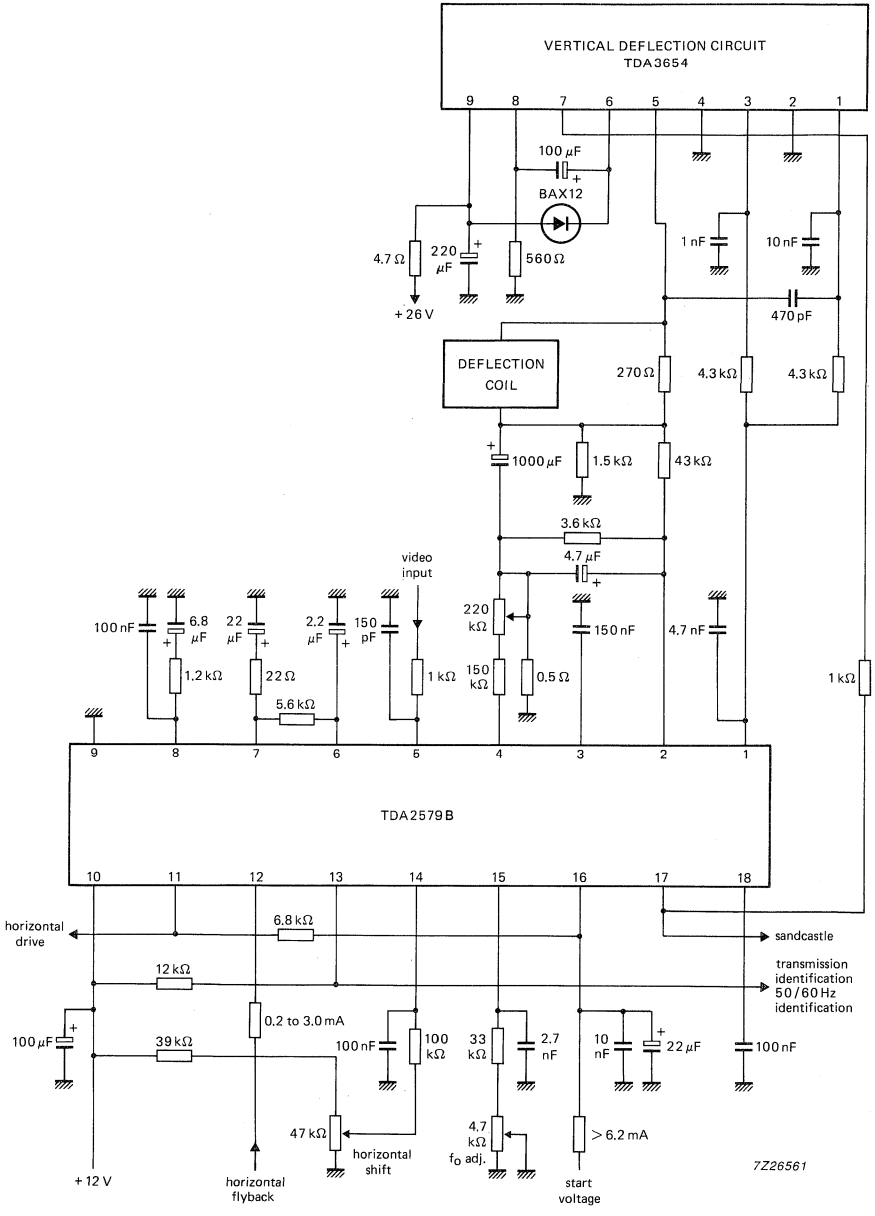


Fig.4 TDA2579B 110° application circuit (45AX).

CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:
- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

QUICK REFERENCE DATA

Supply voltage	$V_{9\text{-}16}$	typ.	12 V
Supply current	I_9	typ.	14 mA
Input signals			
Horizontal drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 11 V
Flyback pulse (differentiated deflection current); peak-to-peak value	$V_{2\text{-}16(p\text{-}p)}$		1 to 5 V
External reference voltage	$V_{10\text{-}16}$	typ.	6,1 V
Output signals			
Duty factor of output pulse	δ	$>$	0 %
		$<$	98 ± 0,8 %
Output voltage at $I_o < 20$ mA (peak value)	$V_{11\text{-}16M}$	typ.	11,8 V
Output current (peak value)	I_{11M}	$<$	40 mA

PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT38).
TDA2582Q: 16-lead QIL; plastic (SOT58).

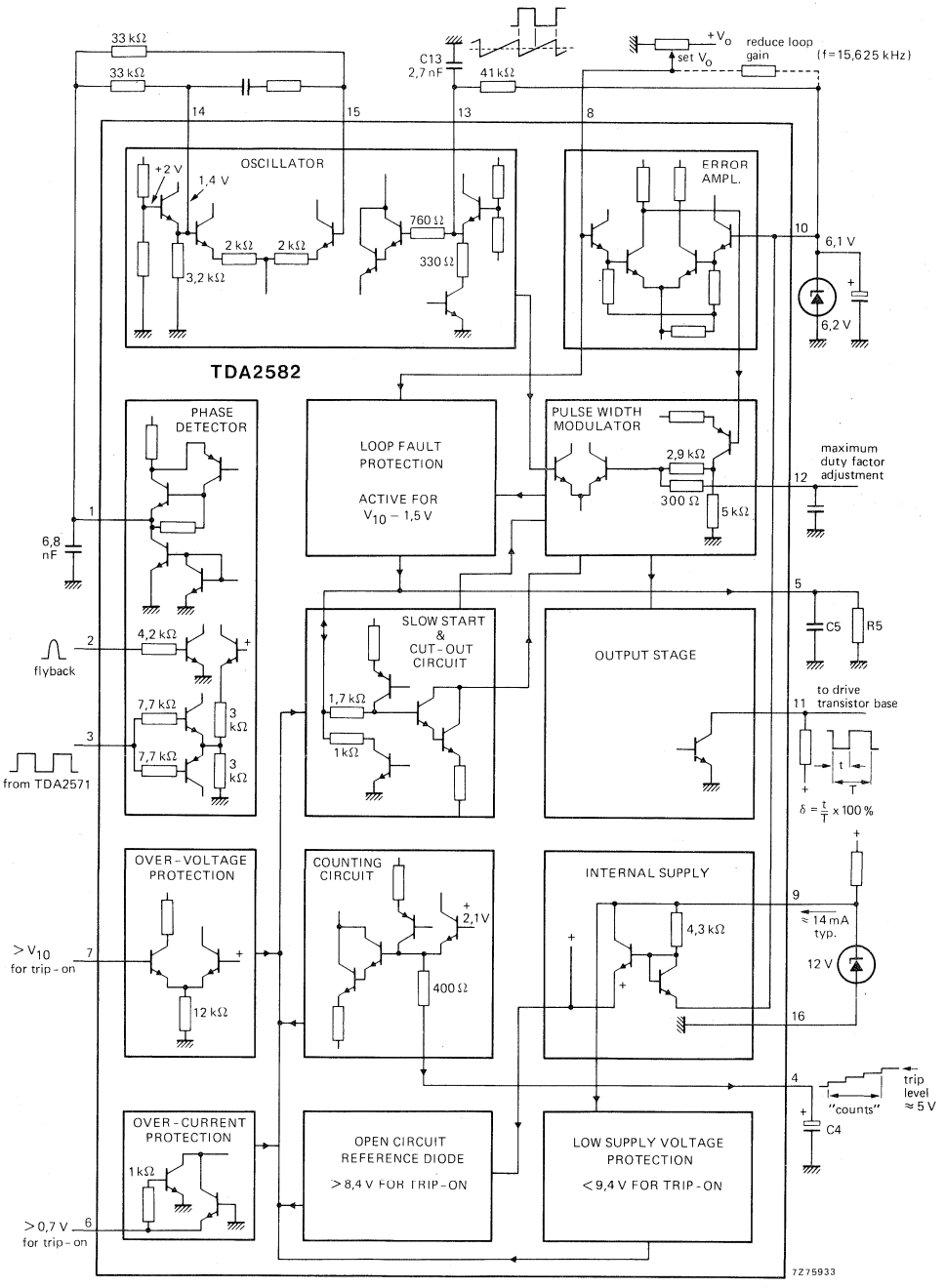


Fig. 1 Block diagram.

Note: trip levels are nominal values.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at pin 9	$V_{9\text{-}16}$	max.	14	V
Voltage at pin 11	$V_{11\text{-}16}$		0 to 14	V
Output current (peak value)	I_{11M}	max.	40	mA
Total power dissipation	P_{tot}	max.	280	mW
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 80	°C

CHARACTERISTICS

$V_{9\text{-}16}$ = 12 V; $V_{10\text{-}16}$ = 6,1 V; T_{amb} = 25 °C; measured in Fig. 4

Supply voltage range	$V_{9\text{-}16}$	typ.	12	V
			10 to 14	V
Protection voltage too low supply voltage	$V_{9\text{-}16}$	typ.	9,4	V
			8,6 to 9,9	V
Supply current at δ = 50%	I_9	typ.	14	mA
Supply current during protection	I_9	typ.	14	mA
Minimum required supply current (note 1)	I_9	<	17	mA
Power consumption	P	typ.	170	mW
Required input signals				
Reference voltage (note 2)	$V_{10\text{-}16}$	typ.	6,1	V
			5,6 to 6,6	V
Feedback input impedance	$\lvert Z_{8\text{-}16} \rvert$	typ.	200	kΩ
High reference voltage protection: threshold voltage	$V_{10\text{-}16}$	typ.	8,4	V
			7,9 to 8,9	V
Horizontal reference signal (square-wave or differentiated; negative transient is reference)				
Voltage driven (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$		5 to 12	V
Current driven (peak value)	I_{3M}		−1 to + 1,5	mA
Switching level current	$\pm I_3$	<	100	μA
Flyback pulse or differential deflection current	$V_{2\text{-}16}$		1 to 5	V
Flyback pulse current (peak value)	I_{2M}	<	1,5	mA
Over-current protection: (note 3) threshold voltage	$-V_{6\text{-}16}$	typ.	640	mV
			600 to 695	mV
	$+V_{6\text{-}16}$	typ.	680	mV
			640 to 735	mV

Notes

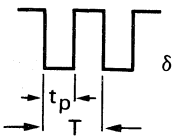
1. This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9\text{-}16}$ = 10 V; $V_{10\text{-}16}$ = 6,2 V; δ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

CHARACTERISTICS (continued)

Over-voltage protection: ($V_{ref} = V_{10-16}$) threshold voltage	V_{7-16}	typ.	V_{ref}–60 mV V_{ref}–130 to V_{ref}–0 mV
Remote control voltage; switch-off (note 1)	V_{4-16}	>	5,6 V
Remote control voltage; switch-on	V_{4-16}	<	4,5 V
'Smooth' remote control; switch-off (note 2)	V_{5-16}	>	4,5 V
'Smooth' remote control; switch-on	V_{5-16}	<	3 V
Remote control switch-off current	I_4	<	1 mA
Delivered output signals			
Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value	$V_{11-16(p-p)}$	>	11,6 V
Output current; peak value	I_{11M}	<	40 mA
Saturation voltage of output transistor at I_{11} = 20 mA	V_{CEsat}	typ. <	200 mV 400 mV
at I_{11} = 40 mA	V_{CEsat}	<	525 mV
Duty factor of output pulse (note 3)	δ	> <	0 % 98 ± 0,8 %
Charge current for capacitor on pin 4	I_4	typ.	110 μA
Charge current for capacitor on pin 5	I_5	typ.	120 μA
Supply current for reference	I_{10}	typ.	1 mA 0,6 to 1,45 mA
Oscillator			
Temperature coefficient		typ. <	0,0003 $^oC^{-1}$ 0,0004 $^oC^{-1}$
Relative frequency deviation for V_{10-16} changing from 5,6 to 6,6 V		typ. <	–1,4 % –2 %
Oscillator frequency spread (with fixed external components)		<	3 %
Frequency control sensitivity at pin 15 f_{nom} = 15,625 kHz		typ.	5 kHz/V

Notes

1. See application information pin 4.
2. See application information pin 5.
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between V_{8-16} and the duty factor is given in Fig. 7 and the relationship between V_{12-16} and the duty factor is shown in Fig. 9.



$\delta = \frac{t_p}{T} \times 100\%$.

Fig. 2.

Phase control loop

Loop gain of APC-system (automatic phase control) *		typ.	5	kHz/μs
Catching range (f_{nom} = 15,625 kHz)	Δf	>	1300	Hz
		<	2100	Hz
Phase relation between negative transient of sync pulse and middle of flyback	t	typ.	1	μs
Tolerance of phase relation	Δt	⩽	± 0,4	μs

PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

* For component values see Fig. 1.

APPLICATION INFORMATION

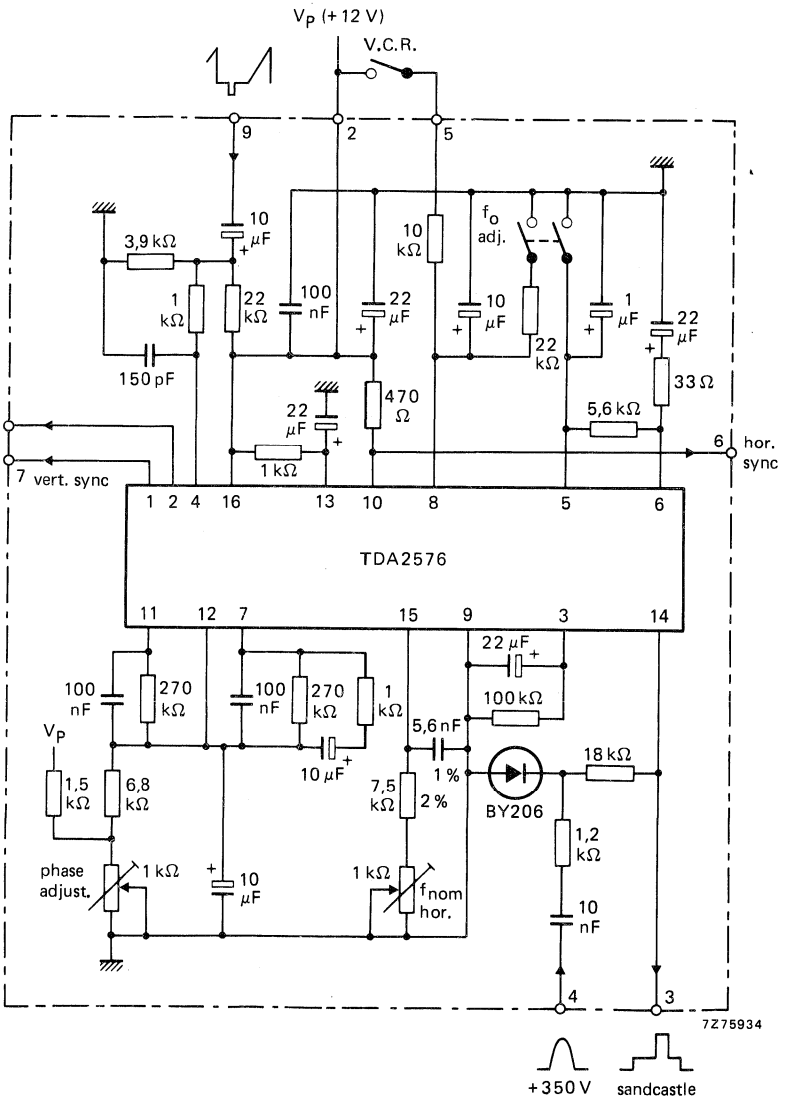


Fig. 3a.

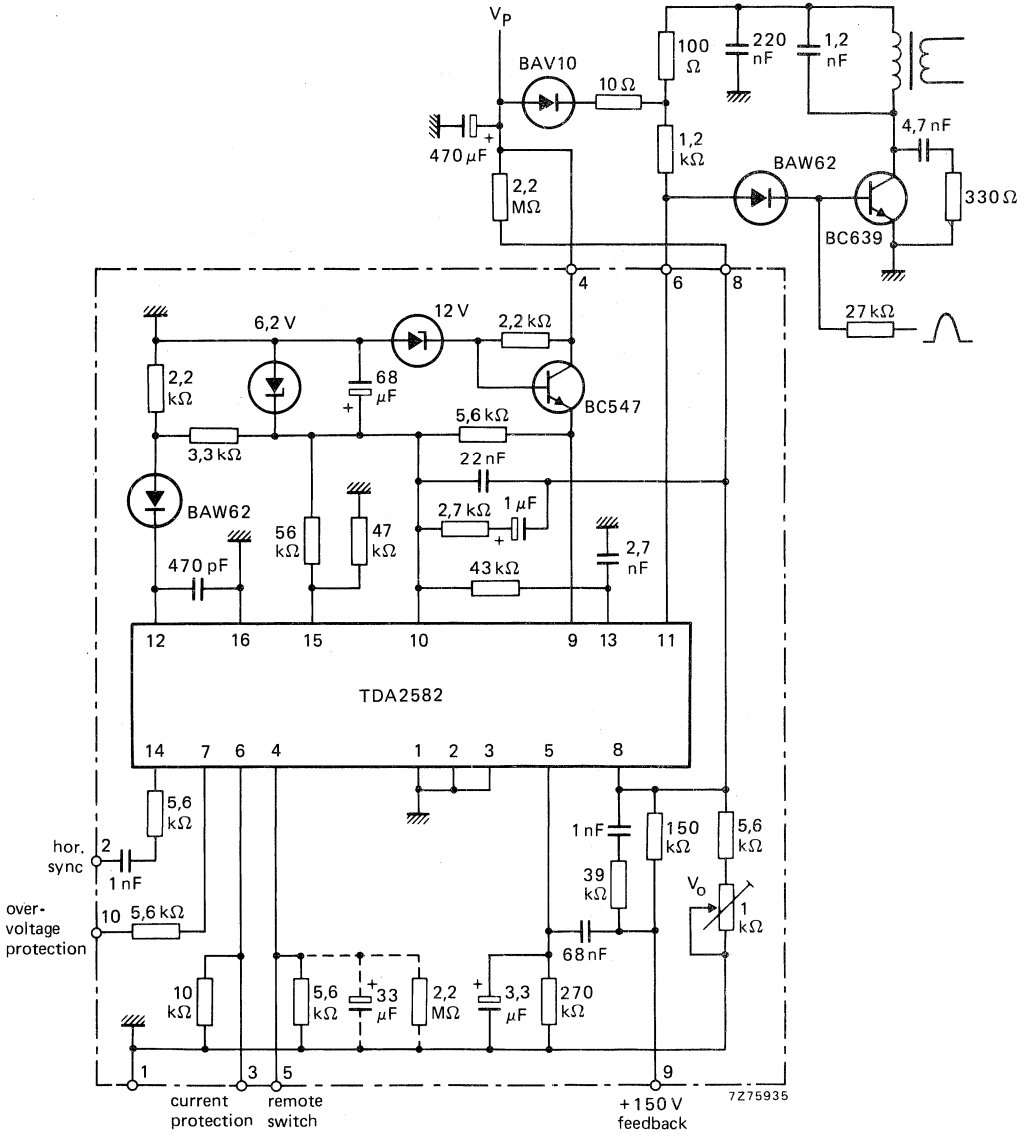


Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

APPLICATION INFORMATION

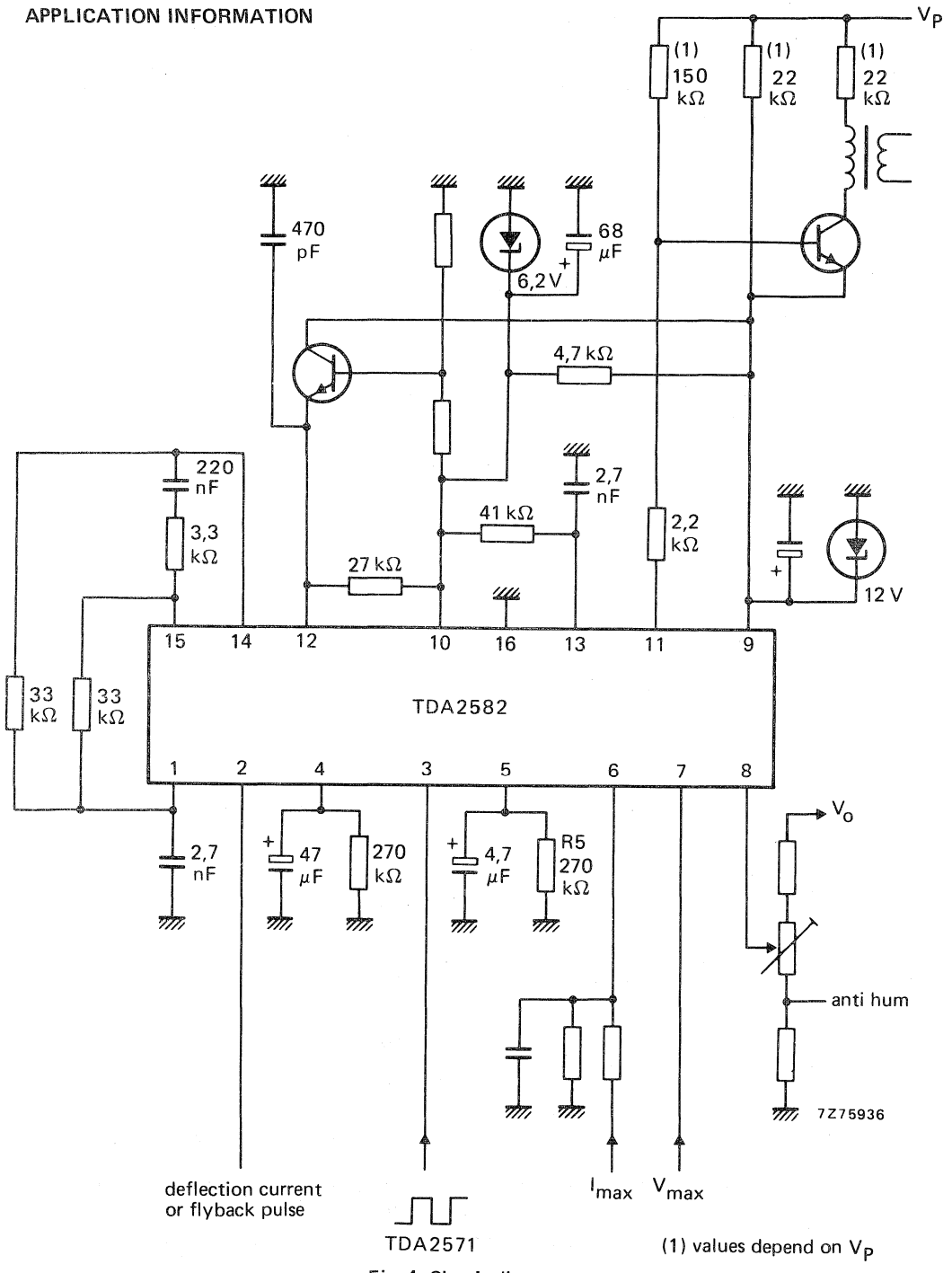


Fig. 4 Circuit diagram.

The function is described against the corresponding pin number

1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/μs (Fig. 4).

2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 μs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 μs).

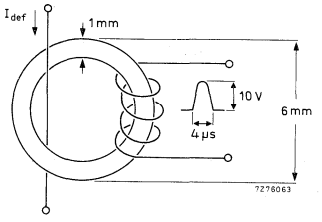


Fig. 5a.

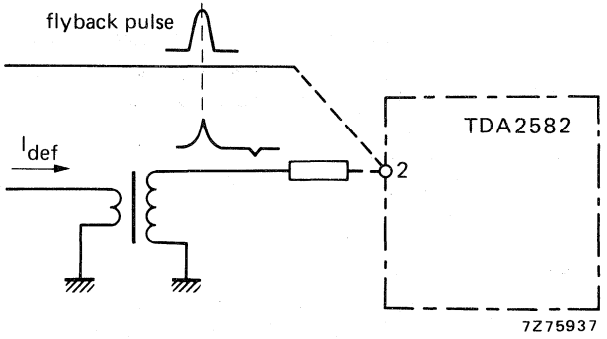


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

4. Re-start count capacitor/remote control input

Counting

An external capacitor (C4 = 47 μF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

APPLICATION INFORMATION (continued)

Remote control input

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

Slow start

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

Transfer characteristic for low feedback voltages

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in Fig. 7.

'Smooth' remote ON/OFF

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

Maximum duty factor adjustment

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

Smoothing

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16} = 6{,}1$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

16. Negative supply (ground)

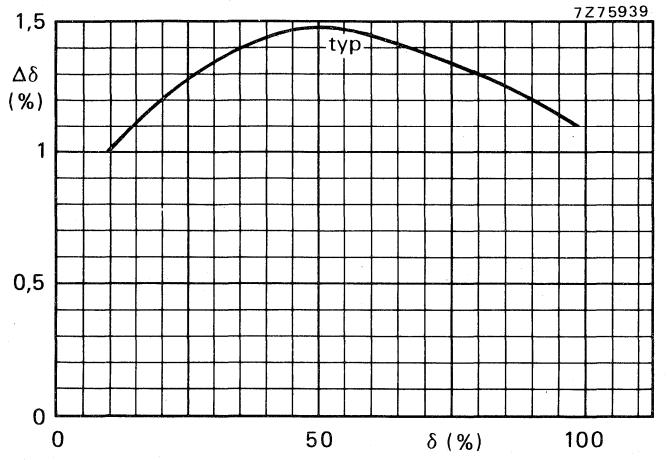


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)} = 1$ mV.

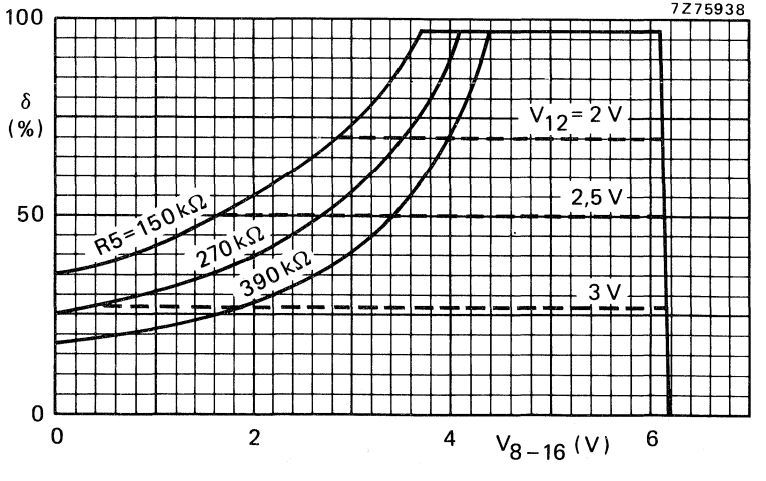


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16} = 6{,}1$ V.

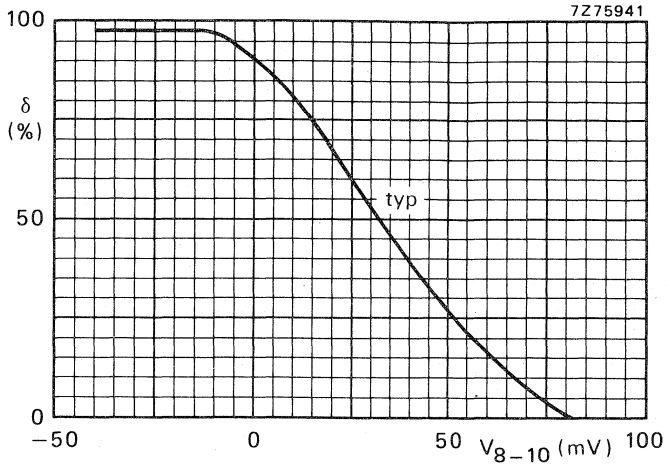


Fig. 8 Duty factor of output pulses as a function of error amplifier input (V_{8-10}); V_{10-16} = 6,1 V.

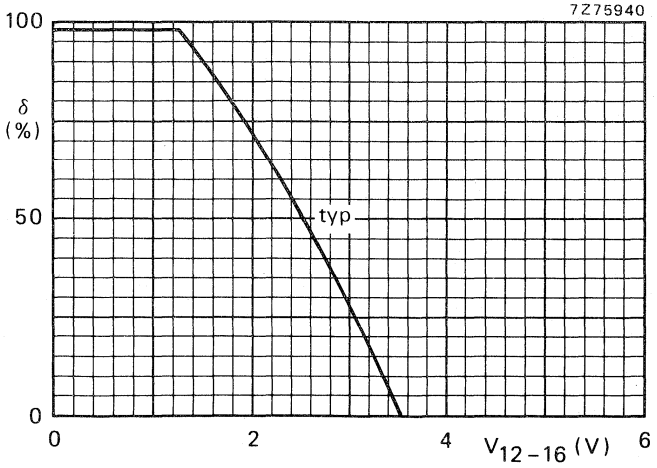


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; V_{10-16} = 6,1 V.

HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3,5 V
at t = 0 (input 4 open or $V_{3\text{-}16}$ = 0)	$V_{4\text{-}16}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

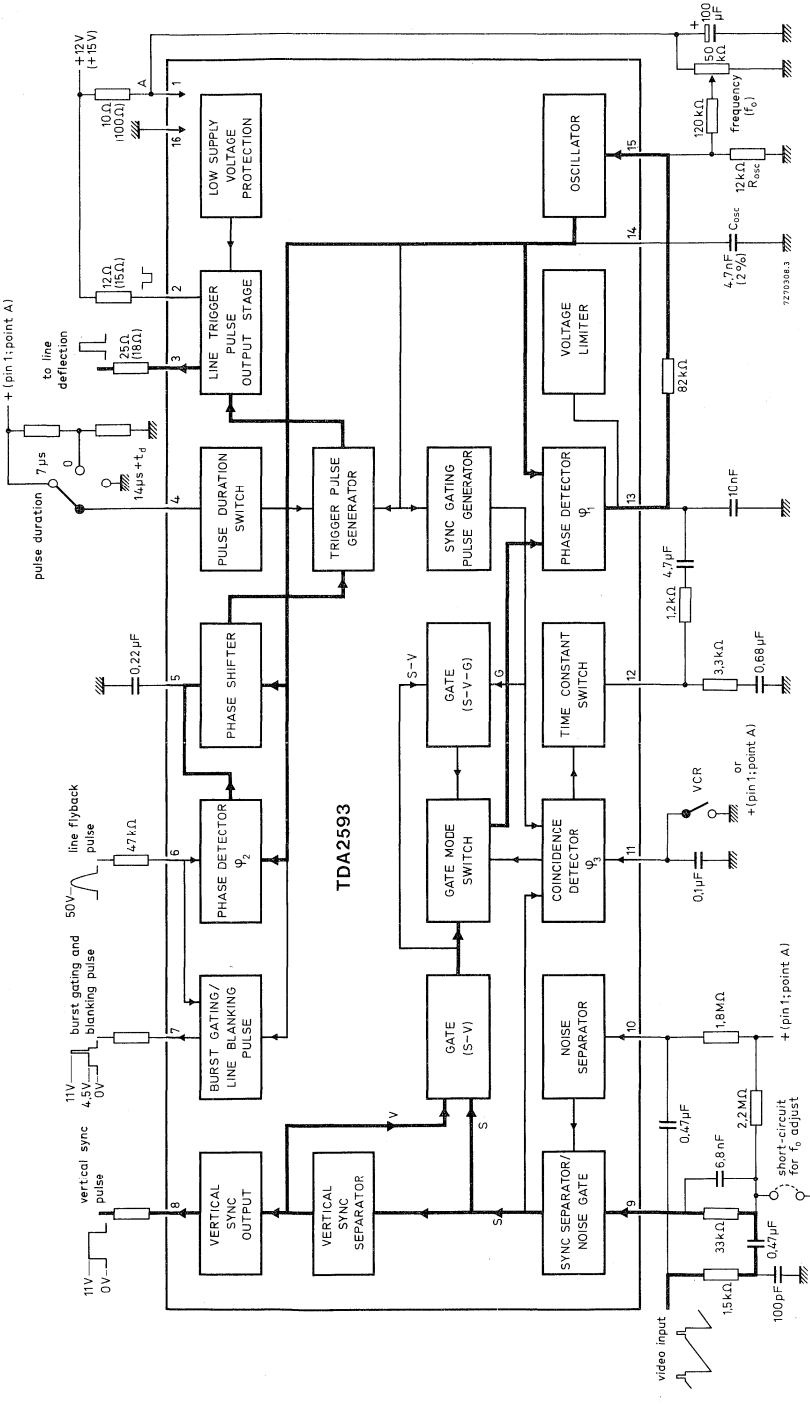


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	V_{1-16}	max.	13,2 V
at pin 2	V_{2-16}	max.	18 V
Voltages			
Pin 4	V_{4-16}	max.	13,2 V
Pin 9	$\pm V_{9-16}$	max.	6 V
Pin 10	$\pm V_{10-16}$	max.	6 V
Pin 11	V_{11-16}	max.	13,2 V
Currents			
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650 mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	10 mA
Pin 11	I_{11}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		0 to + 70 °C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0,8 V
Input keying current	I_9		5 to 100 μA
Input leakage current at $V_{9-16} = -5$ V	I_9	<	1 μA
Input switching current	I_9	⩽	5 μA
Switch off current	I_9	>	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator				
Input switching voltage	$V_{10\text{-}16}$	typ.	1,4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	>	100	μA
		typ.	150	μA
Input leakage current at $V_{10\text{-}16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$	<	7	V
Line flyback pulse				
Input current	I_6	typ.	1	mA
			0,02 to 2	mA
Input switching voltage	$V_{6\text{-}16}$	typ.	1,4	V
Input limiting voltage	$V_{6\text{-}16}$		−0,7 to + 1,4	V
Switching on VCR				
Input voltage	$V_{11\text{-}16}$		0 to 2,5	V
	$V_{11\text{-}16}$		9 to $V_{1\text{-}16}$	V
Input current	$-I_{11}$	<	200	μA
	I_{11}	<	2	mA
Pulse duration switch				
For t = 7 μs (thyristor driving)				
Input voltage	$V_{4\text{-}16}$		9,4 to $V_{1\text{-}16}$	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	$V_{4\text{-}16}$		0 to 3,5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3\text{-}16} = 0$ or input pin 4 open				
Input voltage	$V_{4\text{-}16}$		5,4 to 6,6	V
Input current	I_4	typ.	0	μA

* Permissible range 1 to 7 V.

Vertical sync pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	>	10	V
		typ.	11	V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on}	μs
Burst gating pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	>	10	V
		typ.	11	V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7\text{-}16} = 7$ V	t_p	typ.	4	μs
			3,7 to 4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16} = 7$ V	t	typ.	2,65	μs
			2,15 to 3,15	μs
Output trailing edge current	I_7	typ.	2	mA
Line flyback-blanking pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5	V
Output resistance	R_7	typ.	70	Ω
Output trailing edge current	I_7	typ.	2	mA
Line drive pulse (positive-going)				
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10,5	V
Output resistance				
for leading edge of line pulse	R_3	typ.	2,5	Ω
for trailing edge of line pulse	R_3	typ.	20	Ω
Pulse duration (thyristor driving) $V_{4\text{-}16} = 9{,}4$ to $V_{1\text{-}16}$ V	t_p	typ.	7	μs
			5,5 to 8,5	μs
Pulse duration (transistor driving) $V_{4\text{-}16} = 0$ to 4 V; $t_{fp} = 12$ μs	t_p		$14 + t_d$	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4	V
Overall phase relation				
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2,6	μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	<	0,7	μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration $t_{fp} = 12$ μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	$V_{14\text{-}16}$	typ.	4,4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7,6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0,05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	$V_{13\text{-}16}$		3,8 to 8,2	V
Control current (peak value)	$\pm I_{13M}$		1,9 to 2,3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	<	1	μA
Output resistance at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

Phase comparison φ_2 and phase shifter

Control voltage range	$V_{5\text{-}16}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance				
at $V_{5\text{-}16}$ = 5,4 to 7,6 V			high ohmic	*
at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V	R_5	typ.	8	kΩ
Input leakage current				
$V_{5\text{-}16}$ = 5,4 to 7,6 V	I_5	<	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	<	15	μs
Static control error	$\Delta t/\Delta t_d$	<	0,2	%

Coincidence detector φ_3

Output voltage	$V_{11\text{-}16}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{11M}	typ.	0,1	mA
with coincidence	$-I_{11M}$	typ.	0,5	mA

Time constant switch

Output voltage	$V_{12\text{-}16}$	typ.	6	V
Output current (limited)	$\pm I_{12}$	<	1	mA
Output resistance				
at $V_{11\text{-}16}$ = 2,5 to 7 V	R_{12}	typ.	0,1	kΩ
at $V_{11\text{-}16} < 1{,}5$ V or > 9 V	R_{12}	typ.	60	kΩ

Internal gating pulse

Pulse duration	t_p	typ.	7,5	μs

* Current source.

HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers.
The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1-18} = V_S$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{11-18(p-p)}$	typ.	3 V*
Noise separator input voltage (peak-to-peak value)	$V_{12-18(p-p)}$	typ.	3 V*
Pulse duration switch input voltage			
at t = 14 μs + t_d (transistor driving)	V_{4-18}		0 to 3,5 V
at t = 0 ($V_{3-18} = 0$); input 4 open ($I_4 = 0$)	V_{4-18}		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to-peak value)	$V_{8-18(p-p)}$	typ.	11 V
Burst key output pulse (peak-to-peak value)	$V_{7-18(p-p)}$	typ.	11 V
Line drive-pulse (peak-to-peak value)	$V_{3-18(p-p)}$	typ.	10 V

* Permissible range: 1 to 7 V.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

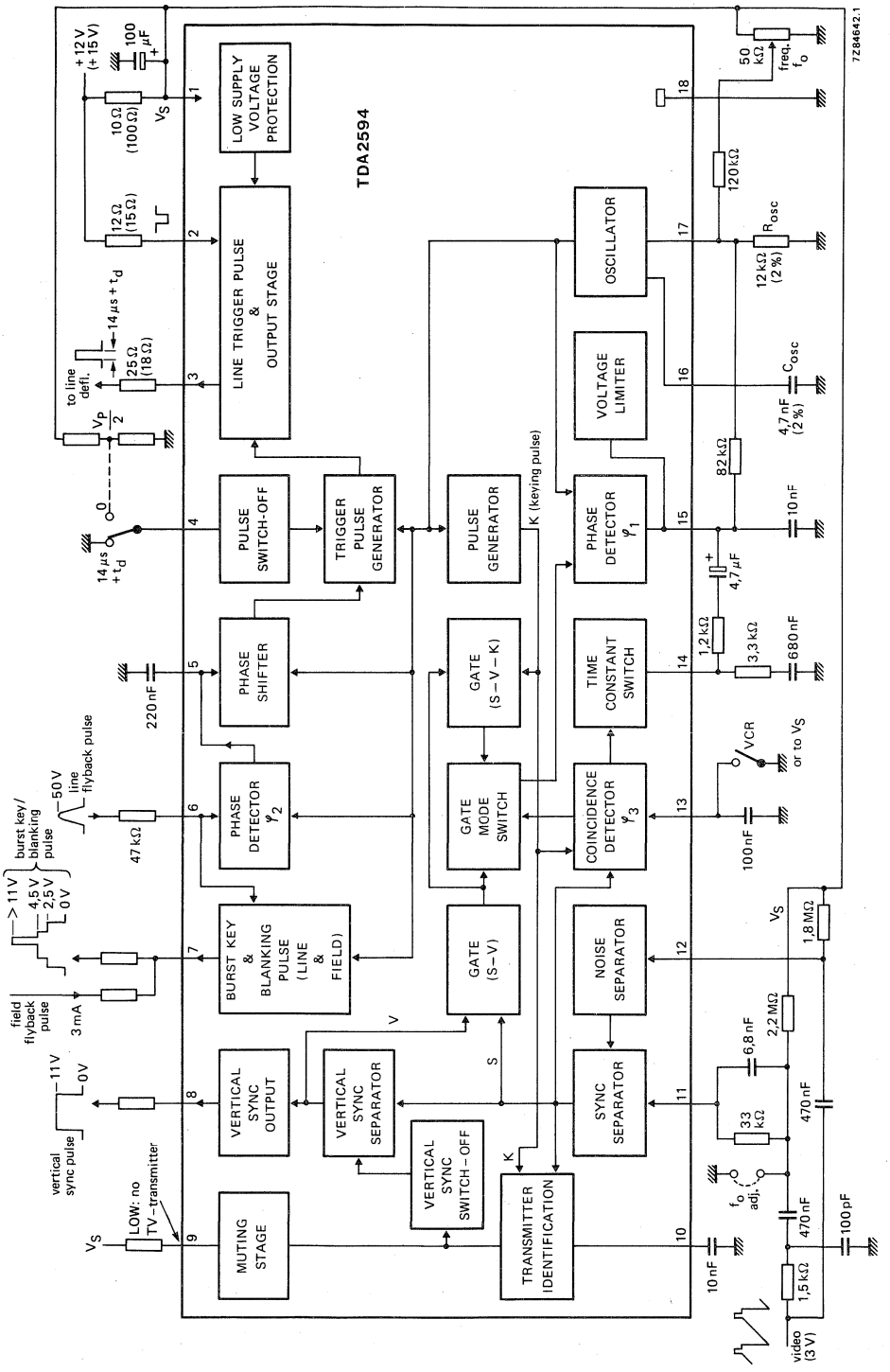


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	$V_{1-18} = V_S$	max.	13,2 V
at pin 2	V_{2-18}	max.	18 V
Voltages			
Pin 4	V_{4-18}	max.	13,2 V
Pin 9	V_{9-18}	max.	18 V
	$-V_{9-18}$	max.	0,5 V
Pin 11	$\pm V_{11-18}$	max.	6 V
Pin 12	$\pm V_{12-18}$	max.	6 V
Pin 13	V_{13-18}	max.	13,2 V
Currents			
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	5 mA
Pin 9	I_9	max.	10 mA
Pin 13	I_{13}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}		−25 to + 125 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

CHARACTERISTICS at $V_{1-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator (pin 11)

Input switching voltage	V_{11-18}	typ.	0,8 V
Input keying current	I_{11}		5 to 100 μA
Input leakage current at $V_{11-18} = -5$ V	I_{11}	⩽	1 μA
Input switching current	I_{11}	⩽	5 μA
Switch off current	I_{11}	⩾	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{11-18(p-p)}$		3 to 4 V*

* Permissible range 1 to 7 V.

Noise separator (pin 12)			
Input switching voltage	V_{12-18}	typ.	1,4 V
Input keying current	I_{12}		5 to 100 μA
Input switching current	I_{12}	⩾	100 μA
		typ.	150 μA
Input leakage current at $V_{12-18} = -5$ V	I_{12}	⩽	1 μA
Input signal (peak-to-peak value)	$V_{12-18(p-p)}$		3 to 4 V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12-18(p-p)}$	⩽	7 V
Line flyback pulse (pin 6)			
Input current	I_6	⩾	0,02 mA
		typ.	1 mA
Input switching voltage	V_{6-18}	typ.	1,4 V
Input limiting voltage	V_{6-18}		−0,7 to +1,4 V
Switching on VCR (pin 13)			
Input voltage	V_{13-18}		0 to 2,5 V
	or: V_{13-18}		9 to V_S V
Input current	$-I_{13}$	⩽	200 μA
	or: I_{13}	⩽	2 mA
Pulse switching off (pin 4)			
For t = 0; input pin 4 open or $V_{3-18} = 0$			
Input voltage	V_{4-18}		5,4 to 6,6 V
Input current	I_4	typ.	0 μA
Vertical sync pulse (positive-going) (pin 8)			
Output voltage (peak-to-peak value)	$V_{8-18(p-p)}$	⩾	10 V
		typ.	11 V
Output resistance	R_8	typ.	2 kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	⩾	t_{on} μs
Switching off the vertical sync pulse	V_{10-18}	⩽	3 V
Burst key pulse (positive-going) (pin 7)			
Output voltage	V_{7-18}	⩾	10 V
		typ.	11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7-18} = 7$ V	t_p	typ.	4 μs
			3,7 to 4,3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7$ V	t	typ.	2,65 μs
			2,15 to 3,15 μs
Output trailing edge current	I_7	typ.	2 mA
Saturation voltage during line scan	V_{7-18}	⩽	1 V

* Permissible range 1 to 7 V.

Line flyback-blanking pulse (positive-going) (pin 7)

Output voltage	V_{7-18}		4,1 to 4,9 V
Output resistance	R_7	typ.	70 Ω
Output trailing edge current	I_7	typ.	2 mA

Field flyback/blanking pulse (pin 7)

Output voltage with externally forced in current I_7 = 2,4 to 3,6 mA	V_{7-18}		2 to 3 V
Output resistance at I_7 = 3 mA	R_7	typ.	70 Ω

TV-transmitter identification output (pin 9; open collector)

Output voltage at I_9 = 3 mA; no TV-transmitter	V_{9-18}	⩽	0,5 V
Output resistance at I_9 = 3 mA; no TV-transmitter	R_9	⩽	100 Ω
Output current at $V_{10-18} \geqslant 3$ V; TV-transmitter identified	I_9	⩽	5 μA

TV-transmitter identification (pin 10)

When receiving a TV signal the voltage V_{10-18} will change from ⩽ 1 V to ⩾ 7 V.

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3-18(p-p)}$	typ.	10 V
Output resistance			
for leading edge of line pulse	R_3	typ.	2,5 Ω
for trailing edge of line pulse	R_3	typ.	20 Ω
Pulse duration (transistor driving) V_{4-18} = 0 to 3,5 V; $-I_4 \geqslant 200$ μA; t_{fp} = 12 μs	t_p		$14 + t_d$ μs*
Supply voltage for switching off the output pulse	V_{1-18}	typ.	4 V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ.	2,6 ± 0,7 μs**

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	$\Delta I/\Delta t$	typ.	30 μA/μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration t_{fp} = 12 μs.

Oscillator (pins 16 and 17)				
Threshold voltage low level	$V_{16\text{-}18}$	typ.	4,4	V
Threshold voltage high level	$V_{16\text{-}18}$	typ.	7,6	V
Charging current	$\pm I_{16}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	Δf_o	⩽	± 5	%▲
Frequency control sensitivity	$\Delta f_o/\Delta_{17}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf_o	typ.	± 10	%
Influence of supply voltage on frequency; reference at V_S = 12 V	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	⩽	± 0,05	%▲
Change of frequency when V_S drops to 5 V; reference at V_S = 12 V	Δf_o	⩽	± 10	%▲
Temperature coefficient of oscillator frequency	TC	⩽	$\pm 10^{-4}$	K^{-1}▲
Phase comparison φ_1 (pin 15)				
Control voltage range	$V_{15\text{-}18}$		4,1 to 7,9	V
Control current (peak value)	$\pm I_{15M}$		1,8 to 2,2	mA
Output leakage current at $V_{15\text{-}18}$ = 4,3 to 7,7 V	I_{15}	⩽	1	μA
Output resistance				
at $V_{15\text{-}18}$ = 4,3 to 7,7 V	R_{13}	high ohmic		*
at $V_{15\text{-}18}$ ⩽ 4,1 V or ⩾ 7,9 V	R_{13}	low ohmic		**
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680	Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12	%▲
Phase comparison φ_2 **and phase shifter** (pin 5)				
Control voltage range	$V_{5\text{-}18}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance at $V_{5\text{-}18}$ = 5,4 to 7,6 V	R_5	high ohmic		*
Input leakage current at $V_{5\text{-}18}$ = 5,4 to 7,6 V	I_5	⩽	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	⩽	15,5	μs
Static control error	$\Delta t/\Delta t_d$	⩽	0,2	%
Coincidence detector φ_3 (pin 13)				
Output voltage	$V_{13\text{-}18}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{13M}	typ.	0,1	mA
with coincidence	$-I_{13M}$	typ.	0,5	mA

* Current source.
** Emitter follower.
▲ Excluding external component tolerances.

Time constant switch (pin 14)

Output voltage	$V_{14\text{-}18}$	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13\text{-}18} = 3{,}5$ to 7 V	R_{14}	typ.	0,1 kΩ
at $V_{13\text{-}18} \leqslant 2{,}5$ V or $\geqslant 9$ V	R_{14}	typ.	60 kΩ

Internal keying pulse

Pulse duration	t_p	typ.	7,5 μs

HORIZONTAL COMBINATION

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

Features

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	typ.	50 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

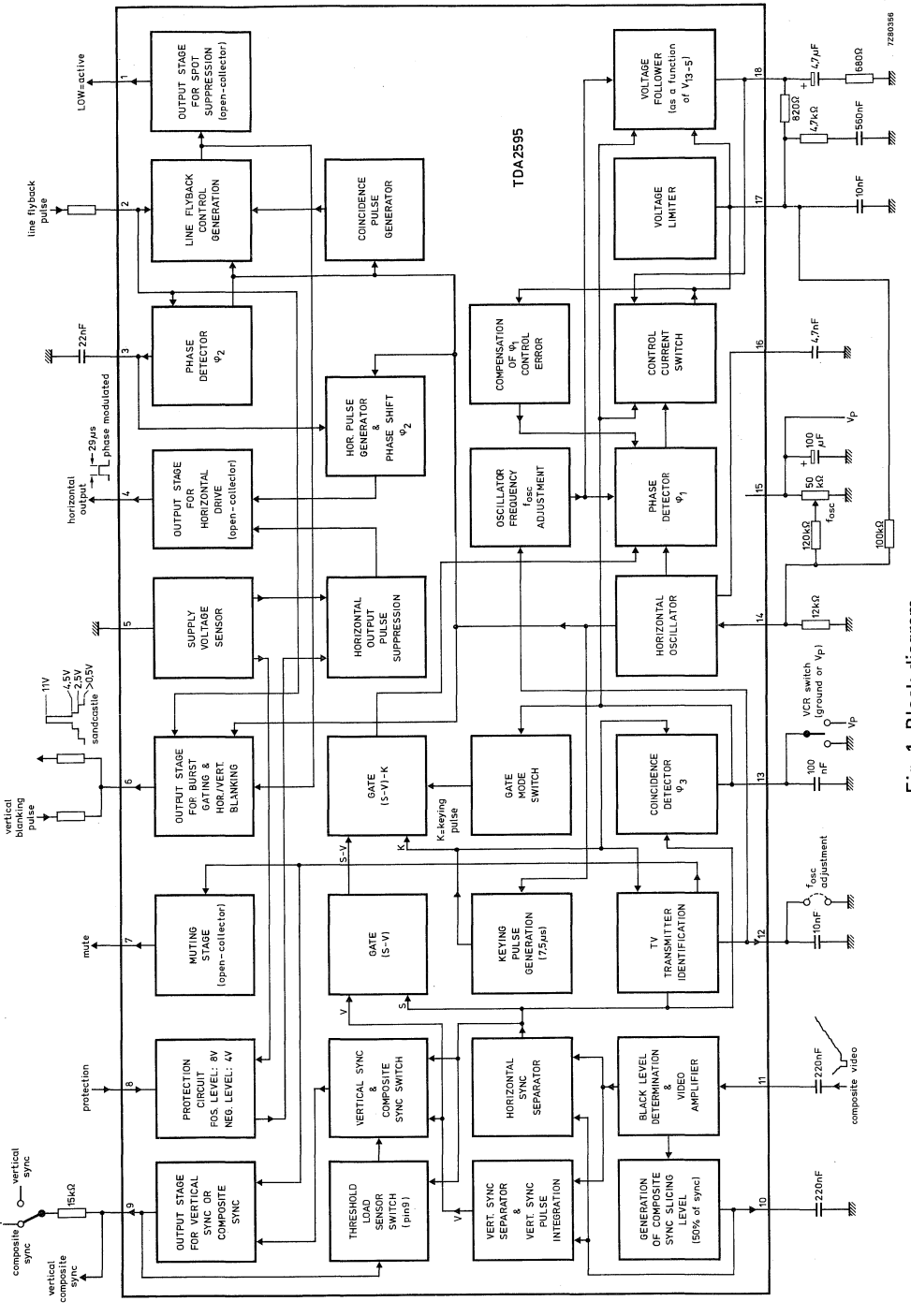


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0,5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	25	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude for $V_{11\text{-}5(p\text{-}p)} < 1{,}5$ V					
Capacitor current during:					
video	I_{10}	–	16	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
discharging	$+I_{16}$	–	1024	–	μA
charging	$-I_{16}$	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 50 mA	V_{4-5}	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V
Hysteresis for switching on the output pulse	ΔV_P	–	250	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3,55	–	8,3	V
Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9{,}5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	$\pm\Delta f_{osc}$	–	680	–	Hz
spread of catching and holding range	$\pm\Delta f_{osc}$	–	10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9,5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9,5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0{,}5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison and flyback control	V_{2-5}	–	3	–	V
Switching level for horizontal blanking	V_{2-5}	–	0,3	–	V
Input voltage limiting	V_{2-5}	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Maximum negative input current	$-I_2$	–	–	500	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2,6 ± 0,7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3	$\Delta I/\Delta t$	–	30	–	$\mu A/\mu s$
Burst gating pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4,1	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6) (note 3)					
Output voltage at I_6 = 2,8 mA	V_{6-5}	2,15	2,5	3	V
Minimum output current at $V_{6-5} > 2{,}15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12) (note 4)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at $I_7 = 3$ mA no TV transmitter	V_{7-5}	–	–	0,5	V
Output resistance at $I_7 = 3$ mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0,8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0,4	–	V
Current limiting for $V_{8-5} = 1$ to 8,5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8,5$ V	R_{8-5}	–	3	–	kΩ
Internal response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; $I_1 = 3$ mA	V_{1-5sat}	–	–	0,5	V
Output leakage current in case of disturbance of line flyback pulse	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_P the vertical output is active independent of synchronization state.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

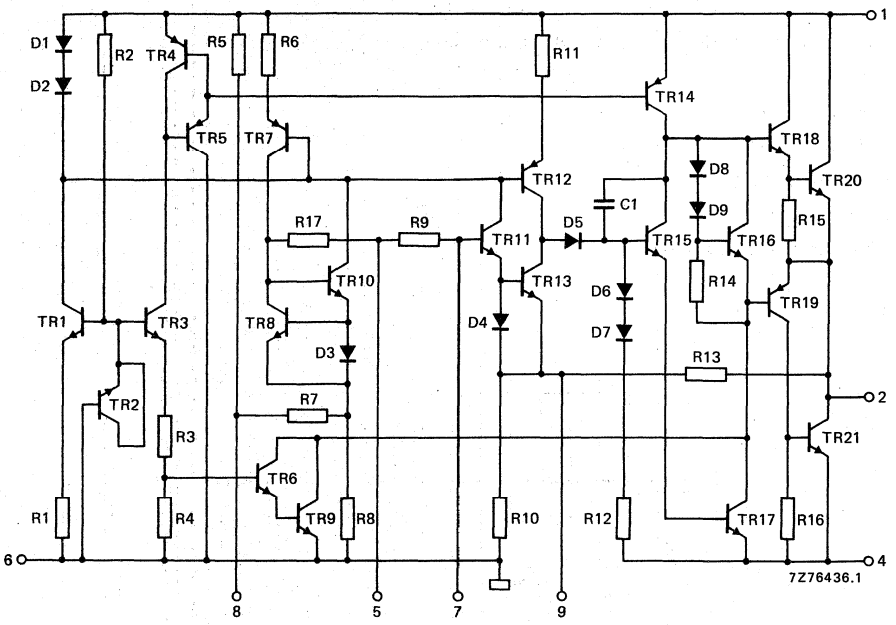


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C

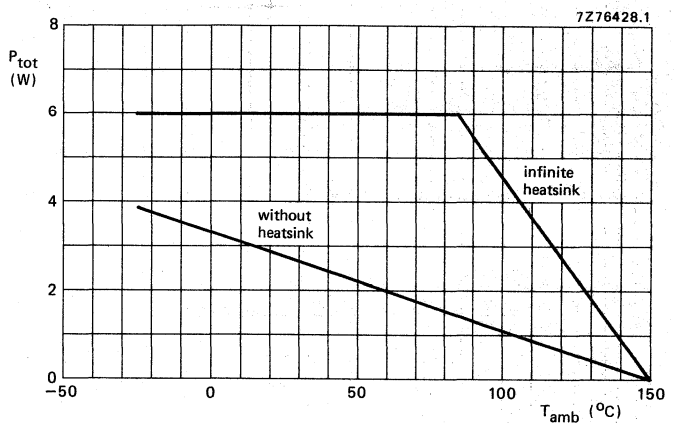


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

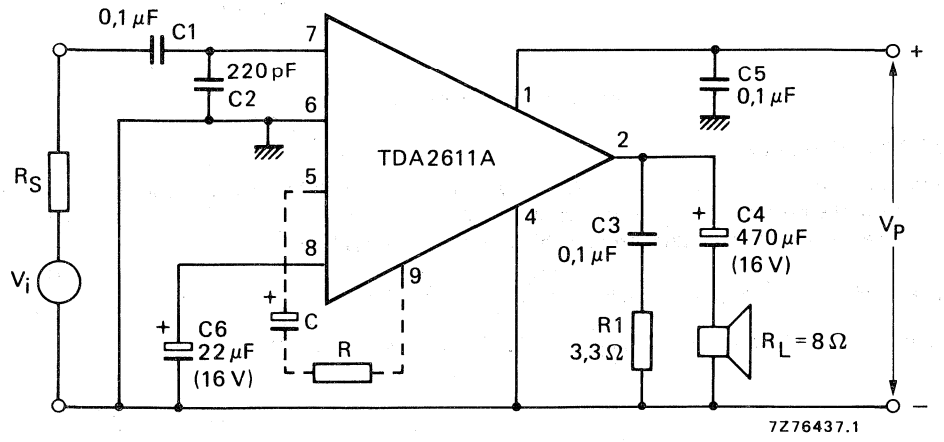


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

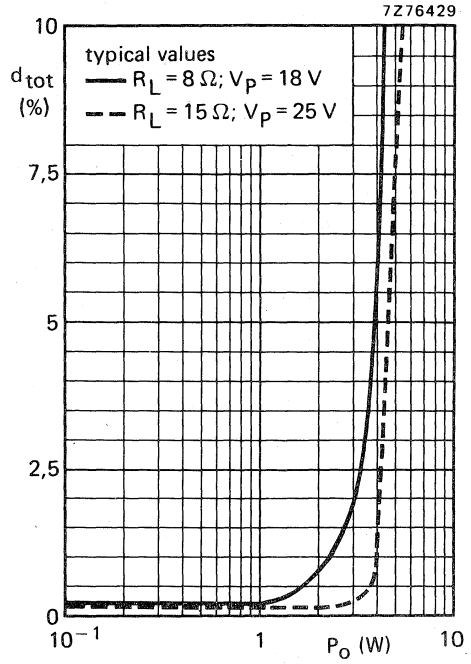


Fig. 4 Total harmonic distortion as a function of output power.

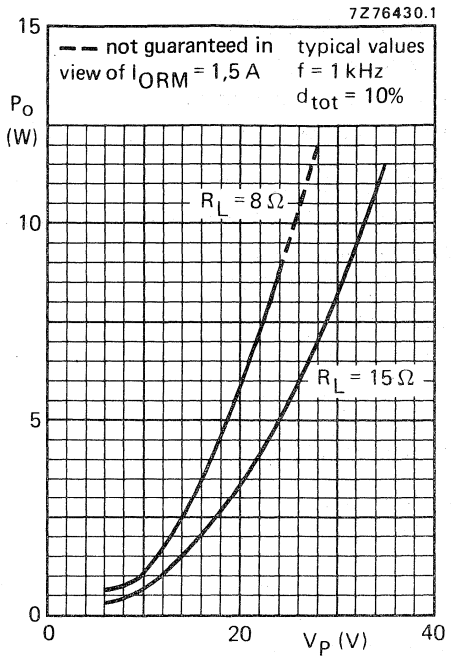


Fig. 5 Output power as a function of supply voltage.

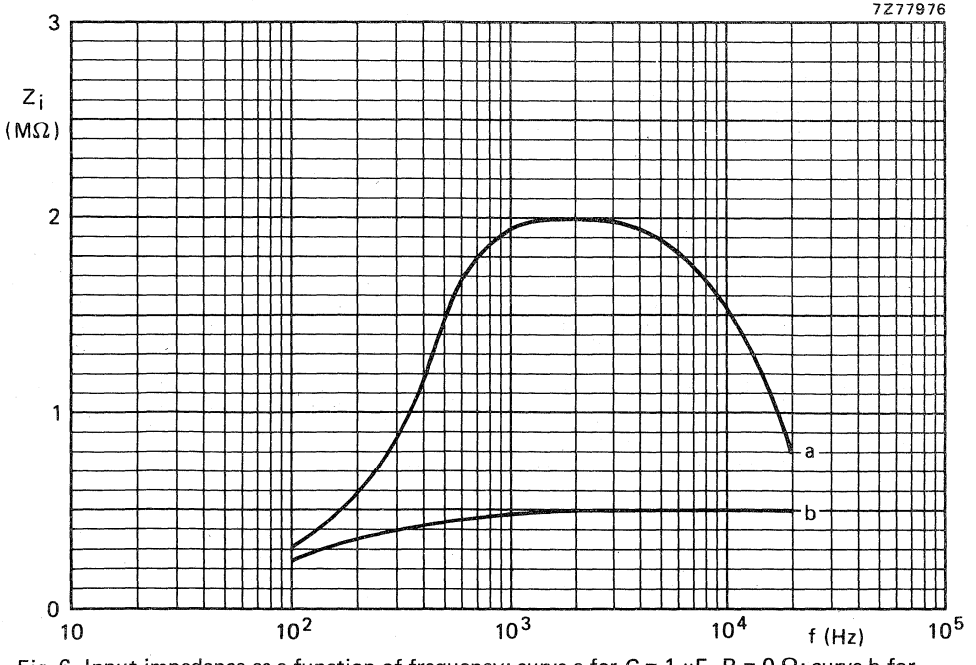


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

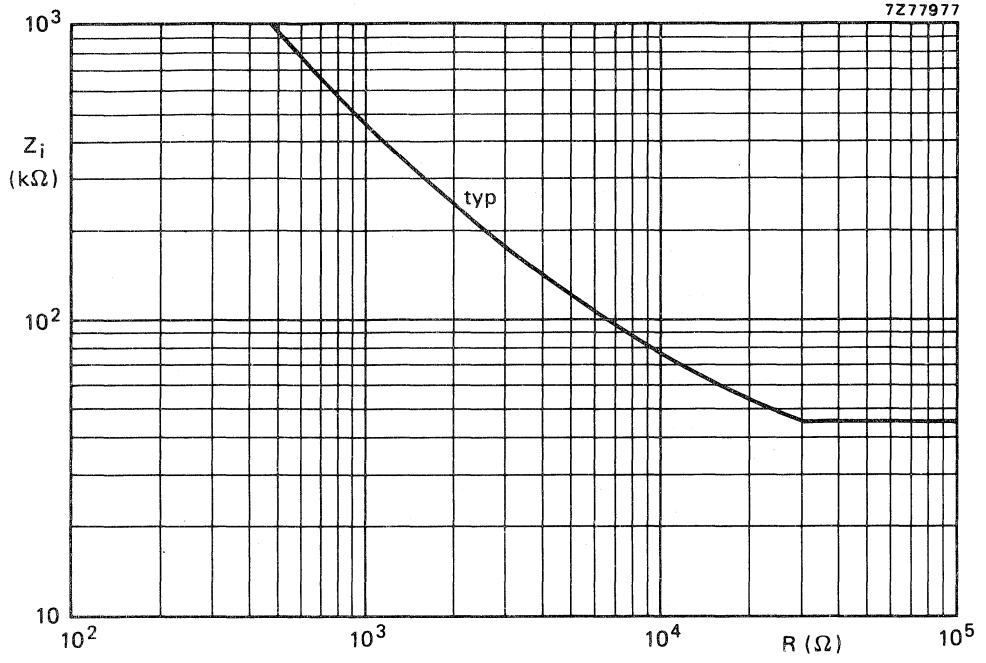


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

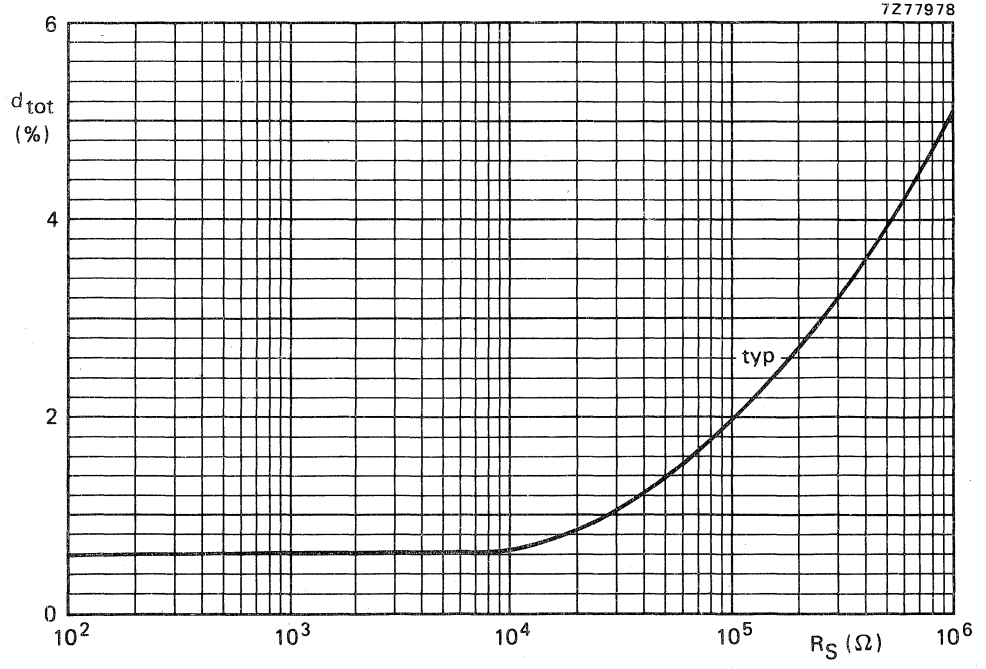


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

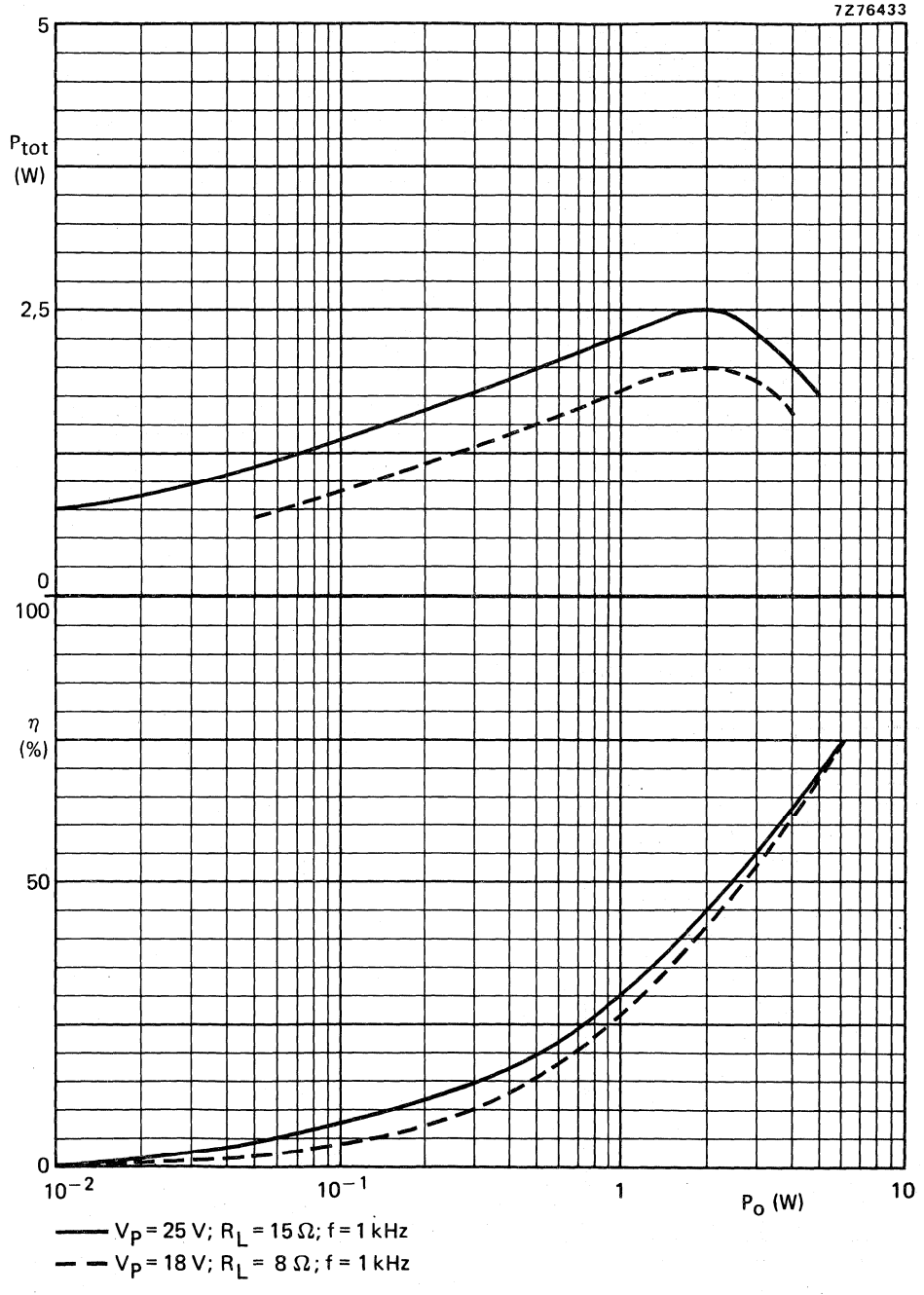


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

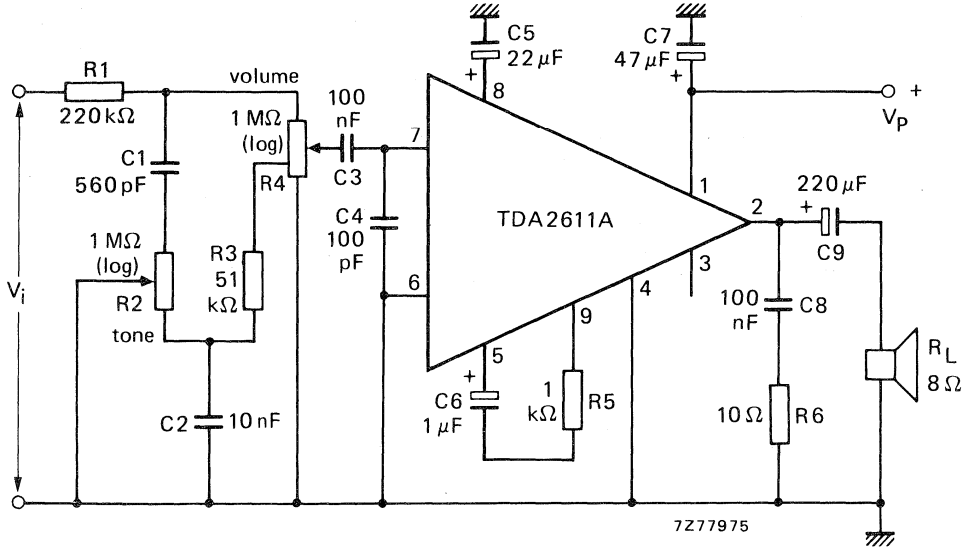


Fig. 10 Ceramic pickup amplifier circuit.

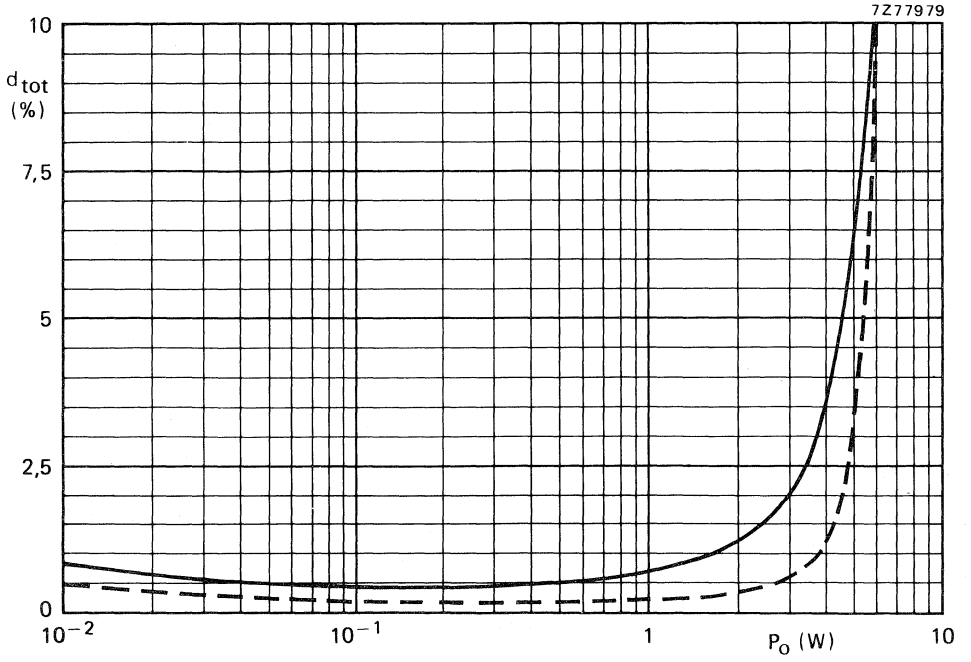


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

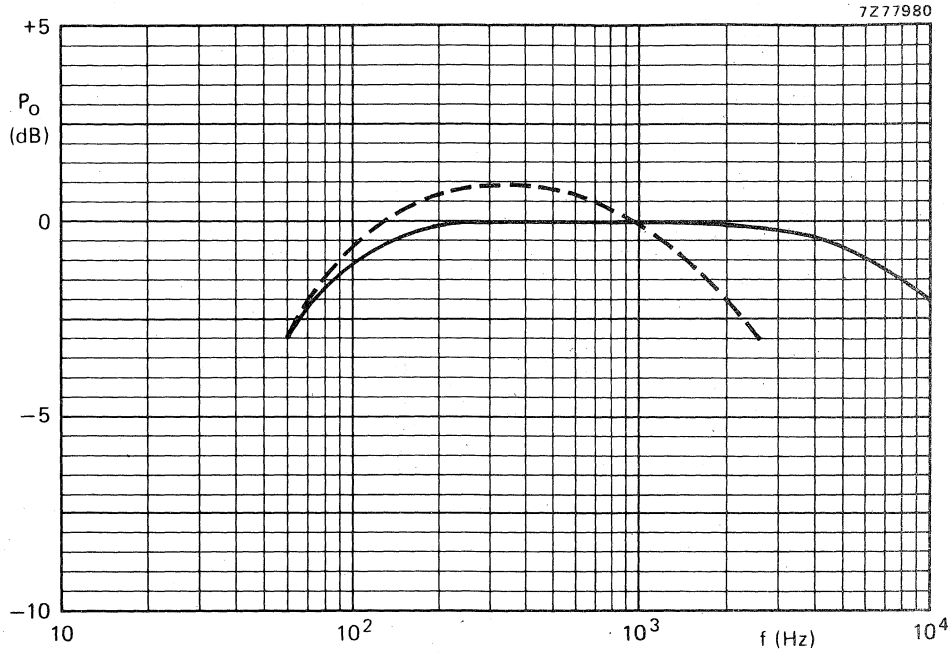


Fig. 12 Frequency characteristics of the circit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_O relative to 0 dB = 3 W; typical values.

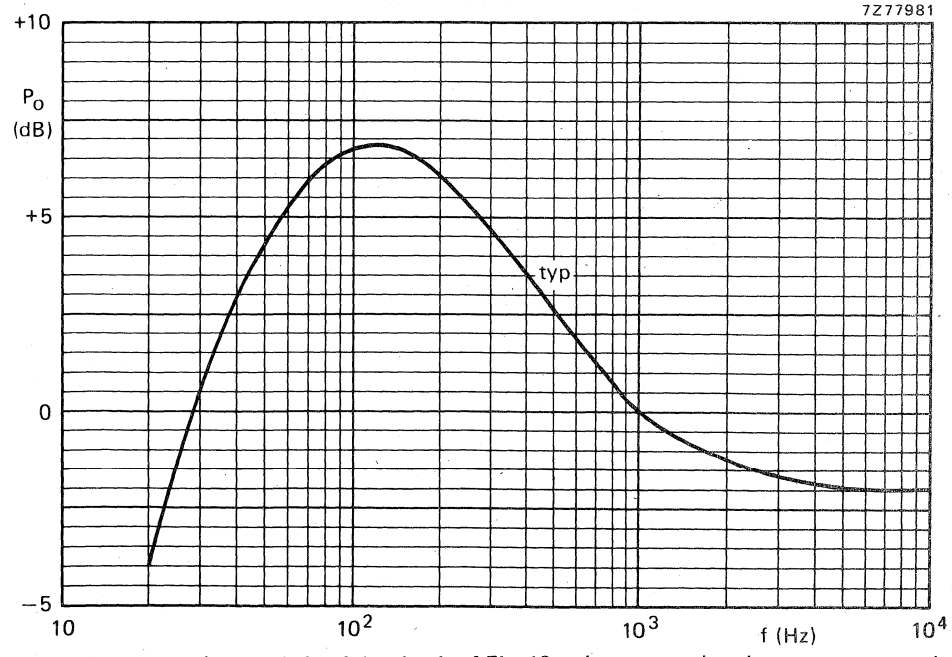


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40 V
Output power at THD = 0,5%, V_P = 24 V	P_O	typ.	6 W
Voltage gain	G_V	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 μV

PACKAGE OUTLINE

TDA2613: 9-lead SIL; plastic power (SOT-110B).

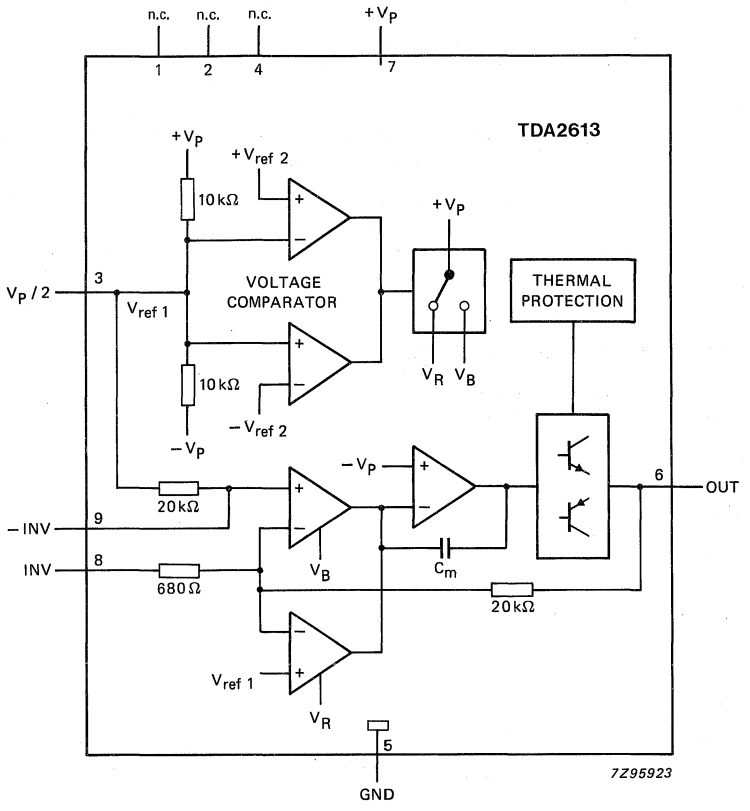


Fig. 1 Block diagram.

PINNING

1.	n.c.	not connected	5.	GND	ground (asymmetrical) / negative supply (symmetrical)
2.	n.c.	not connected	6.	OUT	output
3.	$V_P/2$	½ V_P (asymmetrical) / ground (symmetrical)	7.	+V_P	positive supply
4.	n.c.	not connected	8.	INV	inverting input
			9.	−INV	non-inverting input

FUNCTIONAL DESCRIPTION

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 4, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	40	V
Non-repetitive peak output current		I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	t_{sc}	–	1	hour

Note to the Ratings

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_S) ≥ 4 Ω, the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to V_P = ± 20 V.

DEVELOPMENT DATA

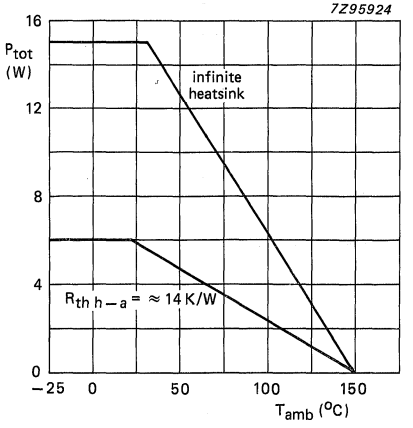


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c} = 8$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = 24$ V, the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h\text{-}a} = \frac{150 - 60}{4{,}1} - 8 \approx 14\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

DEVELOPMENT DATA

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	15	24	40	V
input mute mode		V_P	4	–	10	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to Vp/2	V_{os}	–	30	200	mV
Input mute mode: asymmetrical power supply; test circuit as per Fig. 4; V_P = 8 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	5	15	20	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Supply voltage ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to Vp/2	V_{os}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: symmetrical power supply; test circuit as per Fig. 3; $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25\ ^oC$; f = 1 kHz						
Total quiescent current		I_{tot}	10	20	35	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	$P_o = 4$ W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B	–	40 to 16 k	–	Hz
Voltage gain		G_v	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	$R_S = 2\ k\Omega$	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	V_{os}	–	30	200	mV

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ –3 dB.
2. Ripple rejection at $R_S = 0\ \Omega$, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

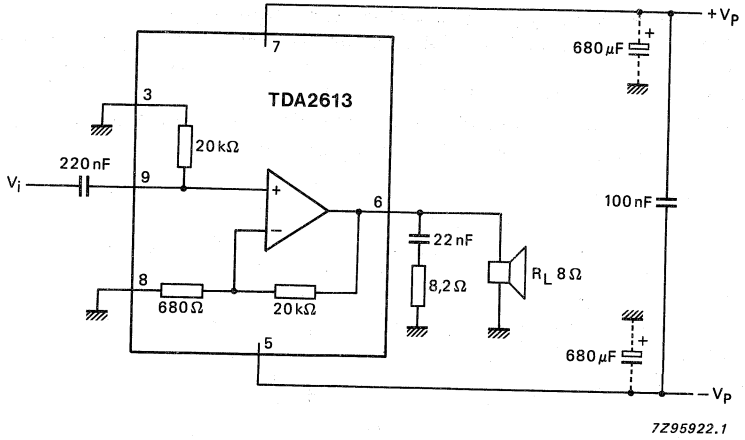


Fig. 3 Test and application circuit; symmetrical power supply.

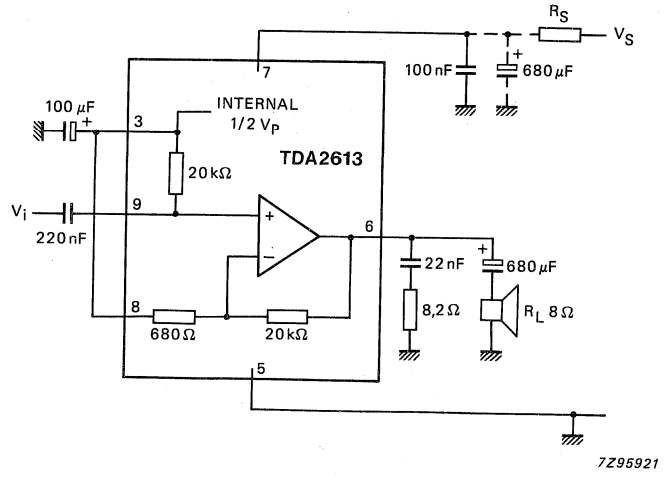


Fig. 4 Test and application circuit; asymmetrical power supply.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 5).

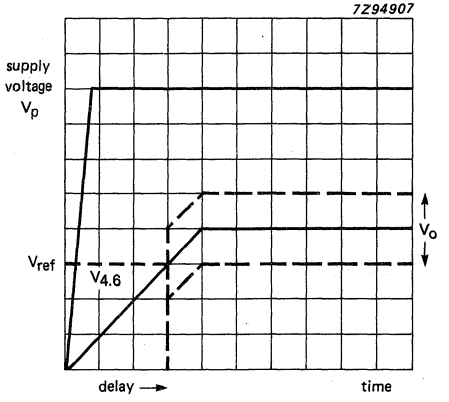


Fig. 5 Input mute circuit; time delay.

VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation
- Synchronization circuit
- Blanking pulse generator with guard circuit
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with thermal and short-circuit protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)*	$I_5 + I_9 = I_S$	typ.	325	mA
Output current (peak-to-peak value)*	$I_{6(p-p)}$	typ.	1,7	A
Maximum output current (peak-to-peak value)	$I_{6(p-p)}$	max.	2,6	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5	K/W

* for 45 AX systems

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT141RGA).

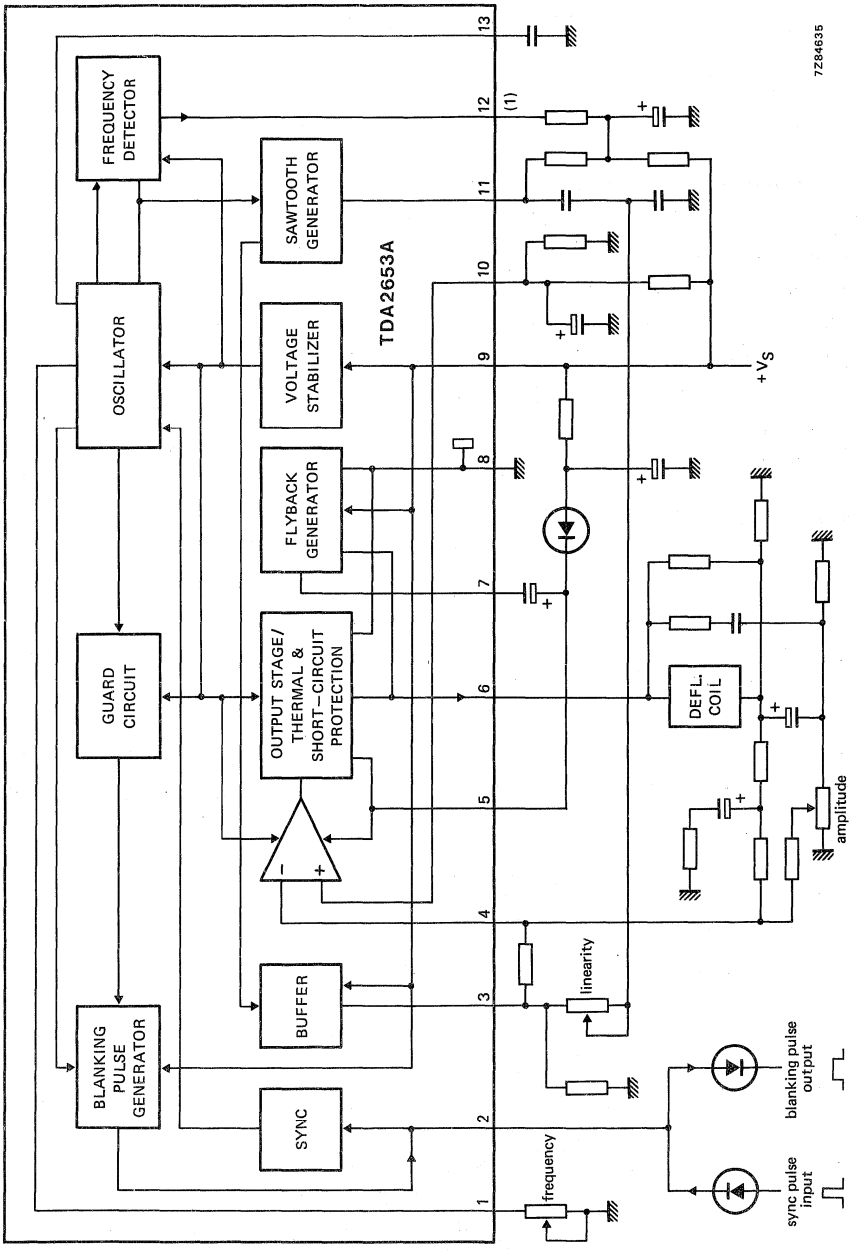


Fig. 1 Block diagram.

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	60 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	60 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1,3 A
	$-I_7$	max.	1,5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting value

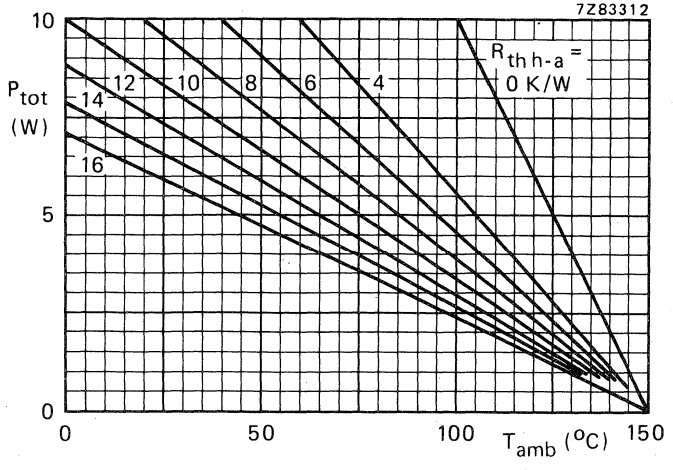


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heat-sink compound is used. $R_{th\ j\text{-}mb} \leq 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage			
at $-I_6$ = 1,1 A	V_{6-8}	⩾	$V_{5-8} - 2,2$ V
		typ.	$V_{5-8} - 1,9$ V
at I_6 = 1,1 A	V_{6-8}	typ.	1,3 V
		⩽	1,6 V
Flyback generator output voltage at $-I_7$ = 1,1 A	V_{7-8}	typ.	$V_S - 2,2$ V
Peak output current	$\pm I_6$	⩽	1,3 A
Flyback generator peak current	$\pm I_7$	⩽	1,3 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0,1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8}		0 to $V_S - 1$ V
	V_{11-8}		0 to $V_S - 2$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾	−2 μA
		⩽	+30 mA
Oscillator temperature dependency			
T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency			
V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage			
at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18,5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1,4 ± 0,07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The DC voltage is proportional to the output voltage (DC feedback). The AC voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (AC feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

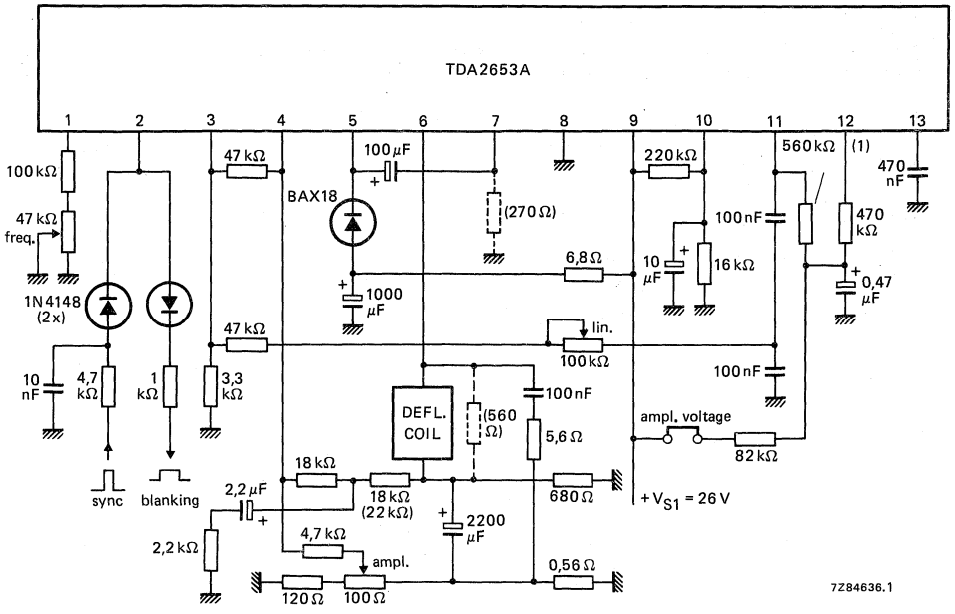
    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

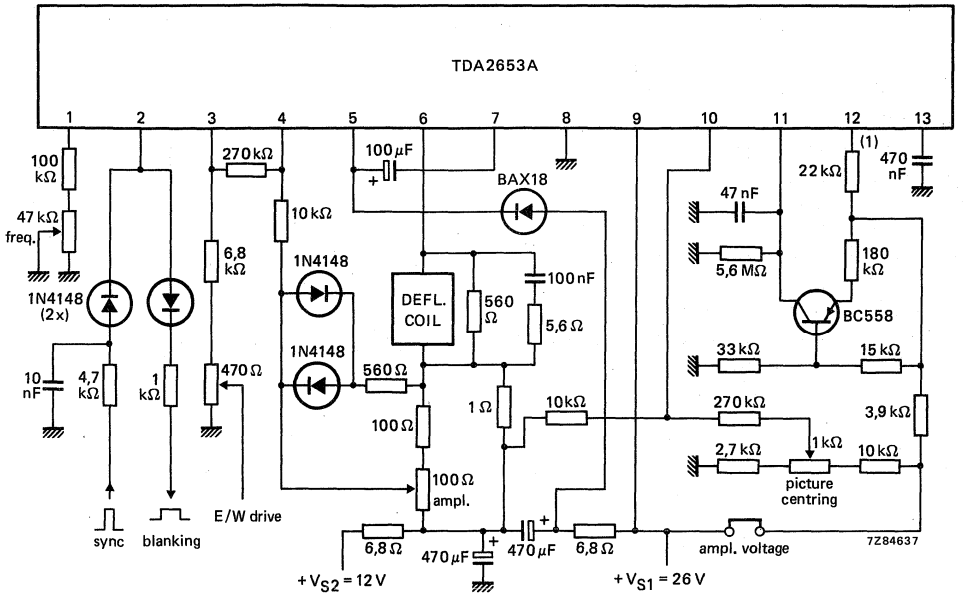
12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 45AX system (26 V).



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 45 AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

QUICK REFERENCE DATA

Supply voltage range (ref. to tab = ground)	V_P		10 to 35	V
Output current (peak-to-peak value)	$I_{9(p-p)}$	max.	2	A
Total power dissipation	P_{tot}	max.	5	W
Operating junction temperature	T_j	max.	150	°C
Thermal resistance from junction to tab	$R_{th\ j\text{-}tab}$	=	12	°C/W

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

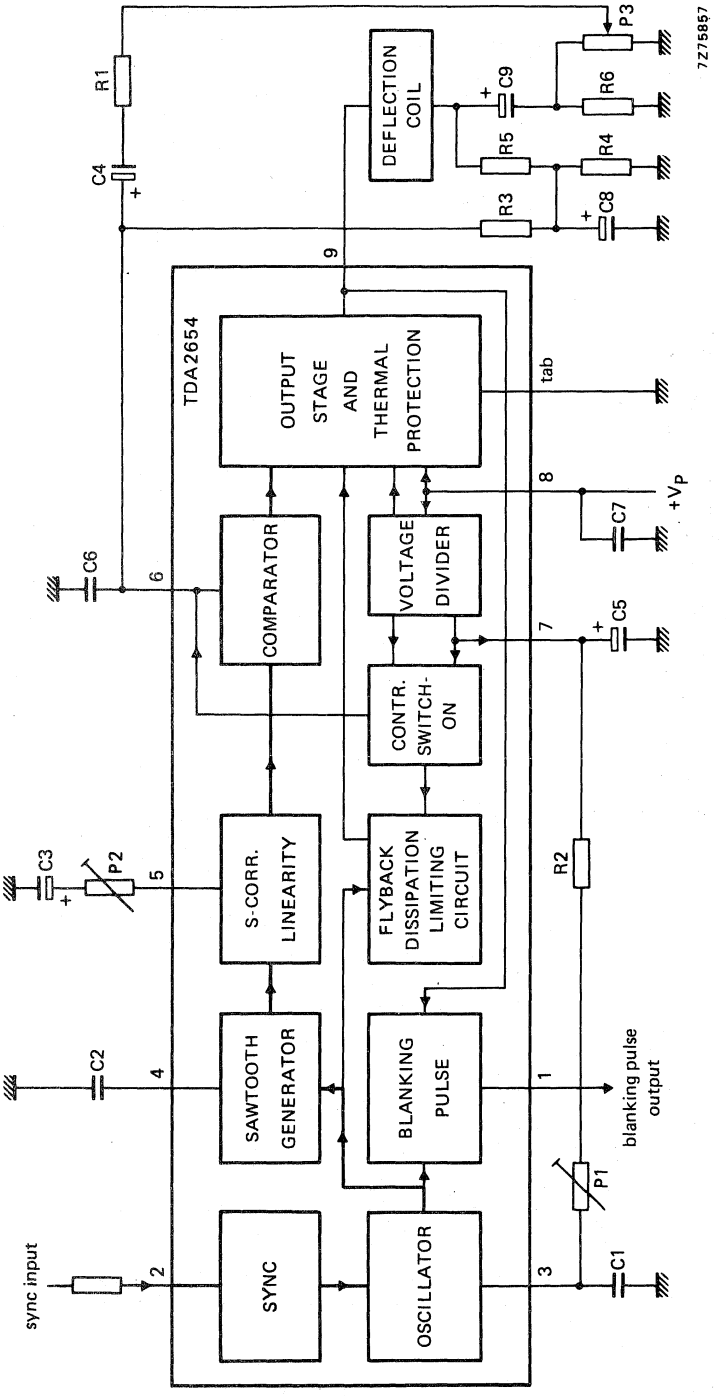


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

Voltages			
Pin 2	V_2	max.	5 V
Pin 3	V_3	max.	17 V
Pin 4	V_4	max.	17 V
Pin 5	V_5	max.	6 V
Pin 6	V_6	max.	13 V
Pin 7	V_7	max.	18 V
Pin 8	V_8 (V_P)	max.	35 V
Currents			
Pin 1	$+I_1$	max.	1 mA
	$-I_1$	max.	5 mA
Pin 2	I_2	max.	2,5 mA
Pin 3	I_3	max.	30 mA
Pin 4	I_4	max.	30 mA
Pin 5	$\pm I_5$	max.	1 mA
Pin 6	$\pm I_6$	max.	3 mA
Pin 9 (repetitive)	$\pm I_9$	max.	1 A
Pin 9 (non-repetitive)	$\pm I_9$	max.	1,5 A
Total power dissipation (see also Fig. 2)	P_{tot}	max.	5 W
Storage temperature	T_{stg}	−25 to + 150	°C
Operating junction temperature	T_j	max.	150 °C

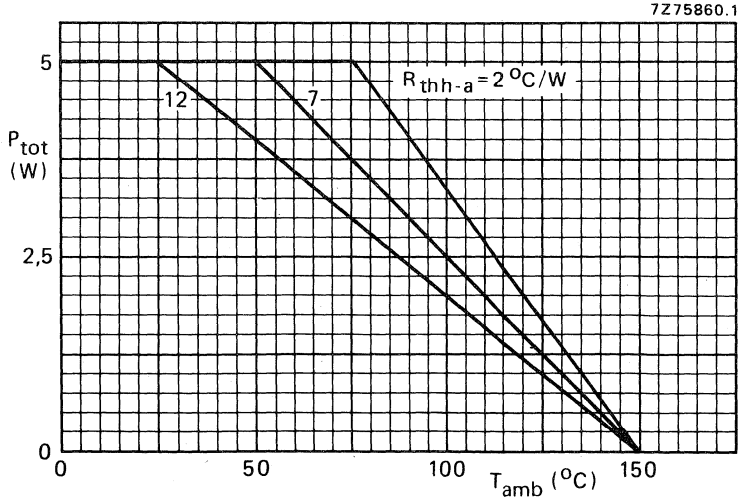


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\ tab-h}$ = 1 °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\ j-tab}$ = 12 °C/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

			monochrome (Fig. 3)	tiny-vision colour (Fig. 4)	
Supply voltage (pin 8)	V_P	typ.	25	31	V
Supply current (pin 8)	I_P	typ.	165	150	mA
Total power dissipation	P_{tot}	typ.	3,1	3,5	W
Output voltage (peak-to-peak value)	$V_{9\,(p\text{-}p)}$	typ.	22	28	V
Blanking pulse; I_1 = 1 mA	V_1	typ.	11,5	14,5	V
Blanking pulse duration	t_p	typ.	1,3	1,4	ms
D.C. input voltage (pin 6)	V_6	typ.	3,4	4,4	V
Deflection current (peak-to-peak value)	$I_{9\,(p\text{-}p)}$	typ.	1,1	0,92	A
Flyback time	t	typ.	1,3	1,32	ms
Free running oscillator frequency	f_{osc}	typ.	46	46	Hz
Oscillator thermal drift		typ.	−0,01	−0,01	Hz/°C
Oscillator voltage shift		typ.	−0,13	−0,12	Hz/V
Tracking range oscillator		typ.	18	18	%
Synchronization input voltage	V_2	>	1	1	V
Voltage divider ratio	V_7/V_8	typ.	0,52	0,52	
Input resistance pin 7	R_7	typ.	2,8	2,8	kΩ
Recommended thermal resistance of heatsink for T_{amb} up to 70 °C	$R_{th\ h\text{-}a}$	<	13	10	°C/W

PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

APPLICATION INFORMATION (see also Fig. 1)

The function is described against the corresponding pin number

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

APPLICATION INFORMATION (continued)

3. Oscillator

The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 μF will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 μF. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

The value depends on the deflection coil.

9. Output

The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

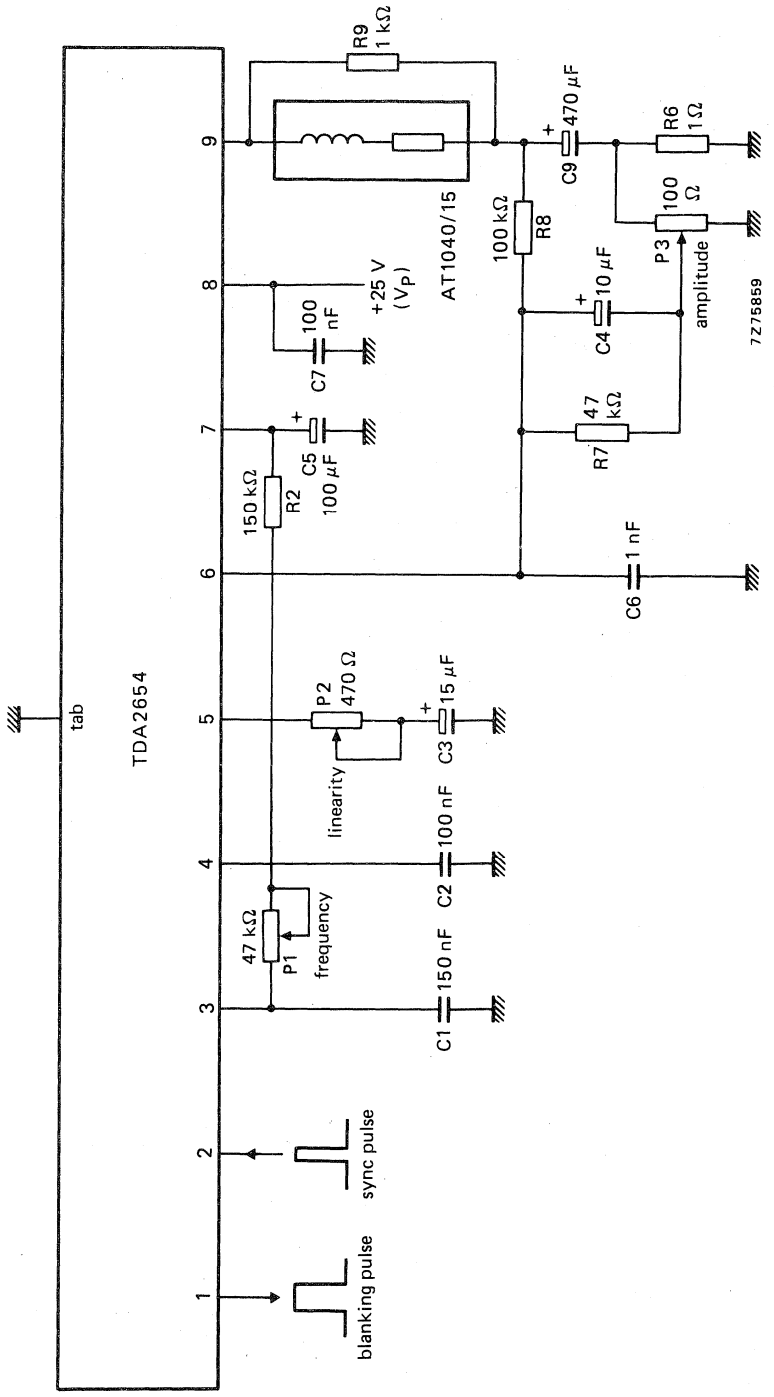
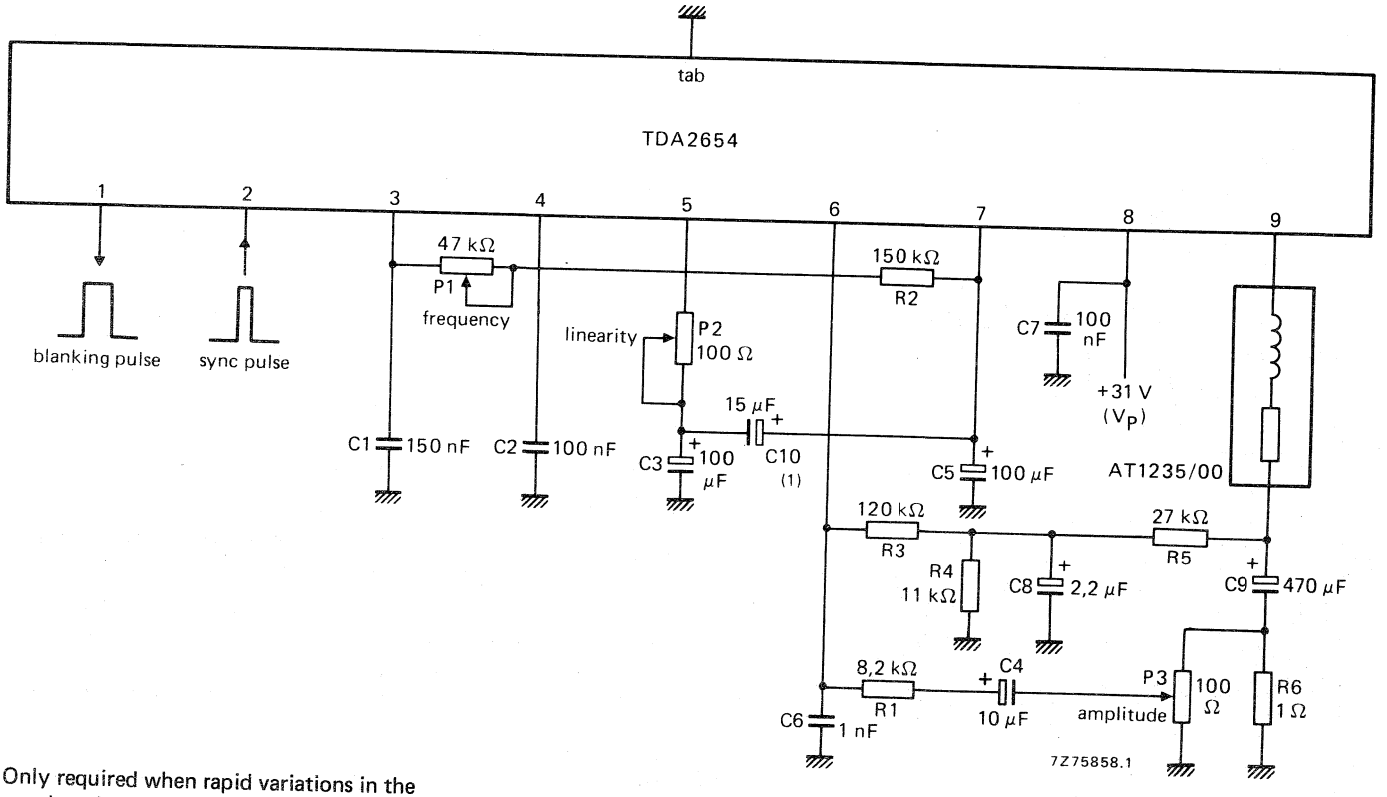


Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)



(1) Only required when rapid variations in the supply voltage are expected.

Fig. 4 Colour 90° vertical deflection system.

VERTICAL DEFLECTION CIRCUIT

GENERAL DESCRIPTION

The TDA2655B is a monolithic integrated circuit for vertical deflection in colour television receivers with 90° picture tubes.

Features

- Synchronization circuit
- Vertical oscillator; 50/60 Hz switch
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with termal and short-circuit protection
- Flyback generator
- Blanking pulse generator with guard circuit
- Voltage stabilizer
- Frequency detector with memory and storage

QUICK REFERENCE DATA

For 90° deflection; measured with respect to cooling fin (ground)

			concept 1*	concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
System supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Deflection current (peak-to-peak value)	$I_{9(p-p)}$	typ.	450	450	mA
Synchronization input voltage (peak-to-peak value)	$V_{5(p-p)}$	min.	1	1	V

*Concept 1: with two supply voltages ; concept 2: with one supply voltage. (See also Figs 2 and 3).

PACKAGE OUTLINE

12-lead DIL; plastic with metal cooling fin (SOT150).

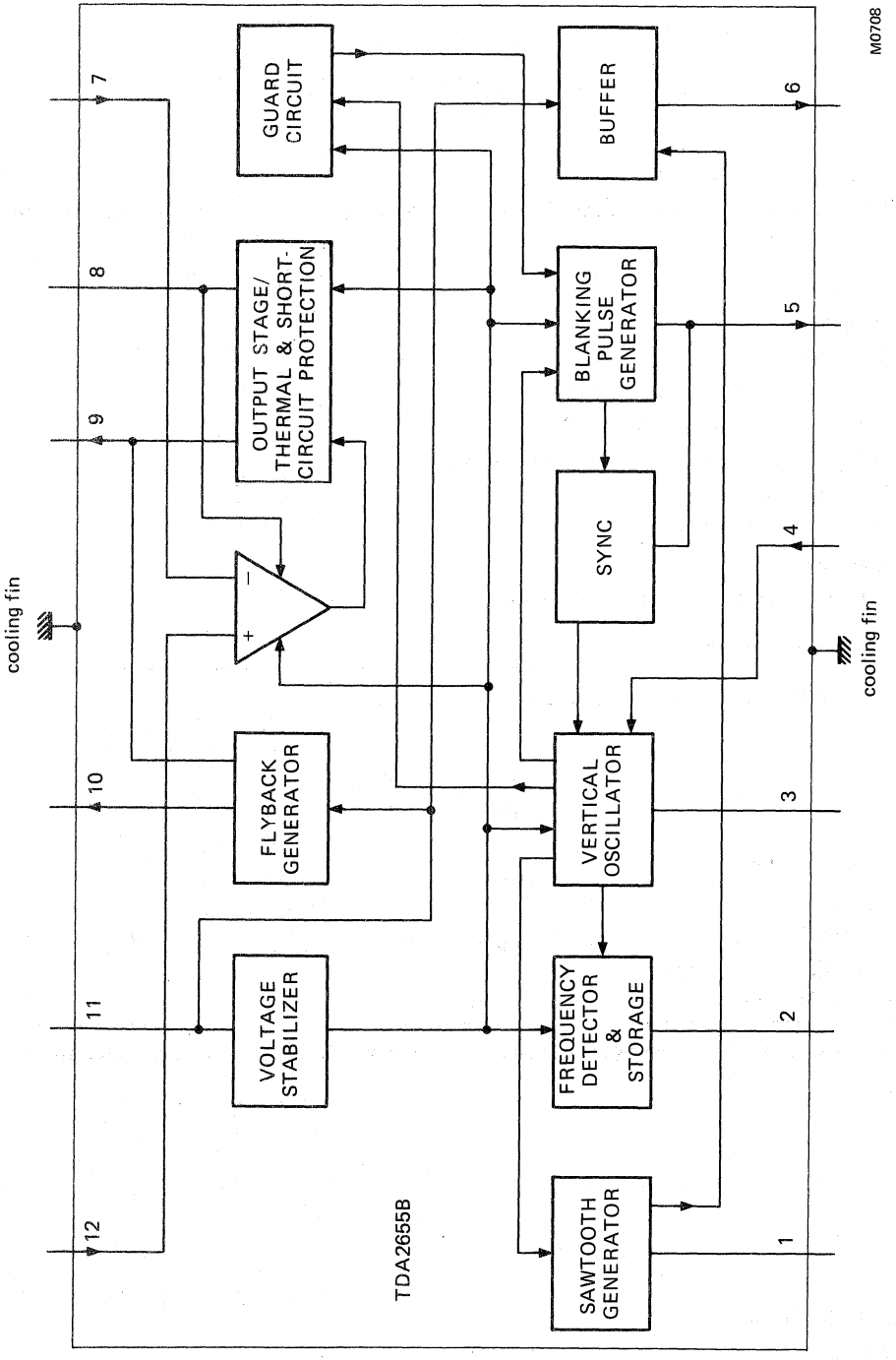


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

with respect to cooling fin (ground)

Supply voltage (pin 11)	$V_{11} = V_P$	max.	40	V
Supply voltage output stage (pin 8)	V_8	max.	60	V
Pin 9	V_9	max.	60	V
	$-V_9$	max.	0	V
Pin 10	V_{10}	max.	40	V
Pin 3	V_3	max.	7	V
Pin 1	V_1	max.	40	V
Pin 6	V_6	max.	7	V
Pins 7 and 12	$V_7; V_{12}$	max.	24	V

Currents

Pin 10	I_{10}	max.	1,2	A
	$-I_{10}$	max.	1,5	A
Pin 5	$\pm I_5$	max.	10	mA
Pin 2	I_2	max.	3	mA
Pin 1	I_1	max.	50	mA
	$-I_1$	max.	0,1	mA
Pin 6	$-I_6$	max.	5	mA
Pin 4	$-I_4$	max.	1	mA
Pin 8, pin 9 and cooling fin	internally limited by the short-circuit protection circuit			

Temperatures

Total power dissipation	internally limited by the short-circuit protection circuit	
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range	T_{amb}	0 °C to limiting values

PINNING

pin number	function	pin number	function
1.	sawtooth capacitor	7.	feedback input
2.	frequency storage information	8.	positive supply of output stage
3.	oscillator capacitor	9.	output
4.	oscillator resistor (adjustment)	10.	flyback generator output
5.	synchronization input/blanking output	11.	positive supply (V_P)
6.	sawtooth buffer stage output	12.	preamplifier input

CHARACTERISTICS

V_P = 22 V; T_{amb} = 25 °C; these characteristics are measured with respect to cooling fin (ground), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage/output stage					
Supply voltage	$V_{11} = V_P$	9	–	30	V
Output voltage					
at I_9 = 0,75 A	V_9	–	1,2	1,4	V
at $-I_9$ = 0,75 A	V_9	$(V_P - 1,9)$	$(V_P - 1,7)$	–	V
Flyback generator output voltage					
at I_{10} = 0,75 A	V_{10}	–	$(V_P - 2,0)$	–	V
Supply currents (without load)					
pin 11	I_{11}	–	10	–	mA
pin 8	I_8	–	3	–	mA
Output current	$\pm I_9$	–	–	1,2	A
Flyback generator peak current	$\pm I_{10}$	–	–	1,2	A
Feedback					
Preamplifier quiescent input currents	$-I_7 = -I_{12}$	–	0,1	–	μA
Synchronization					
Sync input voltage range	V_5	1,0	–	–	V
Synchronizing range		–	28	–	%
Oscillator/sawtooth generator					
Frequency setting input voltage	V_4	6	–	9	V
Sawtooth generator output voltage (peak value)	$V_{1(m)}$	0	$(V_P - 2)$	–	V
Sawtooth generator output current	I_1	–	–	30	mA
Sawtooth generator leakage current	$-I_1$	2	–	–	μA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	–	10^{-4}	–	K^{-1}
Oscillator voltage dependency V_P = 10 to 30 V	$(\Delta f/f)/\Delta V_P$	–	10^{-3}	–	V^{-1}
Blanking pulse generator					
Output voltage (at I_5 = 1 mA)	V_5	–	20	–	V
Output resistance	R_5	–	410	–	Ω
Output current (at V_P = 21 V)	$-I_5$	–	–	5	mA
Blanking pulse duration at 50 Hz sync	t_b	1,33	1,4	1,47	ms
50/60 Hz frequency detector					
Output saturation voltage (LOW level for 50 Hz)	V_2	–	1	–	V
Leakage current	I_2	–	1	–	μA

parameter	symbol	min.	typ.	max.	unit
Buffer stage					
Output voltage	$V_{6(m)}$	0	$(V_P - 1)$	–	V
Output current	$-I_6$	–	–	4	mA
Thermal resistance					
From junction to case (cooling fin)	$R_{th\ j\text{-}c}$	–	–	15	K/W
Junction temperature					
Switching point thermal protection	T_j	142	150	158	°C

APPLICATION INFORMATION

The following application data is obtained from measurements made on the circuits shown in Figs 2 and 3, application circuits for 90° deflection systems. Measurements are made with respect to the cooling fin (ground).

			Fig. 2 concept 1*	Fig. 3 concept 2*	
System supply voltages	V_{P1}	typ.	22	22	V
	V_{P2}	typ.	12	–	V
Supply currents	I_{P1}	typ.	135	140	mA
	$-I_{P2}$	typ.	8	–	mA
Output voltage (d.c. value)	V_9	typ.	12,2	13,8	V
Output voltage (peak-to-peak value)	$V_{9(p\text{-}p)}$	typ.	42	43	V
Output current (peak value)	$-I_{9(m)}$	typ.	450	450	mA
Deflection current (peak-to-peak value)	$I_{defl\ (p\text{-}p)}$	typ.	850	850	mA
Flyback time	t_{fl}	typ.	0,9	1,0	ms
Oscillator frequency adjustment without sync	f_o	typ.	46,5	46,5	Hz
Total power dissipation per package (see note)	P_{tot}	max.	1,8	1,8	W
Ambient temperature	T_{amb}	max.	70	70	°C
Thermal resistance (junction to ambient)	$R_{th\ j\text{-}a}$	max.	40	40	K/W

*Concept 1 : with two supply voltages; concept 2 : with one supply voltage.

Note

Calculated with ΔV_{P1} of +5% and ΔR_{defl} of −7%.

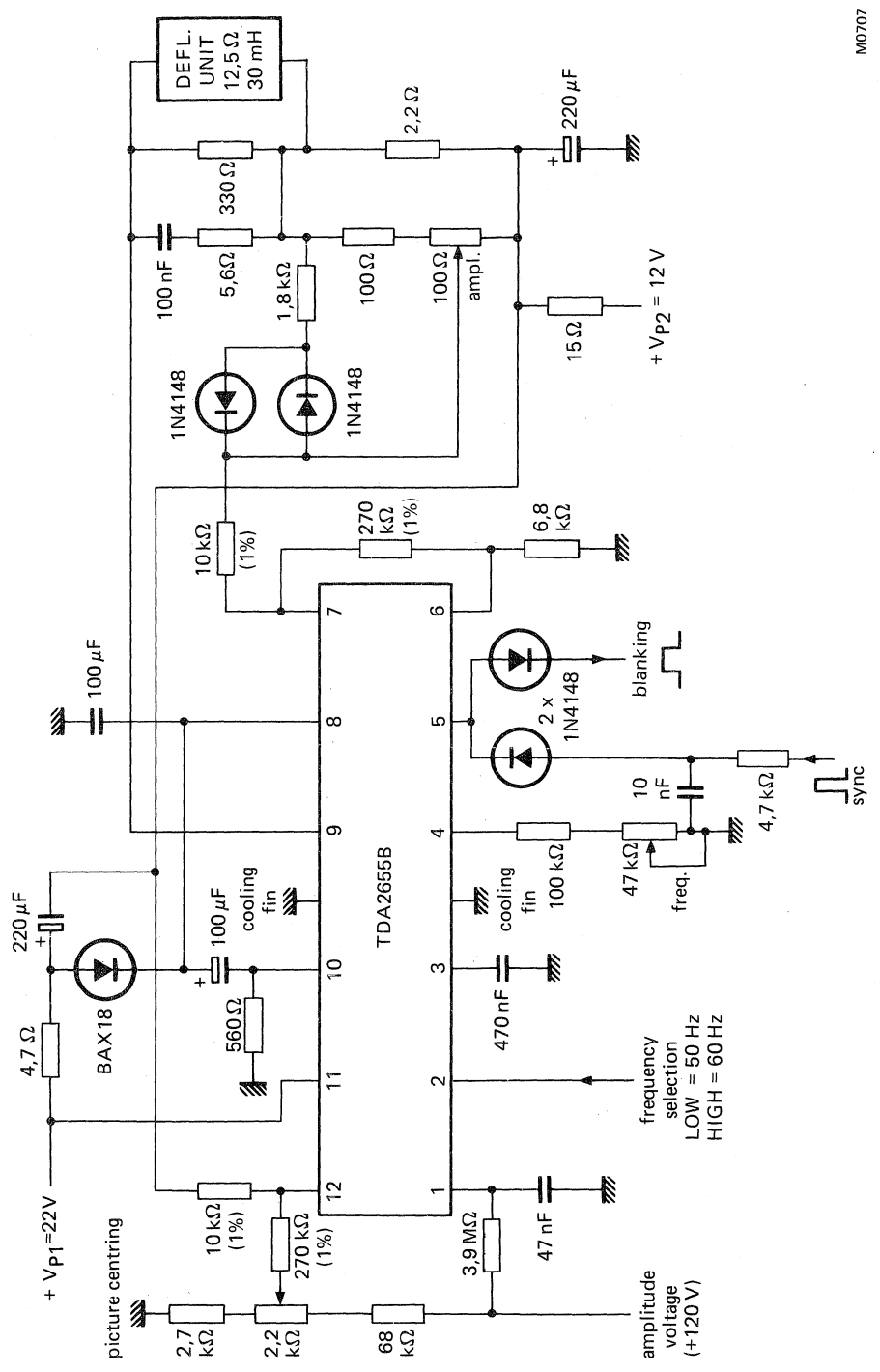


Fig. 2 Typical application circuit with two supply voltages; for use with 90° picture tubes.

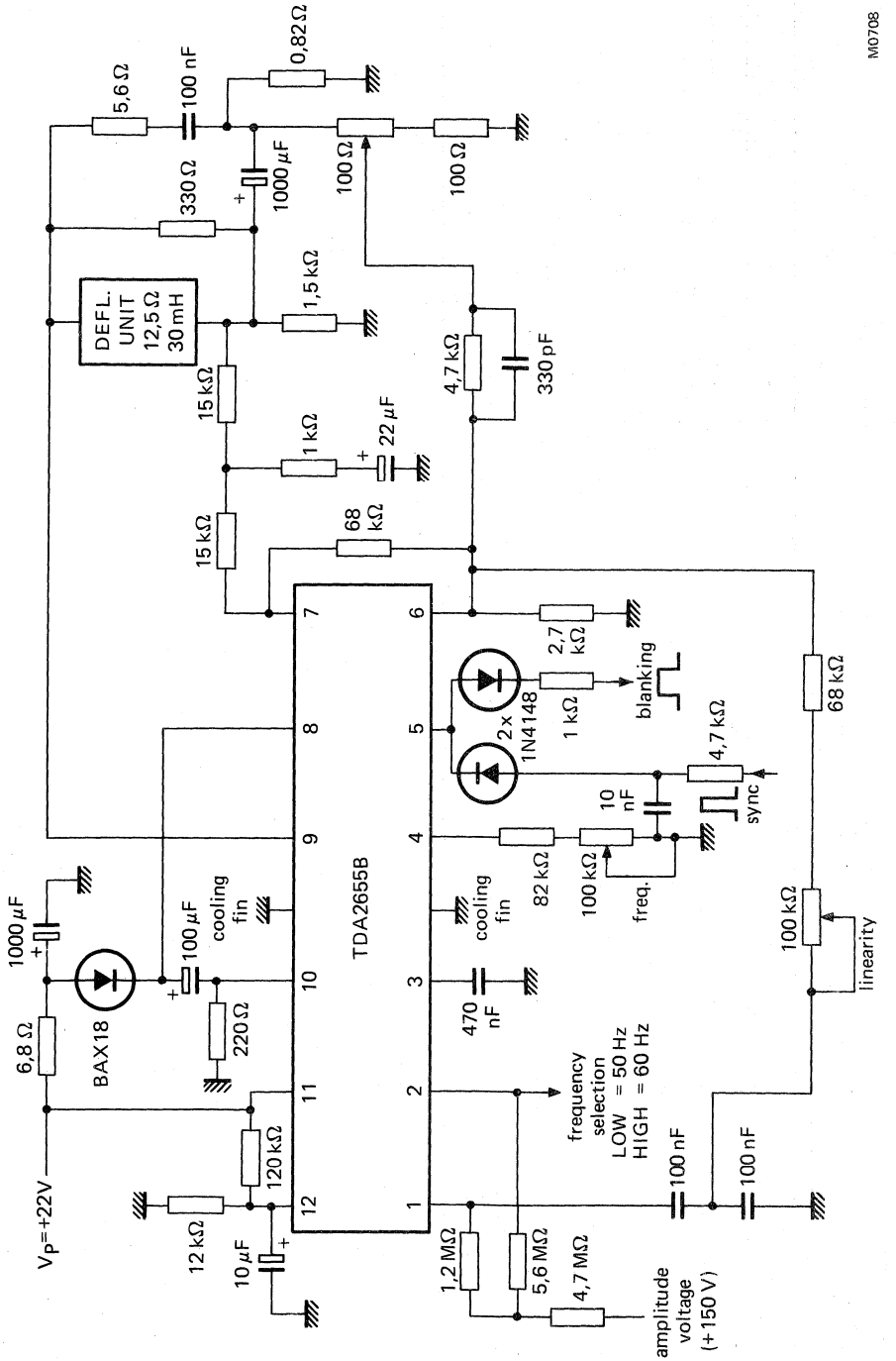


Fig. 3 Typical application circuit for a single supply voltage; for use with 90° picture tubes.

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